TEXAS INSTRUMENTS

Design Considerations for Logic Products

Application Book

1997

Advanced System Logic Products

General Design Considerations 1
Backplane Design 2
Device-Specific Design Aspects 3
5-V Logic Design 4
3.3-V Logic Design 5
Clock-Distribution Circuits (CDC) 6
Boundary-Scan IEEE Std 1149.1 (JTAG) Logic 7
Packaging 8
Index 9

Design Considerations for Logic Products

Application Book

Printed on Recycled Paper

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Printed in U.S.A. by
Custom Printing Company
Owensville, Missouri

INTRODUCTION

This collection of application reports and articles is intended to provide the design engineer with a valuable technical reference for Texas Instruments (TI) products. It contains reports written or revised between September 1992 and March 1997. The book is divided into eight sections, each focusing on different aspects of design decisions.

Section 1, ***General Design Considerations***, includes discussions about logic features, such as the bypass capacitor and output-damping resistor, and provides answers to difficult questions, such as how to improve electromagnetic compatibility and what negative consequences can arise when operating ICs outside their recommended operating conditions.

Section 2, ***Backplane Design***, includes reports on TI's Gunning Transceiver Logic (GTL) and Backplane Transceiver Logic (BTL) families. Aspects of line reflection and live insertion also are considered.

Each design is ultimately the result of several individual-device decisions. Consequently, the designer needs skew, transition rise and fall times, input characteristics, and waveforms for many devices. Section 3, ***Device-Specific Design Aspects***, covers these topics and many more for TI's most popular product lines. TI is dedicated to providing support for older families, while remaining on the cutting edge of technology. Section 3 includes our most popular CMOS (AC, ACT, ALVC, LV, LVC, and HC) and BiCMOS (ABT, ALB, BCT, and LVT) logic families, as well as some of our older technologies (ALS, AS, F, LS, and S).

Section 4, ***5-V Logic Design***, delivers more specific information on the Advanced BiCMOS Technology (ABT), Advanced High-Speed CMOS (AHC), Crossbar Technology (CBT), and Advanced Schottky (AS) logic families. ABT and AHC devices are the recommended families for high-to-medium-performance 5-V designs.

As process geometries continue to decrease in size to accommodate higher performances, system voltage requirements decline as well. In addition, end-consumer segments are always looking for ways to extend battery life. Section 5, ***3.3-V Logic Design***, contains reports designed to aid the 5-V to 3.3-V transition and highlights the Low-Voltage CMOS (LVC) logic family.

Section 6, ***Clock-Distribution Circuits (CDC)***, provides information on skew, electromagnetic interference (EMI) prevention, and phase-lock loop (PLL) based clock drivers.

As packaging trends and increased device functionality continue to allow smaller packages, board testing will become increasingly difficult. IEEE Std 1149.1 (JTAG) and TI's boundary-scan logic devices are the answer. Section 7, ***Boundary-Scan IEEE Std 1149.1 (JTAG) Logic***, includes 12 reports that give designers the facts on built-in self-test and designing with boundary-scan logic.

Section 8, ***Packaging***, covers DIP to TVSOP packages and concludes with a discussion of package thermal considerations.

Section 9, ***Index***, is a comprehensive index to topics in this book.

For more information on these or other TI products, please contact your local TI representative, authorized distributor, the TI technical support hotline at 972-644-5580, or visit the TI logic home page at http://www.ti.com/sc/logic.

For a complete listing of all TI logic products, please order our logic CD-ROM (literature number SCBC001) and/or Logic Selection Guide (literature number SDYU001) by calling our literature response center at 1-800-477-8924.

Contents

1 General Design Considerations 1–1

The Bypass Capacitor in High-Speed Environments 1–3
Printed-Circuit-Board Layout for Improved Electromagnetic Compatibility 1–15
Bus-Interface Devices With Output-Damping Resistors or Reduced-Drive Outputs 1–29
Designing With Logic 1–47

2 Backplane Design 2–1

GTL/BTL: A Low-Swing Solution for High-Speed Digital Logic 2–3
Next-Generation BTL/Futurebus Transceivers Allow Single-Sided SMT Manufacturing 2–19
The Bergeron Method: A Graphic Method for Determining Line Reflections in Transient Phenomena ... 2–31
Live Insertion 2–59

3 Device-Specific Design Aspects 3–1

Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices 3–3
Implications of Slow or Floating CMOS Inputs 3–17
Input and Output Characteristics of Digital Integrated Circuits 3–33
Metastable Response in 5-V Logic Circuits 3–71
Timing Measurements With Fast Logic Circuits 3–87
Designing With the SN54/74LS123 3–127
Digital Phase-Locked Loop Design Using SN54/74LS297 3–147

4 5-V Logic Design 4–1

ABT Enables Optimal System Design 4–3
Advanced High-Speed CMOS (AHC) Logic Family 4–21
Advanced Schottky Load Management 4–43
SN74CBTS3384 Bus Switches Provide Fast Connection and Ensure Isolation 4–83
Texas Instruments Crossbar Switches 4–91

5 3.3-V Logic Design 5–1

5-V to 3.3-V Translation With the SN74CBTD3384 5–3
Low-Cost, Low-Power Level Shifting in Mixed-Voltage Systems 5–11
LVC Characterization Information 5–21
Mixing It Up With 3.3 Volts 5–45
CMOS Power Consumption and C_{pd} Calculation 5–55

Contents (Continued)

6 Clock-Distribution Circuits (CDC) ***6–1***

Application and Design Considerations for the CDC5XX Platform of Phase-Lock Loop Clock Drivers ... 6–3
Clock Distribution in High-Performance PCs ... 6–23
EMI Prevention in Clock-Distribution Circuits ... 6–33
Minimizing Output Skew Using Ganged Outputs ... 6–49
Phase-Lock Loop-Based (PLL) Clock Driver: A Critical Look at Benefits Versus Costs ... 6–59

7 Boundary-Scan IEEE Std 1149.1 (JTAG) Logic ***7–1***

Boundary Scan Speeds Static Memory Tests ... 7–3
Design-For-Test Analysis of a Buffered SDRAM DIMM ... 7–13
Hierarchically Accessing 1149.1 Applications in a System Environment ... 7–29
JTAG/IEEE 1149.1 Design Considerations ... 7–41
A Look at Boundary Scan From a Designer's Perspective ... 7–57
Partitioning Designs With 1149.1 Scan Capabilities ... 7–73
A Proposed Method of Accessing 1149.1 in a Backplane Environment ... 7–87
Built-In Self-Test (BIST) Using Boundary Scan ... 7–101
Design Tradeoffs When Implementing IEEE 1149.1 ... 7–113
Impact of JTAG/1149.1 Testability on Reliability ... 7–127
System Testability Using Standard Logic ... 7–139
What's an LFSR? ... 7–155

8 Packaging ***8–1***

Medium-Pin-Count Surface-Mount Package Information ... 8–3
Comparison of the Packages DIP, SOIC, SSOP, TSSOP, and TQFP ... 8–13
Recent Advancements in Bus-Interface Packaging and Processing ... 8–37
Thin Very Small-Outline Package (TVSOP) ... 8–49
Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices ... 8–95

9 Index ***9–1***

General Design Considerations 1
Backplane Design 2
Device-Specific Design Aspects 3
5-V Logic Design 4
3.3-V Logic Design 5
Clock-Distribution Circuits (CDC) 6
Boundary-Scan IEEE Std 1149.1 (JTAG) Logic 7
Packaging 8
Index 9

Contents

Page

The Bypass Capacitor in High-Speed Environments 1–3
Printed-Circuit-Board Layout for Improved Electromagnetic Compatibility 1–15
Bus-Interface Devices With Output-Damping Resistors or Reduced-Drive Outputs 1–29
Designing With Logic 1–47

The Bypass Capacitor in High-Speed Environments

SCBA007A
November 1996

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title *Page*

Introduction **1–7**

Bypass Definition **1–7**

Bypassing Considerations **1–7**
- Capacitor Type 1–8
- Capacitor Placement 1–8
- Output Load Effect 1–10
- Capacitor Size 1–13

Summary **1–14**

References **1–14**

List of Illustrations

Figure *Title* *Page*

1 V_{CC} Line Disturbance vs Frequency 1–7
2 Typical Power Layout 1–8
3 Capacitive Storage (Bypass Capacitor) 1–9
4 V_{CC} Line Disturbance vs Capacitor Size at Different Distances 1–9
5 V_{CC} Line Disturbance vs Capacitor Size With Resistive Load at Different Frequencies 1–10
6 V_{CC} Line Disturbance vs Capacitor Size With 60-pF Load at Different Frequencies 1–11
7 V_{CC} Line Disturbance vs Capacitor Size at Different Capacitive Loads 1–12
8 I_{CC} vs Frequency 1–13
9 V_{CC} Line Disturbance vs Frequency 1–14

Widebus is a trademark of Texas Instruments Incorporated.

Introduction

High-speed switching environments generate noise on power lines (or planes) due to the charging and discharging of internal and external capacitors of an integrated circuit. The instantaneous current generated with the rising and falling edges of the outputs causes the power line (or plane) to ring. This behavior can violate the V_{CC} recommended operating conditions or generate false signals, creating serious problems. A simple and easy solution must be considered to prevent such a problem from occurring. This solution is the bypass capacitor.

Bypass Definition

A bypass capacitor stores an electrical charge that is released to the power line whenever a transient voltage spike occurs. It provides a low-impedance supply, thereby minimizing the noise generated by the switching outputs of the device.

Bypassing Considerations

A system without bypassing techniques can create severe power disturbance and cause circuit failures. Figure 1 shows the V_{CC} line of the 'ABT541 ringing while all outputs are switching. Note that there is no bypass capacitor at the V_{CC} pin. There are a few issues that should be considered when bypassing power lines (or planes).

- The capacitor type
- The capacitor placement
- The output load effect
- The capacitor size

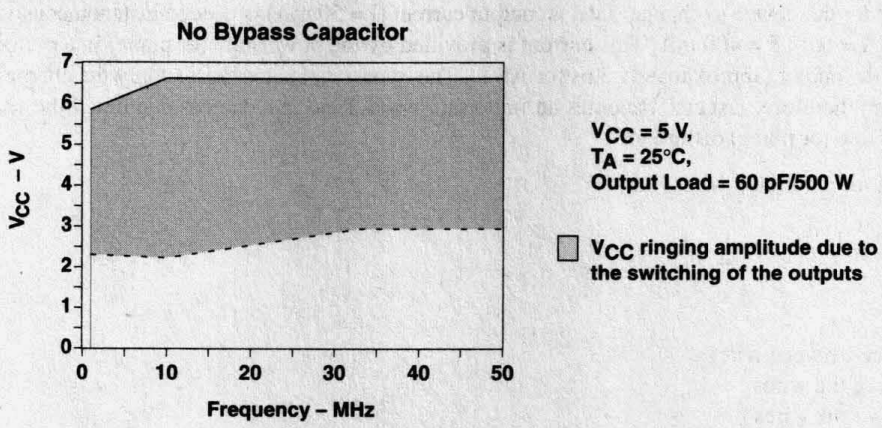


Figure 1. V_{CC} Line Disturbance vs Frequency

Capacitor Type

In a high-speed environment the lead inductances of a bypass capacitor become very critical. High-speed switching of a part's outputs generates high frequency noise (>100 MHz) on the power line (or plane). These harmonics cause the capacitor with high lead inductance to act as an open circuit, preventing it from supplying the power line (or plane) with the current needed to maintain a stable level, and resulting in functional failure of the circuit. Therefore, bypassing a power line (or plane) from the device internal noise requires capacitors with very small inductances. That is why the multilayer ceramic chip capacitors (MLC) are more favorable than others for bypassing power lines (or planes). They exhibit negligible internal inductance, thereby allowing the charge to flow easily, when needed, without degradation.

Capacitor Placement

Most of the printed circuit boards are designed to maintain a short distance between power and ground. This is done by laminating the power line (or plane) with the ground plane and can be electrically approximated with lumped capacitances as shown in Figure 2. However, this is not enough to have a reliable system, and another technique must be considered to provide a low-impedance path for the transient current to be grounded. This can be done by placing the bypass capacitor close to the power pin of the device.

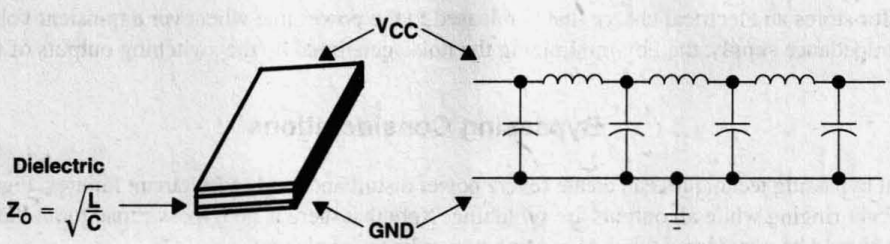


Figure 2. Typical Power Layout

Why This Location Is Very Important

Consider a device driving a line from low to high having an impedance ($Z \cong 100\ \Omega$) and a supply voltage ($V_{CC} = 5$ V) (see Figure 3). In order for the device to change state, an output current ($I = 50$ mA) is needed instantaneously. Note that for eight outputs switching, $I = 50 \times 8 = 400$ mA. This current is provided by the power line (or plane) in a period less than or equal to the rise time of the output (approximately 3 ns for ABT). The bypass capacitor must supply the charge in that same period to avoid V_{CC} drop; therefore, distance becomes an important issue. Line inductances can block the charge from flowing, leaving the power line (or plane) disturbed.

Using the formula for paralleled wires:

$$L = l\frac{\mu_0}{\pi}\ln\frac{d}{r} \quad (1)$$

Where:

- d = distance between wires
- l = length of the wires
- r = radius of the wires
- μ_0 = permeability of medium between wires

The inductance (L) is directly proportional to the distance between the lines as well as the length of the lines. Therefore, by reducing the loop ABCD in Figure 3, the inductance is minimized, allowing the capacitor to function more efficiently and, hence, keep the noise off the power line (or plane).

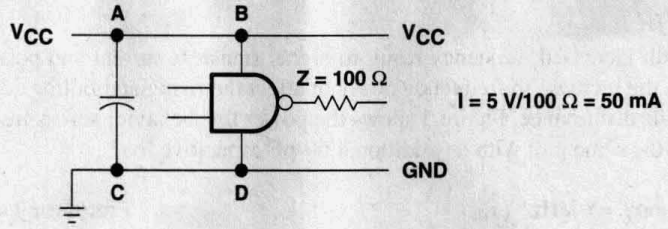


Figure 3. Capacitive Storage (Bypass Capacitor)

Several tests were performed on an 'ABT541 device to study the behavior of its power line (or plane) as the outputs switch simultaneously. This data is taken at different distances from the power pin (0.3, 1, and 2 inches) using four capacitors (0.001, 0.01, 0.1, and 1 μF), with an input frequency of 33 MHz and all eight outputs switching simultaneously (worst case). Figure 4 shows that the line disturbance increases as the capacitor is moved away from the power pin.

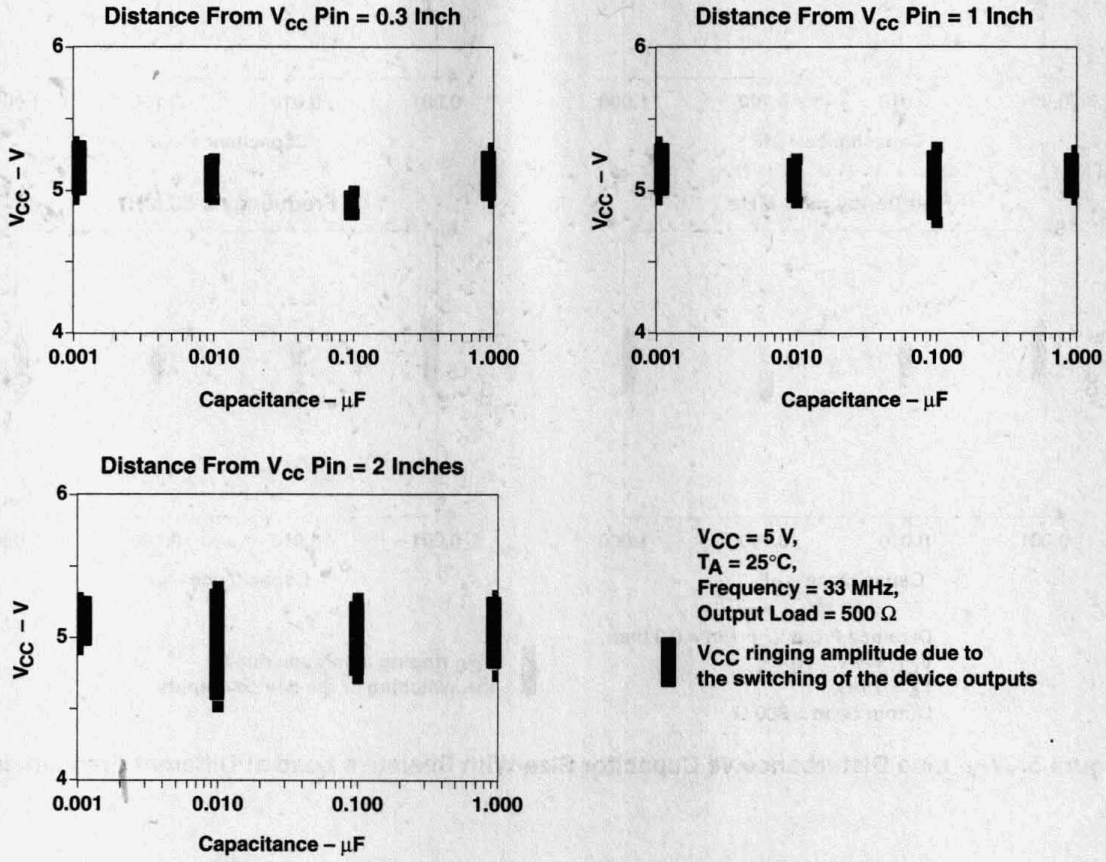


Figure 4. V_{CC} Line Disturbance vs Capacitor Size at Different Distances

Output Load Effect

Capacitive loads combined with increased frequency result in higher transient current and possible V_{CC} oscillation. If the output load is purely resistive, the increase in frequency does not affect the rising and falling edge of the outputs; therefore, it does not increase the V_{CC} line disturbance. Figure 5 shows the power line behavior across frequency while driving only a resistive load. Figure 6 shows the same plot with an additional 60-pF capacitive load.

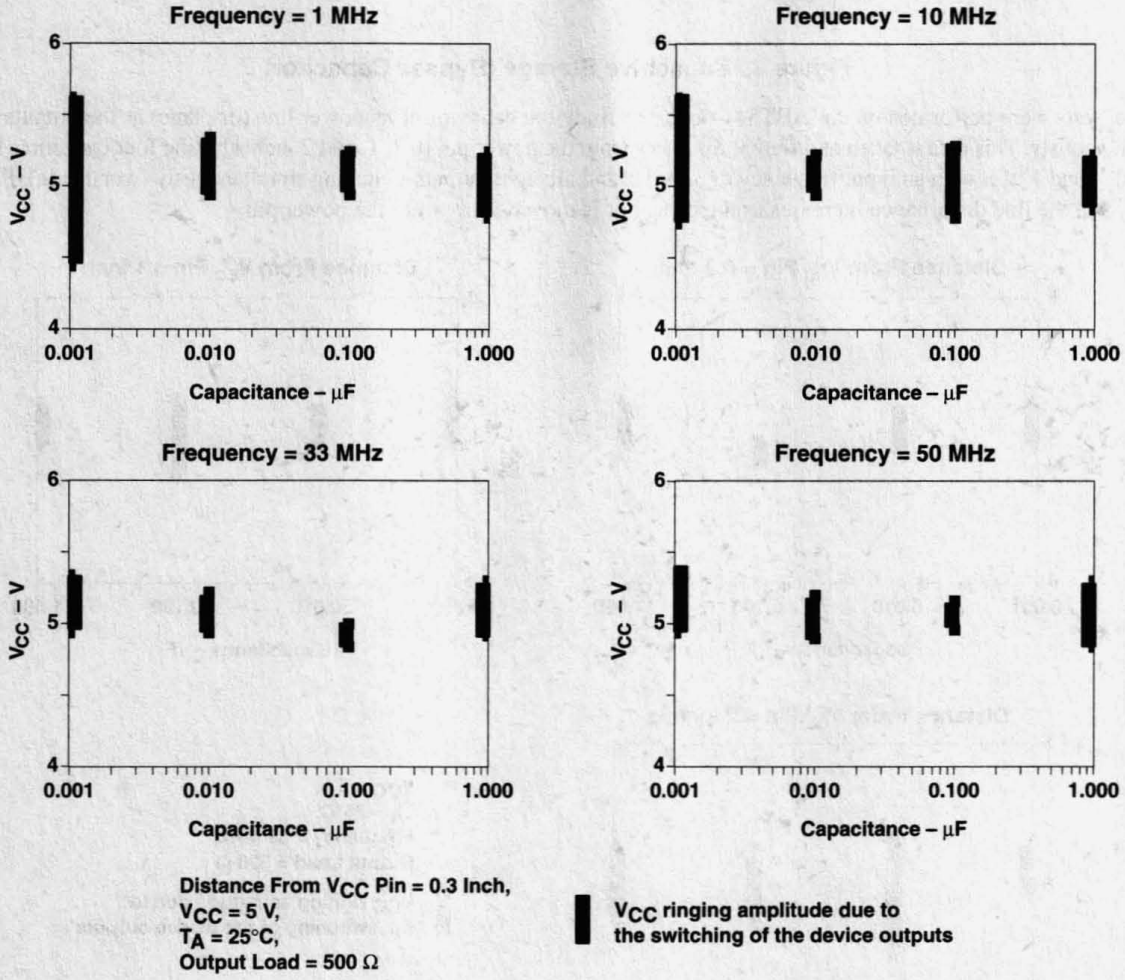


Figure 5. V_{CC} Line Disturbance vs Capacitor Size With Resistive Load at Different Frequencies

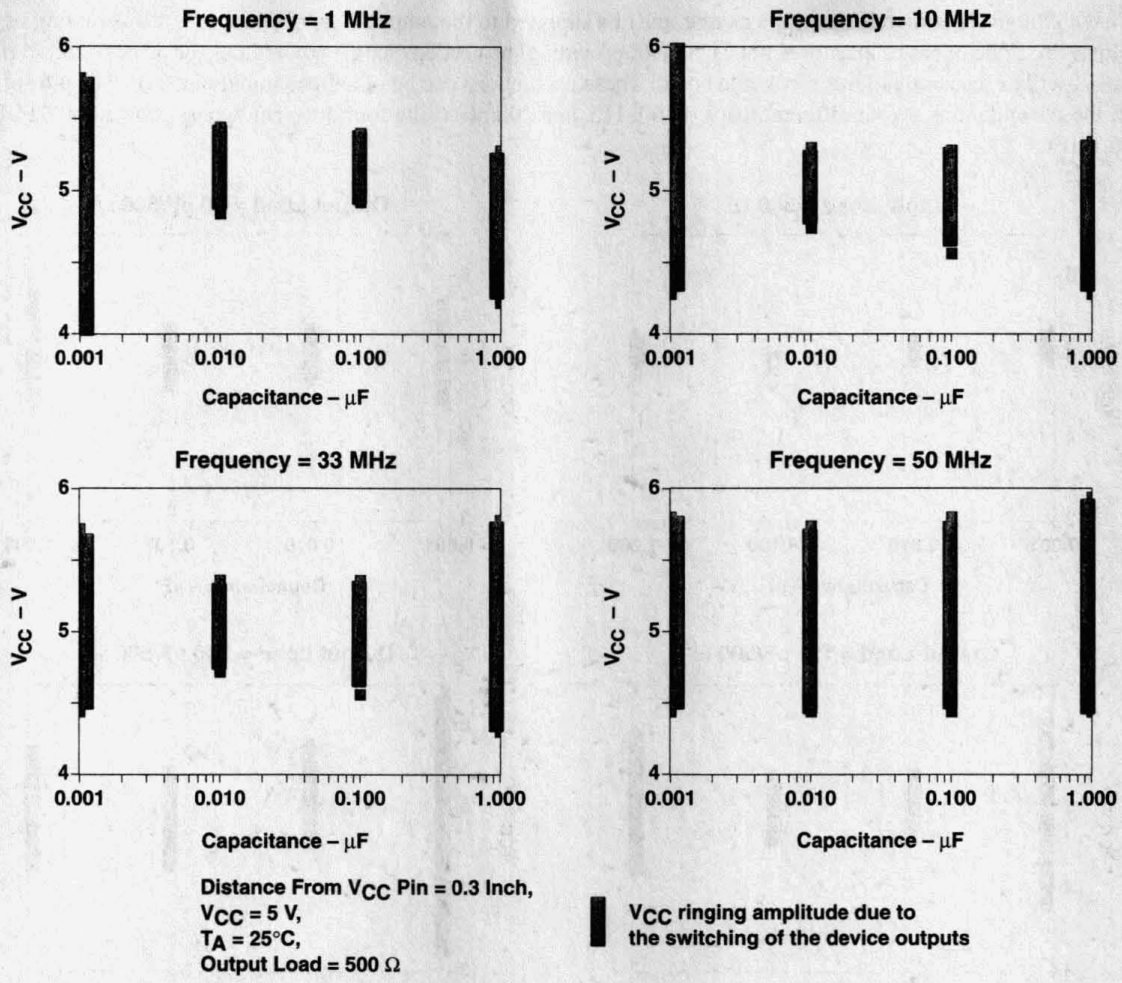


Figure 6. V_{CC} Line Disturbance vs Capacitor Size With 60-pF Load at Different Frequencies

When driving large capacitive loads, more charge must be supplied to the output load, resulting in a slower rising or falling edge. However, if the bypass capacitor is not capable of providing the needed charge, power lines (or planes) start to ring and eventually oscillate, causing failures across the board. These oscillations can be of a great amplitude, 2- to 3-V p-to-p. Figure 7 shows these oscillations at four different loads (0, 60, 115, and 200 pF) using four different bypass capacitors (0.001, 0.01, 0.1, and 1 μF).

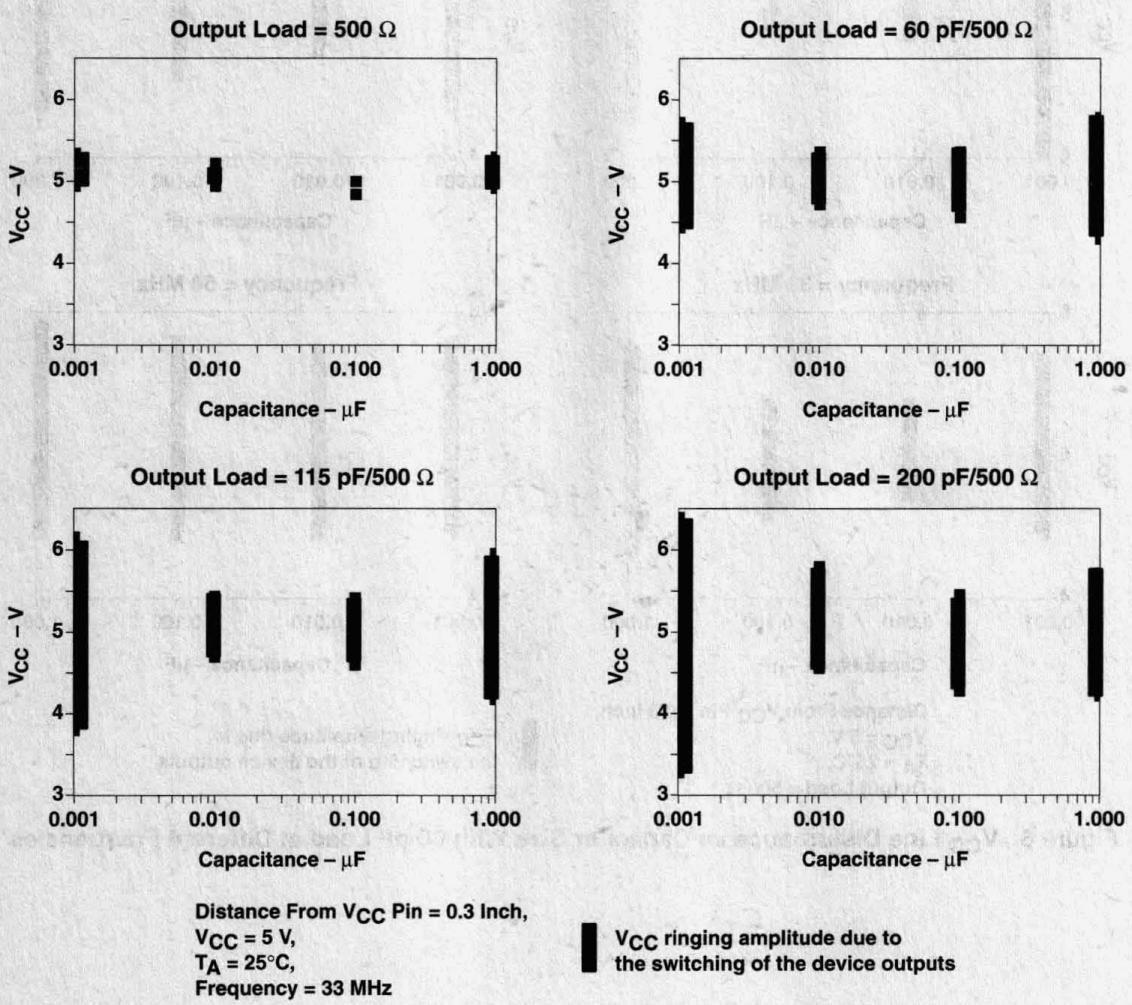


Figure 7. V_{CC} Line Disturbance vs Capacitor Size at Different Capacitive Loads

Capacitor Size

How can we choose the right bypass capacitor? The most important parameter is the ability to supply instantaneous current when it is needed.

There are two ways to calculate the bypass-capacitor size for a device:

1. The amount of current needed to switch one output from low to high (I), the number of outputs switching (N), the time required for the capacitor to charge the line (Δt), and the drop in V_{CC} that can be tolerated (ΔV) must be known.

   The following equation can be used:

$$C = \frac{I \times N \times \Delta t}{\Delta V} \quad (2)$$

   where Δt and ΔV can be assumed.

For example, with $\Delta V = 0.1$ V, $\Delta t = 3$ ns, N = 8, and I obtained from either Figure 3 (for rough estimate) or from the plot in Figure 8 (assuming 50-MHz frequency), using I = 44 mA, the equation is:

$$C = \frac{44 \times 10^{-3} \times 8 \times 3 \times 10^{-9}}{0.1} = 10080 \times 10^{-12} = 0.01\ \mu F \quad (3)$$

2. Several capacitor manufacturers specify the maximum pulse slew rate. This allows the capacitor's maximum current to be calculated. For example, a 0.1-µF capacitor rated at 50 V/µs can supply: $i = c\ dv/dt = 0.1 \times 50 = 5$ A. This current is greater than the maximum current (I × N = 44 mA × 8 outputs switching = 352 mA) required by the device used in the previous example.

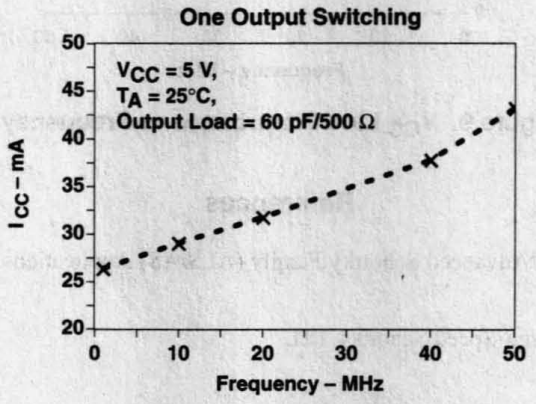


Figure 8. I_{CC} vs Frequency

Summary

Bypass capacitors play a major role in achieving reliable systems. The absence of the bypass capacitor can generate false signals and create major problems across the entire board. Figure 1 shows the undesired ringing caused by simultaneously switching the outputs of the 'ABT541. Also, choosing a capacitor with negligible lead inductance can avoid unpredictable behavior at high frequencies. Locating the capacitor closer to the V_{CC} pin of a device can avoid further complications and eliminate the ringing entirely. Figure 6 shows the V_{CC} line behavior with the bypass capacitor placed 0.3 inch away from the V_{CC} pin, whereas Figure 9 shows the same plot with the same load, but the bypass capacitor is located at the pin; there is dramatic improvement in the latter case. This technique can also be applied to Texas Instruments Widebus™ family by bypassing all V_{CC} pins. This is the most effective method for eliminating the V_{CC} line ringing. It is always important to minimize the loop between the V_{CC} pin, the ground, and the bypass capacitor. Finally, choosing the capacitor size by using either method mentioned earlier is highly recommended. If one considers all these issues, a good bypass technique can be employed.

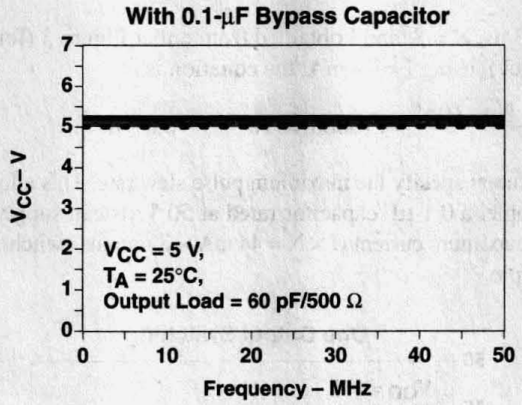


Figure 9. V_{CC} Line Disturbance vs Frequency

References

1 Texas Instruments Incorporated, "Advanced Schottky Family (ALS/AS) Applications," *ALS/AS Logic Data Book*, 1995, literature number SDAD001C.

2 Walton, D., "P.C.B. Layout for High-Speed Schottky TTL".

Printed-Circuit-Board Layout for Improved Electromagnetic Compatibility

SDYA011
October 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	*Page*
Abstract	**1–19**
Introduction	**1–19**
Behavior of Digital Circuits	**1–20**
Suppression of Interference on Supply Lines	**1–21**
Suppression of Interference on Signal Lines	**1–24**
Oscillator	**1–26**
Summary	**1–28**

List of Illustrations

Figure	*Title*	*Page*
1	Current Paths in an Electronic System	1–19
2	CMOS Inverter Circuit	1–20
3	Supply Current of CMOS Circuits as a Function of the Input Voltage	1–20
4	Circuit With Parasitic Components	1–21
5	Currents in the Supply Lines	1–22
6	Currents in the Supply Lines Using an Inductor	1–23
7	Placement of the IC, C_B, and L_{CH}	1–24
8	Arrangement of Signal Lines and Their Return Lines	1–24
9	Currents in Signal and Supply Lines	1–25
10	Layout of Signal and Ground Lines	1–25
11	Crystal Oscillator Circuit	1–26
12	Proposal for the Layout of the Metallization for an Oscillator	1–27

Abstract

The significance of electromagnetic compatibility (EMC) of electronic circuits and systems has recently been increasing. This increase has led to more stringent requirements for the electromagnetic properties of equipment. Two property aspects are of interest: the ability of a circuit to generate the lowest (or zero) interference, and the immunity of a circuit to the effects of the electromagnetic energy it is subjected to. The effects on electronic circuits and systems is well documented, but little attention has been paid to circuit behavior and the interference it generates. This application report explains important criteria that determine the EMC of a circuit and, thus, provides the development engineer with information for the design of circuits and layout of circuit boards.

Introduction

The EMC of an electronic circuit is mainly determined by how components are laid out with respect to each other and by how electrical connections are made between components. Every current flowing in a line generates a current of the same magnitude flowing in a corresponding return line. This line loop creates an antenna that can radiate electromagnetic energy whose magnitude is determined by the current amplitude, the repetition frequency of the signal, and the geometrical area of the current loops. Figure 1 shows the current paths of a typical circuit layout.

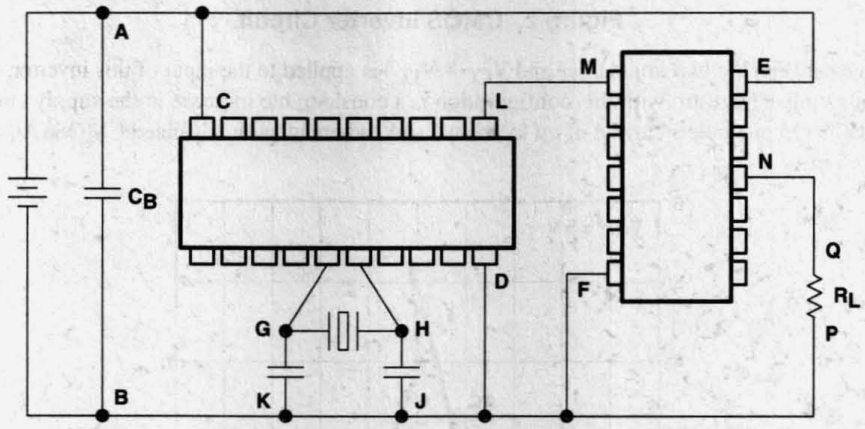


Figure 1. Current Paths in an Electronic System

Classes of lines that contribute, in varying degrees, to the undesirable radiation that is generated are:

- The supply lines in Figure 1 form loops A–C–D–B and A–E–F–B. The energy the system needs to operate is conducted by these lines. Since the power consumption of the circuit is not constant but depends on its instantaneous state, then all the frequency components generated in the individual parts of the system are represented on these supply lines. Because of the relatively high impedance of the supply lines (usually about 100 Ω), fast current changes cannot be suppressed while en route, therefore, this function must be fulfilled by the blocking capacitor (C_B).
- Additional loops are formed by the signal and control lines (L–M–F–D and N–Q–P–F). The area these lines enclose is usually small, if those lines outside the system are not considered. These lines often transmit signals at high frequencies, so signal and control lines must be considered.
- The oscillator circuit and its external frequency-determining components form loop G–H–J–K. Since the highest frequencies are usually found at this point, particular care must be taken with the design of the circuit to avoid unnecessary interference voltages and, with the routing of connecting lines, to minimize the effective areas of the antennas.

Behavior of Digital Circuits

Knowing the relationships of several important properties of logic circuits leads to specific and effective ways of improving EMC. These properties are demonstrated with CMOS integrated circuits (ICs). An example will help explain several improving effects that arise in a similar way with other device technologies.

Figure 2 shows the circuit of a simple inverter constructed with N-channel and P-channel transistors. If a voltage, V_I, is applied to the input, which is less than the threshold voltage (V_{IT-}) of the N-channel transistor, this transistor will be nonconducting, whereas, the P-channel transistor will conduct. In the opposite way, the N-channel transistor will conduct and the P-channel transistor will be nonconducting if a voltage $V_I > V_{CC} - V_{IT+}$ is applied at the input (V_{IT+} is the threshold voltage of the P-channel transistor). In both cases, no current, except negligible leakage currents, flows through the circuit. This is also the reason for the extremely low current consumption of CMOS circuits in a quiescent state.

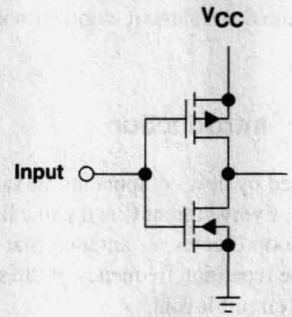


Figure 2. CMOS Inverter Circuit

However, if a voltage between the two limits (V_{IT} and $V_{CC} - V_{IT}$) is applied to the input of this inverter, both transistors will be more or less conducting. The result with this configuration is a considerable increase in the supply current (see Figure 3). In such a case, HCMOS circuits take a current of up to about 1 mA, whereas, with advanced CMOS (AC), the supply current can increase to over 5 mA.

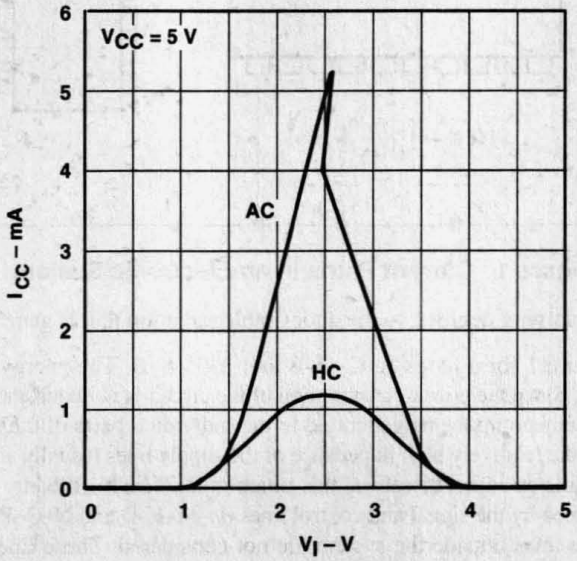


Figure 3. Supply Current of CMOS Circuits as a Function of the Input Voltage

Because the input voltage at such a circuit cannot traverse the critical voltage region when changing from a low to a high (or vice versa) in an infinitely short time, there is flow during this time of pulse-shaped current peaks (often known as current spikes), of such magnitude that cannot be neglected. In an input stage, current amplitudes of 1 mA to 5 mA must be expected (see Figure 3). Considerably more critical is this phenomenon at the outputs of an IC. Since the output stages must drive the load that is connected to the output, these transistors must be made considerably bigger. As a result, the amplitudes of the current peaks also increase correspondingly to values of from 20 mA for HCMOS devices to 60 mA for AC devices, with a pulse width of 5 ns to 10 ns.

Suppression of Interference on Supply Lines

The current peaks mentioned previously are one of the most significant causes of electromagnetic interference. Every time an output is switched, a corresponding pulse of current flows along the supply lines. The latter connections lead by a more or less direct route from the module to the central power supply. The problem will be aggravated when the outputs of an IC are switched at a high repetition rate, such as along the lines connecting a processor with its corresponding memory.

In practice, decoupling the supply voltage close to the IC with a ceramic capacitor (C_B = 100 nF) is recommended. In digital systems this technique is effective in ensuring that, with the expected load changes, no inadmissible supply voltage changes can occur. However, this will result in only a very limited reduction of the electromagnetic interference.

To achieve a significant improvement, it is first necessary to analyze the complete circuit and its parasitic components. Figure 4 shows the circuit under examination. Two transistors (Q1 and Q2) are the output stage of an IC whose behavior is to be analyzed. Connection to the surrounding circuitry is made with the $L_p/R_p/C_p$ network, which represents the parasitic components of the package. The following individual values are assumed:

- Inductance of the package leads L_p = 5 nH to 30 nH
- Capacitance of the package leads C_p = 1.5 pF to 3 pF
- Ohmic resistance of the package leads R_p = 0.1 Ω

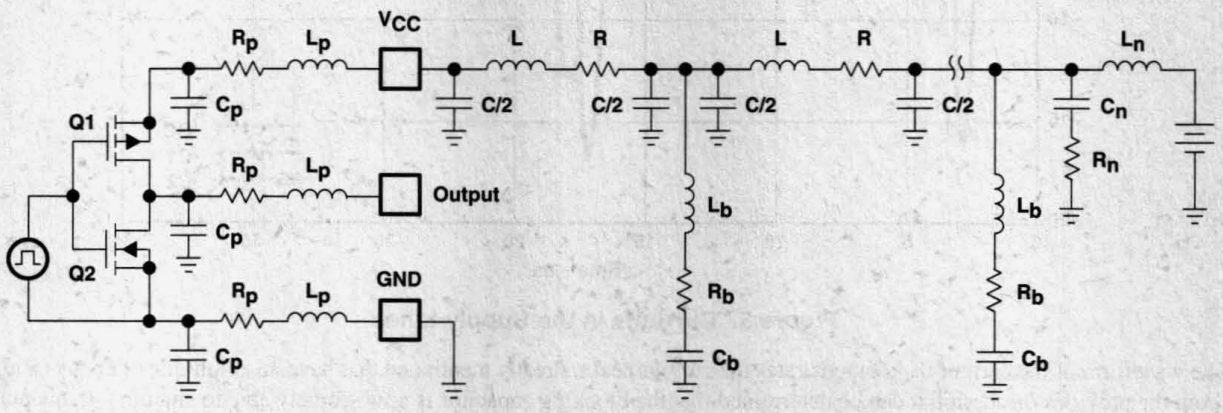


Figure 4. Circuit With Parasitic Components

From the supply terminals V_{CC} and GND of the IC, a connection is made to C_B as identified in Figure 1 across the dc source. The following values for the components of the impedance per unit of length of the line from the V_{CC} source on the circuit boards to the V_{CC} terminal of the IC are assumed:

- Inductance per unit length L' = 5 nH/cm
- Capacitance per unit length C' = 0.8 pF/cm
- Resistance per unit length R' = 0.01 Ω/cm

The supply line subsequently reaches the first blocking capacitor, C_B (see Figure 4, right-hand L_b, R_b, C_b totem), whose equivalent circuit is made up as follows:

- Capacitance C_b = 100 nF (typical value)
- Inductance of the leads L_b = 2 nH (SMD package)
- Resistive losses R_b = 0.2 Ω

From here, a long line (length = 5 cm) is taken to the next blocking capacitor, C_B (see Figure 4, center L_b, R_b, C_b totem); this line and the capacitor can also be represented by the same equivalent circuit as mentioned above. For simplicity, it will be assumed that the subsequent circuit can be represented by the well-known vehicle power-supply equivalent circuit components:

- Inductance L_n= 5 µH
- Capacitance C_n = 0.1 µF
- Resistance R_n = 50 Ω

The behavior of this circuit was simulated using a SPICE program; it was assumed that no load was connected to the output of the IC, i.e., the circuit was left open. Figure 5 shows the calculated current waveforms. The following definitions apply:

- I_{CC}: Current in the V_{CC} connection to the IC
- I_{C1}: Current in the first blocking capacitor
- I_{C2}: Current in the second blocking capacitor

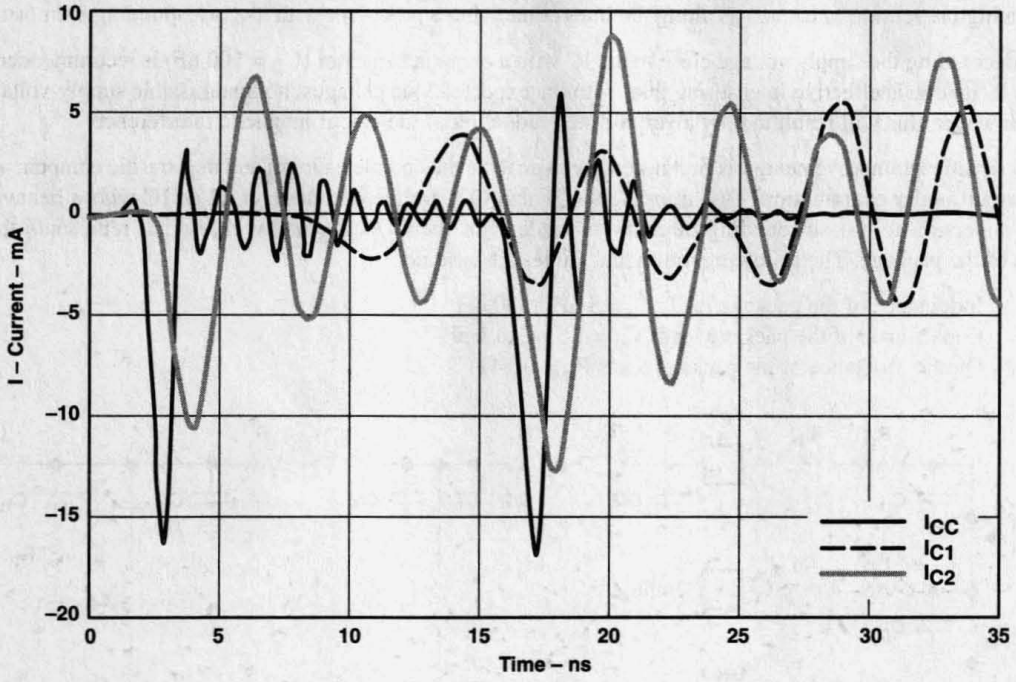


Figure 5. Currents in the Supply Lines

The waveform of the current I_{CC} demonstrates the current peaks already mentioned that have an amplitude of about 15 mA. From the previous discussion it can be determined that the blocking capacitor is now scarcely able to smooth out this pulse of current. In fact, the resonant circuit formed by the line inductance (principally that of the package of the IC) and the C_B will be excited, and an increase of current will take place (current I_{C1}). A major part of the current (I_{C2}) is transplanted via the supply line, and flows with a scarcely diminished amplitude also into the next C_B.

From the point of view of the EMC of the circuit shown, C_B, in this form, is unable to significantly reduce the radiated interference. The long supply lines – which, in practice, are always present – with the relatively large areas that these lines surround, form an effective antenna. At the frequencies present, an unacceptable level of interference is radiated.

To improve the behavior of the circuit, measures must first be taken to ensure that the spread in the system of the currents shown in Figure 5 is limited. This cannot be achieved with C_B alone; improvement of its properties, relative to the requirements detailed here, cannot be achieved. Because the inductance causing the interference has already been formed, to a large extent by the packages of the ICs and by the connection to the capacitor, no significant improvement can be achieved by simply connecting in parallel several capacitors having different capacitance values. Of greater concern is preventing the current causing the disturbance from reaching other parts of the circuit. This can be achieved by introducing an inductive coil behind the first C_B, which represents a sufficiently high resistance at high frequencies. In the simulated circuit, an inductor having an inductance L_{CH} = 1 µH was assumed, the impedance of which could be limited at high frequencies by a resistor of 50 Ω connected in parallel.

The results of the simulation are shown in Figure 6. As might be expected, the currents in the leads to the IC I_{CC} and in the first C_B (I_{C1}) have not become any smaller. However, Figure 6 shows that there is a reduction of the current amplitude (I_{CH}) by more than 20 dB after the inductor. This method can contribute to a significant reduction of the radiation.

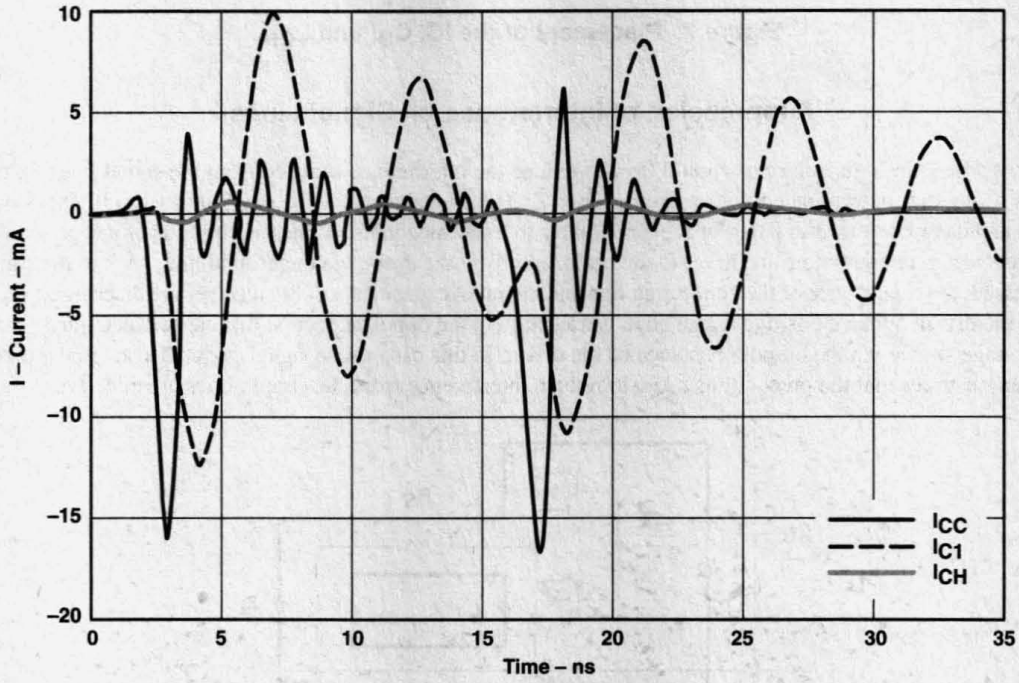


Figure 6. Currents in the Supply Lines Using an Inductor

Next is the question of how the individual components should be arranged on the circuit board to achieve the maximum reduction of the radiation. Figure 7 shows a circuit proposal for this purpose. A grounded area under the IC is connected to the GND pin of the circuit. This ground ensures that the major part of the field lines emanating from the IC are concentrated between the IC and ground level. As a result of the skin effect on the large surface area, the line inductance to C_B is reduced still further. It is immaterial whether the capacitor is situated near the positive (V_{CC}) or the negative (GND) supply connection. It is only important that the parasitic inductances and the effective areas of the antennas are kept as small as possible. The inductor (L_{CH}) should be as close as possible to the part of the circuit where the interference is to be suppressed.

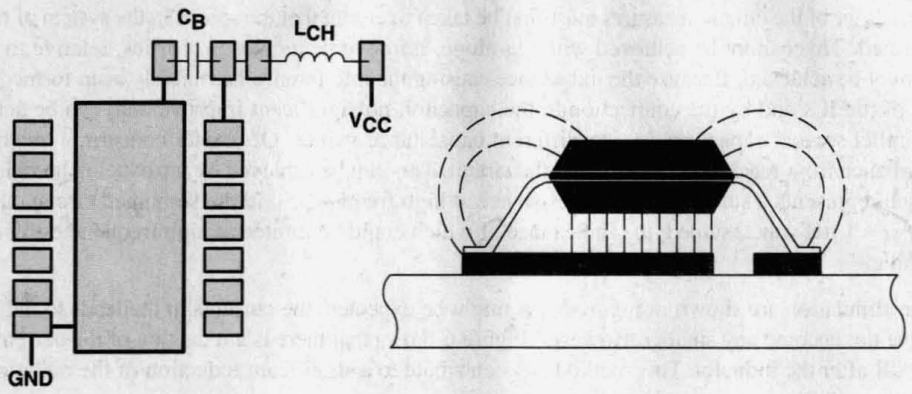


Figure 7. Placement of the IC, C_B, and L_{CH}

Suppression of Interference on Signal Lines

Figure 8 shows where the signal currents should flow to reduce the interference radiated from the signal lines. In this circuit, a gate drives a line that is terminated with an impedance Z. The impedance can be made up of the IC input capacitance (C_{IN} = 5 pF) and its input resistance (R_{IN}) of several kilohms to a few megohms. At the transmission of a negative signal edge, the current flows from the output of the driver to the drain, and from the drain, via the ground line, back to the signal source. Simply expressed, the capacitance of the connecting line and the input capacitance of the receiver are discharged via the output resistance of the driver. When a positive signal edge is transmitted, the opposite occurs: this capacitance must be charged by the supply voltage source via the output resistance of the driver. In this case, these signal currents also appear on the supply lines. This demonstrates that the precautions taken to reduce interference from the supply lines are effective.

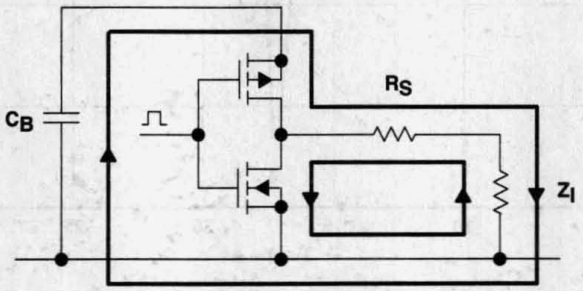


Figure 8. Arrangement of Signal Lines and Their Return Lines

Figure 9 shows the results of the simulation of the arrangement just discussed. In this example, the output of the IC drives a 5-cm-long line having a characteristic impedance (Z_O = 100 Ω) that is terminated at its end with 100 kΩ and 5 pF in parallel. As a result of the largely capacitive loading, the amplitude of the current peak I_{CC} is significantly reduced on the negative edge at the output V_{OUT}. The capacitance at the output keeps the voltage at this point at the original potential (high) for a short time and prevents a current flow through the upper transistor of the output stage (voltage difference = 0 V). At the positive edge, the signal current I_{OUT} is added to the lateral current in the output I_{CC}.

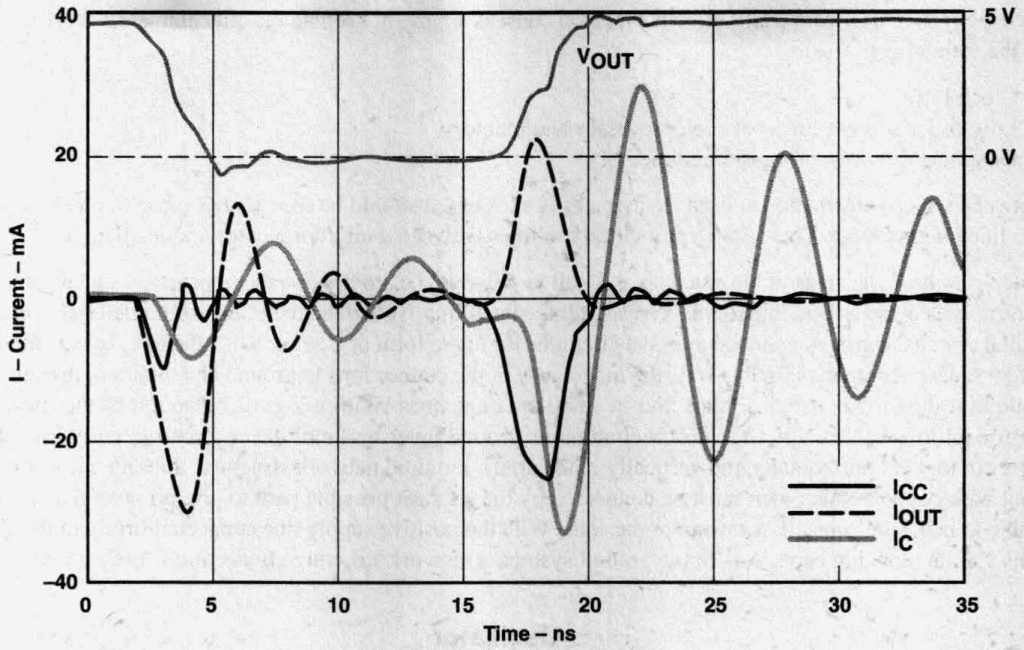


Figure 9. Currents in Signal and Supply Lines

Currents may be reduced by connecting a resistance (R_S) in series with the output. Line-transmission theory shows that this resistance has no negative influence on the speed of the circuit, provided the output resistance of the driver (consisting of its internal resistance + series-resistance R_S) is smaller than, or equal to, the characteristic impedance of the line (Z_O = 70 Ω to 120 Ω) to which it is connected. In practice, resistance values are about 50 Ω, so the current amplitude can be reduced by about 3 dB. This solution needs more components and should be used only when the distortion resulting from line reflections must be reduced at the same time.

Care should be taken to make the antennas as ineffective as possible, i.e., make the areas enclosed by the outward and return lines as small as possible. An effective method is to run the return line parallel to the signal line (see Figure 10). (This is automatically ensured with multilayer circuit boards that have a continuous ground level under the signal lines.) If signals with high frequencies (such as clock signals) are transmitted or lines are very long, this method will often be used. In this case, lines having defined line impedances (be cautious of reflections) as a result will also be provided. With an appropriate layout of the additional ground lines, crosstalk between critical lines can be reduced.

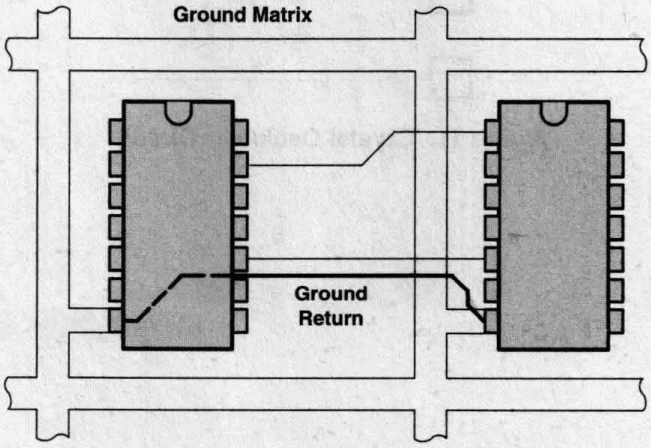


Figure 10. Layout of Signal and Ground Lines

The most cost-effective and technically-effective method consists simply of keeping the critical lines as short as possible, while observing the following priorities:

1. Clock lines
2. Low-order address lines between processor and memory
3. Data lines between processor and memory

All ICs between which information at high frequencies is exchanged should be mounted as close to one another as possible to keep the line lengths short. This applies particularly to lines between a microprocessor and its memory.

The next step is to keep the areas of the antennas as small as possible, i.e., to provide the transmitted signals with a return path which, in turn, is as close as possible to the corresponding signal line. To reduce the effect of tangled lines on circuit boards for fast digital circuits, a ground connection of the circuit board in the form of a network is effective, but the mesh area should be only a few square centimeters. In this way, the inductance of the connections to ground and their lengths can be optimized. This technique results in short return lines and in small-area antennas. With a logical reduction of the mesh area, a final arrangement conforms electrically to that of a continuous ground layer in a multilayer circuit board. Ground lines with a spacing of 2 cm to 4 cm horizontally and vertically make up the required network structure. Subsequently, all free areas can be filled out with copper, which then must be connected by the shortest possible path to ground potential. With large areas, it is advisable to make the contacts at several of the ends. With the positive supply line connected firmly to the supply-voltage connections via the blocking capacitors to the ground system, a network structure connection is not needed.

Oscillator

The highest frequencies in digital systems are usually found in the clock generator. From this point, the oscillator signal is transmitted to the other subsystems, mostly in the form of a divided frequency. It is customary for the oscillator amplifier to be integrated into the microcomputer or processors so that only passive components, such as the crystal and necessary capacitors, need to be connected externally (see Figure 11).

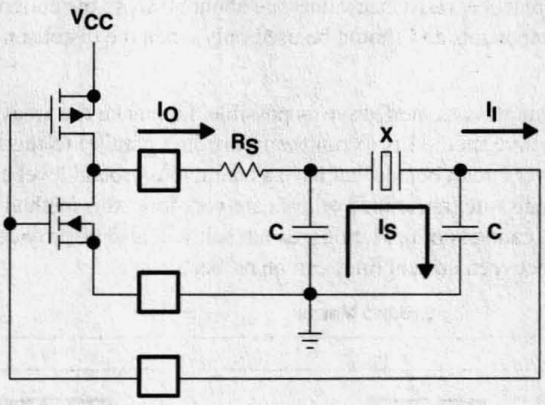


Figure 11. Crystal Oscillator Circuit

The crystal-oscillator circuit needs to be analyzed with respect to the flow of significant currents to determine where interference suppression is necessary. A parallel resonant circuit is formed by the delta section, consisting of the crystal (X) and the two capacitors (C). The crystal behaves like an inductance, with the resonant frequency being somewhat above the actual resonant frequency of the crystal. The impedance of the delta section, measured at the input or output, typically amounts to several tens of kilohms because of the high Q of the crystal. When components are correctly dimensioned, a very small current (I_O) flows between the amplifier and the external components because of the high resistance of the circuit. However, there is an opposite effect as a result of the MOS circuits not having output impedances that are ideally matched to the crystal; they should also be several kilohms. In addition, these circuits usually supply a square-wave signal containing harmonics, to which the delta section no longer represents a high resistance. The result is correspondingly high output currents in the amplifier. An improvement usually can be achieved by a resistor (R_S) in series with the amplifier output (see Figure 11). Ideally, the voltage waveform at the input of the resonant circuit will then be a sine wave. The output is correctly terminated by the high input impedance of the MOS circuit, such that, in this case, only a very small current (I_I) flows.

Capacitor C (see Figure 11) has an impedance of only a few hundred ohms at the resonant frequency. Consequently, a current (I_S) flows in the resonant circuit that is much higher than the current on the line leading to this part of the circuit. This loop must be regarded as considerably more critical; therefore, construction must be compact, with extremely short lines.

Figure 12 suggests how this can be done. The two capacitors (C) of the resonant circuit are placed directly beside the crystal (X). Note that these components should be as close as possible to the corresponding pins of the IC.

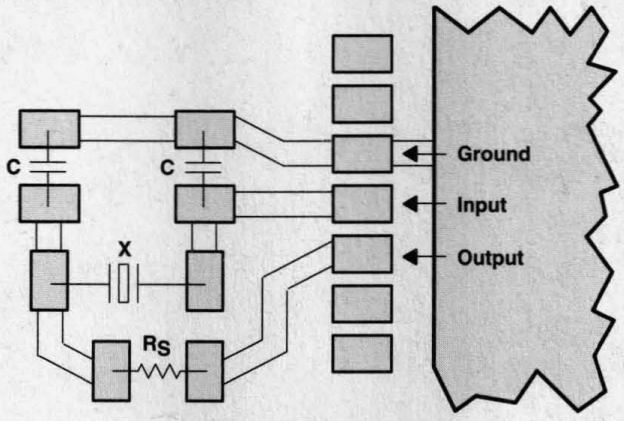


Figure 12. Proposal for the Layout of the Metallization for an Oscillator

The crystal and the capacitors' part of the circuit board, and the radiated interference that results from them, are largely under the control of the development engineer. Nevertheless, it is also necessary that the ground connection needed for the amplifier be made as near as possible to the IC, i.e., beside the amplifier connections, if possible. This ensures that when there are also longer connections in the IC package, unavoidable current loops will enclose only a small area.

Summary

This application report covers several important factors to be considered when designing circuit boards to ensure the EMC of subsystems. The proposals are based on well-understood basic principles and have been successfully implemented to make electronic circuits immune to self-generated interference (e.g., crosstalk) or interference coupled into them from outside sources. Since radiation is simply the opposite of irradiation, the logical further development and application of these rules results in circuits that fulfill the requirements of electromagnetic compatibility.

The implementation of EMC-compatible circuit boards begins when a circuit is first being developed and components are being selected. If wrong decisions are made at this early stage, they often must be corrected later with a considerable expenditure in time and effort, for example, with costly screening. An understanding of circuit operation is absolutely necessary when laying out circuit boards to ensure that appropriate ECM measures are taken. The reduction of the effective areas of the antennas requires, for example, that not only the signal line is taken by the shortest route, but the corresponding return line as well. Perhaps a longer line, but one that is taken parallel to an existing ground or supply line, will be the better solution. Computer-aided layout programs have, until now, been unable to provide useable results with respect to an improvement in EMC. The processes used for these programs do not take electrical requirements into account. This means that the experience of the development engineer is needed to decide how and where every critical connection should be made. The computer can then serve as an *intelligent draftsman*.

Bus-Interface Devices With Output-Damping Resistors or Reduced-Drive Outputs

SCBA012
December 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**1–33**
Output-Damping Resistors	**1–33**
Reduced-Drive Outputs	**1–36**
Practical Applicability of Wave Theory to Predict Signal Waveform Curves	**1–40**
Overview of Technologies and Application Areas	**1–42**
Transceivers With Output-Damping Resistors or Reduced-Drive Outputs	**1–44**
Conclusion	**1–46**
Acknowledgment	**1–46**
References	**1–46**

List of Illustrations

Figure	*Title*	*Page*
1	Line-Impedance Matching	1–33
2	Signal Waveforms Showing Effect of Damping Resistors	1–34
3	Damping-Resistor Implementation	1–35
4	Signal Waveforms With Impedance Mismatch (Z_O = 33 Ω, Z_L = 20 Ω)	1–35
5	Signal Waveforms With Impedance Mismatch (Z_O = 33 Ω, Z_L = 50 Ω)	1–36
6	Implementation of Various Drive Concepts	1–37
7	Line Driven By High-, Balanced-, or Light-Drive Device	1–37
8	Signal Waveforms With High Drive (Z_O = 6 Ω, Z_L = 33 Ω)	1–38
9	Signal Waveforms With Balanced Drive (Z_O = 12.5 Ω, Z_L = 33 Ω)	1–38
10	Signal Waveforms With Light Drive (Z_O = 32 Ω, Z_L = 33 Ω)	1–39
11	Signal Waveforms With Balanced Drive (Z_O = 12.5 Ω, Z_L = 50 Ω)	1–39
12	Signal Waveforms for SN74ABT244 and SN74ABT2244 Driving a SIMM Module	1–41
13	Decision Tree for Selecting Driver Output Type	1–43

Widebus is a trademark of Texas Instruments Incorporated.

List of Tables

Table	*Title*	*Page*
1	Low- and High-Level Output Drive Specifications for Selected TI Logic Devices	1–36
2	Low- and High-Level Output Drive Specifications for FCT16xxx Logic Devices	1–37
3	Advanced 5-V Buffers With Damping Resistor or Reduced-Drive Options	1–42
4	Advanced 3.3-V Buffers With Damping Resistor or Reduced-Drive Options	1–42
5	Advanced Transceivers With High-Drive Outputs on Both Ports (Type 1)	1–44
6	Advanced Transceivers With High-Drive Outputs on One Port and Damping-Resistor Outputs on the Other Port (Type 2)	1–44
7	Advanced Transceivers With Balanced-Drive Outputs on One Port and Damping-Resistor Outputs on the Other Port (Type 3)	1–44
8	Advanced Transceivers With Balanced-Drive Outputs on Both Ports (Type 4)	1–45
9	Advanced Transceivers With Damping-Resistor Outputs on Both Ports (Type 5)	1–45
10	Advanced Transceivers With Light-Drive Outputs on Both Ports (Type 6)	1–45
11	Advanced Transceivers With Reduced-, Unbalanced-Drive Outputs on Both Ports (Type 7)	1–45

Introduction

The spectrum of bus-interface devices with damping resistors or balanced/light output drive currently offered by various logic vendors is confusing at best. Inconsistencies in naming conventions and methods used for implementation make it difficult to identify the best solution for a given application. This report attempts to clarify the issue through looking at several vendors' approaches and discussing the differences.

Output-Damping Resistors

The idea of integrating output-damping resistors in line buffers and drivers is to suppress signal undershoots and overshoots on the transmission line through what is usually referred to as line-impedance matching (see Figure 1). The effective output impedance of the line driver (Z_O) is matched with the line impedance (Z_L). Thus, no signal reflection occurs at the line start ($Z_O = Z_L$; reflection coefficient at point A is 0). The input impedance of the receiving device (Z_I) is assumed to be several orders of magnitude higher than the line impedance. This is valid for CMOS and BiCMOS devices. In this case, the reflection coefficient at point B is approximately 1, such that almost all of the wave energy is reflected at the end of the line.

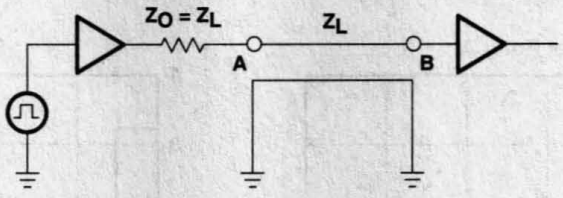


Figure 1. Line-Impedance Matching

Figure 2 illustrates the signal waveforms for a high-to-low transition for a line driver without and with output-damping resistors under these conditions. T is the line signal transmission time, i.e., the time it takes for the signal wave to travel from point A to point B or vice versa. The high-level signal prior to the output transition of the line driver has a level of about 3.3 V, typical for 5-V TTL-level devices, such as ABT or FCT-T, as well as all 3.3-V logic devices. The line impedance is assumed to be 33 Ω.

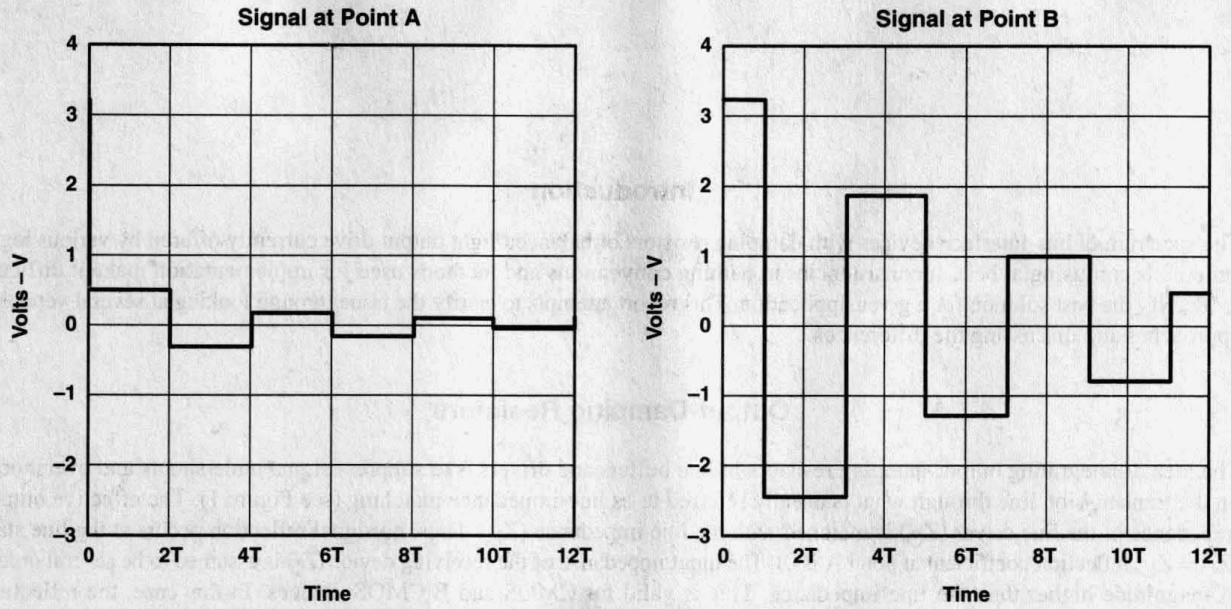
Without the damping resistor (see Figure 2a), a driver output impedance of 5 Ω is assumed. The incident wave at point A and t = 0 establishes a signal level of:

$$V_A = 3.3\ V \times \frac{1 - 33\ W}{5\ W + 33\ W} = 0.43\ V \quad (1)$$

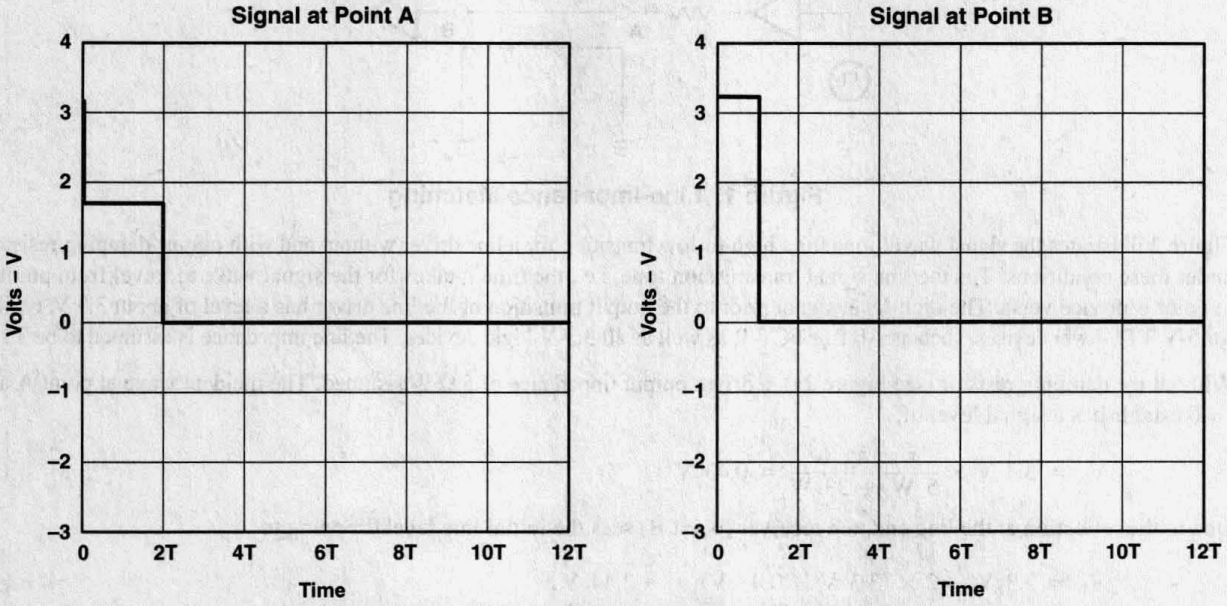
Due to the reflection at the line end, the receiver (point B) sees the initial line level dropping to

$$V_B = 3.3\ V - 2 \times (3.3\ V - 0.43\ V) = -2.44\ V \quad (2)$$

which represents a considerable undershoot. With a damping resistor, the effective output impedance is assumed to be 33 Ω, thus matching the line impedance. In this case, while there is a step in the signal at the driver output (point A), the receiver side (point B) sees a very clean signal transition without any significant undershoot or overshoot. Signal waveforms are analogous to this for a low-to-high transition, in which case the line without damping resistors shows significant signal overshoot.



a) SIGNAL WAVEFORMS WITHOUT DAMPING RESISTOR (Z_O = 5 Ω)

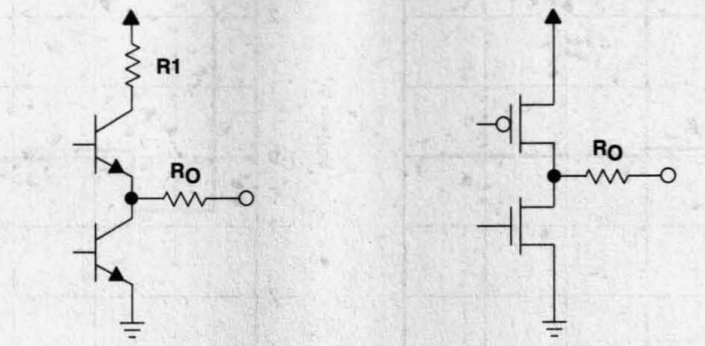


b) SIGNAL WAVEFORMS WITH DAMPING RESISTOR (Z_O = Z_L = 33 Ω)

Figure 2. Signal Waveforms Showing Effect of Damping Resistors

The damping-resistor solution is particularly important when designing memory arrays because excessive undershoots and overshoots may cause data loss in memory devices. Although line-impedance matching is optimized for point-to-point transmission where it helps establish near-perfect signal waveforms, it also works fine in most memory array configurations where there is one driver and many receiving modules. Some of the modules may see a step in the signal waveform (see Figure 2b), but this is only for a short period of time (typically less than 1 ns) and does not affect data transmission. The goal to prevent excessive undershoots and overshoots is still fully accomplished.

Texas Instruments (TI), Philips, and a number of other manufacturers implement output-damping-resistor options in several logic families. The device nomenclature used by all these vendors is a "2" added in front of the device number, that is, the damping-resistor version of the popular '244 octal buffer is referred to as a '2244. Having been the first to introduce a '2244 function with the SN74ALS2244 in the mid-1980s, TI quickly expanded its spectrum of devices with output-damping resistors. Today, it covers the ALS, F, BCT, ABT, LVT, LVC, and ALVC product lines as well as other specialized bus-interface devices.



a) BIPOLAR OR BiCMOS OUTPUT WITH DAMPING RESISTOR (e.g., ABT2xxx, LVT2xxx)

b) CMOS OUTPUT WITH DAMPING RESISTOR (e.g., LVC2xxx, ALVC162xxx)

Figure 3. Damping-Resistor Implementation

Figure 3 shows simplified output diagrams that illustrate how damping-resistor outputs are implemented in the ABT/LVT and LVC/ALVC families, respectively.[2,3] The value of the output-damping resistor (R_O) is typically about 25 Ω. The resistor value in the upper output stage of the bipolar/BiCMOS output, R1, is only a few ohms. Together with the impedance of the output stage itself, this leads to an effective total output impedance of about 33 Ω for all of these circuits. Because line impedance in memory systems is usually around 20 Ω to 50 Ω and some level of impedance mismatch is acceptable, this output impedance value covers almost all practical uses. A good rule of thumb is that a mismatch up to a factor of two will not change signal characteristics much. Figures 4 and 5 show the signal condition for an output-damping-resistor device with a 33-Ω output impedance and line impedance of 20 Ω and 50 Ω, respectively. Signal distortion is still acceptable in both cases.

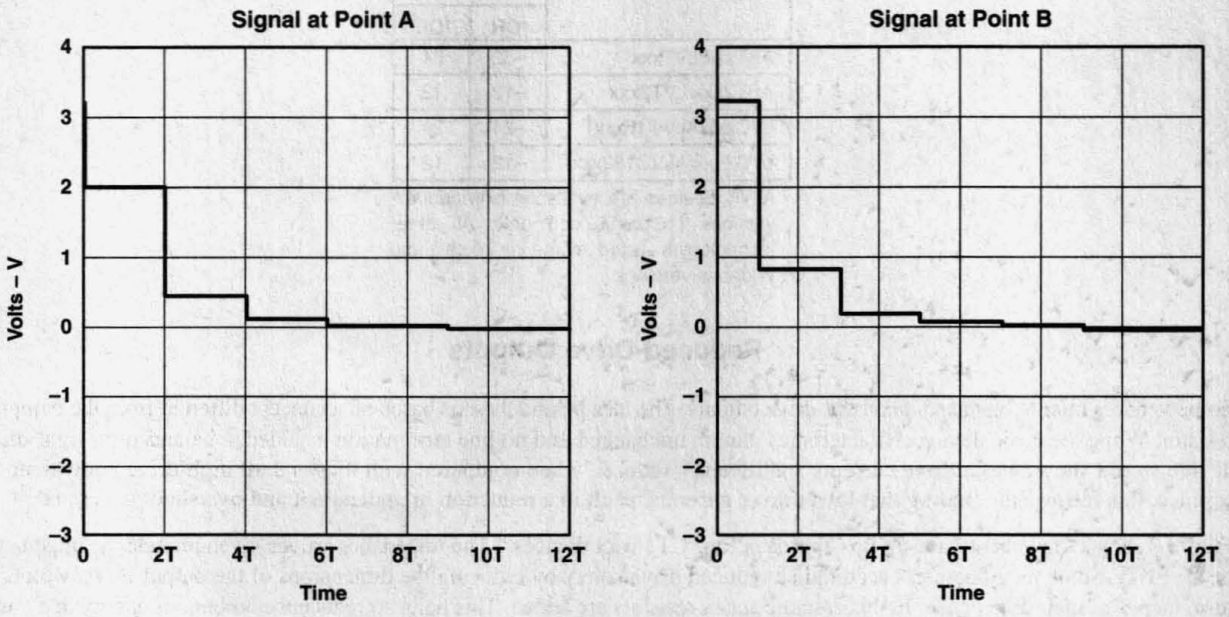


Figure 4. Signal Waveforms With Impedance Mismatch (Z_O = 33 Ω, Z_L = 20 Ω)

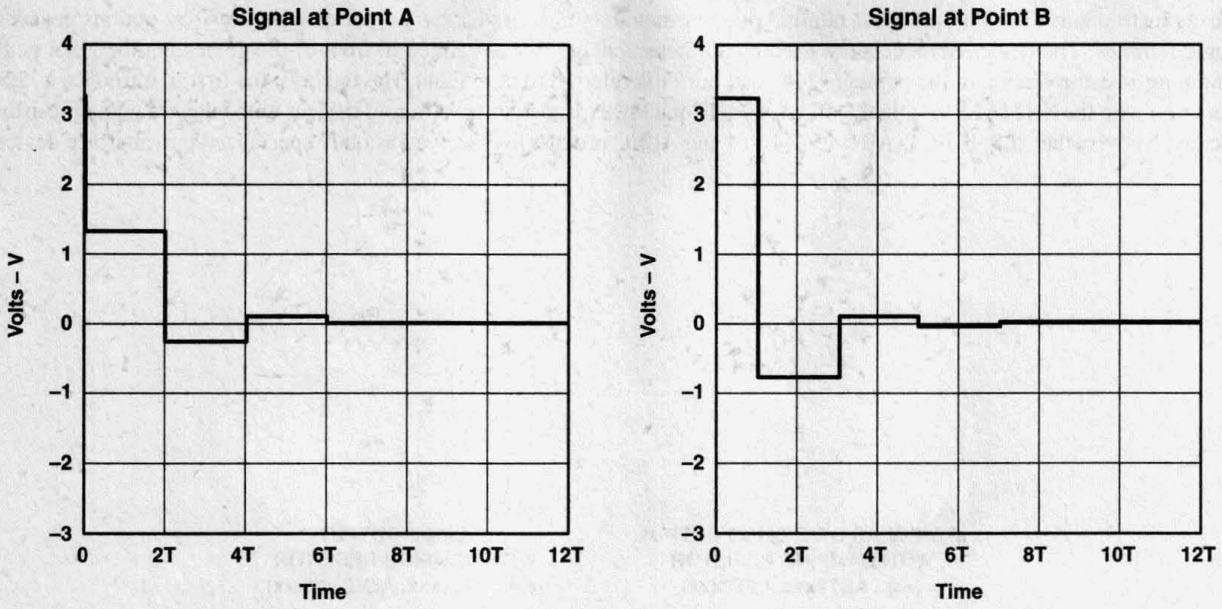


Figure 5. Signal Waveforms With Impedance Mismatch (Z_O = 33 Ω, Z_L = 50 Ω)

The output stage dimensioning of devices with damping resistors usually remains unchanged. The introduction of the damping resistor reduces the nominal output drive currents, but still leaves a drive capability sufficient for most applications. Table 1 shows low- and high-level output drive specifications for the families mentioned above. Note that I_{OH} and I_{OL} are balanced on all '2xxx devices.

Table 1. Low- and High-Level Output Drive Specifications for Selected TI Logic Devices

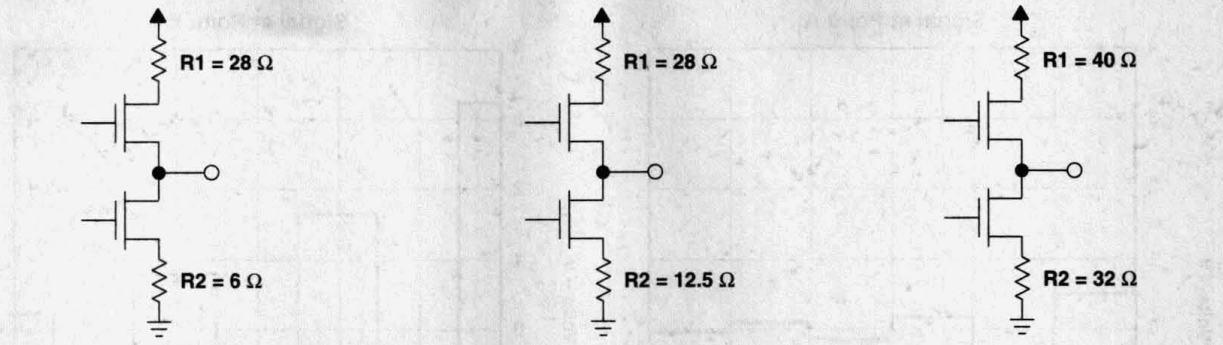
TECHNOLOGY	OUTPUT CURRENT (mA)	
	I_{OH}	I_{OL}
ABTxxx/LVTxxx	–32	64
ABT2xxx/LVT2xxx	–12	12
LVCxxx/ALVC16xxx†	–24	24
LVC2xxx/ALVC162xxx†	–12	12

† ALVC devices are available in Widebus™ versions (16xxx/162xxx) only. All other technologies listed come in octal and Widebus versions.

Reduced-Drive Outputs

Some vendors refer to balanced- and light-drive outputs. The idea behind these is based on a concept different from the damping resistor. While the basic device characteristics remain unchanged and no line termination is added, a balanced- or light-drive device would show output drive currents significantly reduced when compared with its standard high-drive equivalent. In essence, this follows the finding that lower drive currents result in a reduction in undershoot and overshoot generated.

Figure 6 shows implementations of this approach for FCT16xxx devices.[4] The impedance values given include the impedance of the FETs. Some manufacturers accomplish reduced drive solely by reducing the dimensions of the output FETs, which, in turn, increases their impedance. In this case, no series resistors are added. This helps to reduce the amount of energy that could cause undershoots and overshoots, but does not necessarily establish true line-impedance matching because output impedance may remain too low (for example, lower output path in Figure 6b).



a) HIGH-DRIVE FCT16xxx OUTPUT b) BALANCED-DRIVE FCT162xxx OUTPUT c) LIGHT-DRIVE FCT166xxx OUTPUT

Figure 6. Implementation of Various Drive Concepts

Table 2 shows the resulting nominal output drive specifications.

Table 2. Low- and High-Level Output Drive Specifications for FCT16xxx Logic Devices

DRIVE TYPE		OUTPUT CURRENT (mA)	
		I_{OH}	I_{OL}
FCT16xxx	High drive	–32	64
FCT162xxx	Balanced drive	–24	24
FCT166xxx	Light drive	–8	8

Based on a line with Z_L = 33 Ω (see Figure 7) showing a high-to-low signal transition, Figures 8 through 10 illustrate the effect on signal undershoot and overshoot. As illustrated in Figure 6, the output impedance of the driver, Z_O, is 6 Ω, 12.5 Ω, or 32 Ω, for high-, balanced-, and light-drive outputs, respectively.

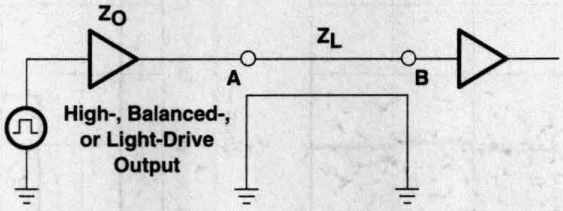


Figure 7. Line Driven By High-, Balanced-, or Light-Drive Device

As would be expected, the high-drive version (see Figure 8) exhibits signal characteristics very similar to those shown for a standard bus driver without an output-damping resistor (see Figure 2a).

Similarly, signal waveforms with the light-drive version (see Figure 10) resemble those of a bus driver with an output-damping resistor (see Figure 2b). The low nominal output drive of ±8 mA limits the applicability of these devices to systems where the output drives one or a few receivers only.

While not quite as severe as the high-drive version, the balanced-drive device (see Figure 9) still causes considerable undershoots because its low-level output impedance of 12.5 Ω is too low to match the line impedance. Matters get worse if line impedance is higher than 33 Ω. Figure 11 demonstrates this, assuming a line impedance of 50 Ω.

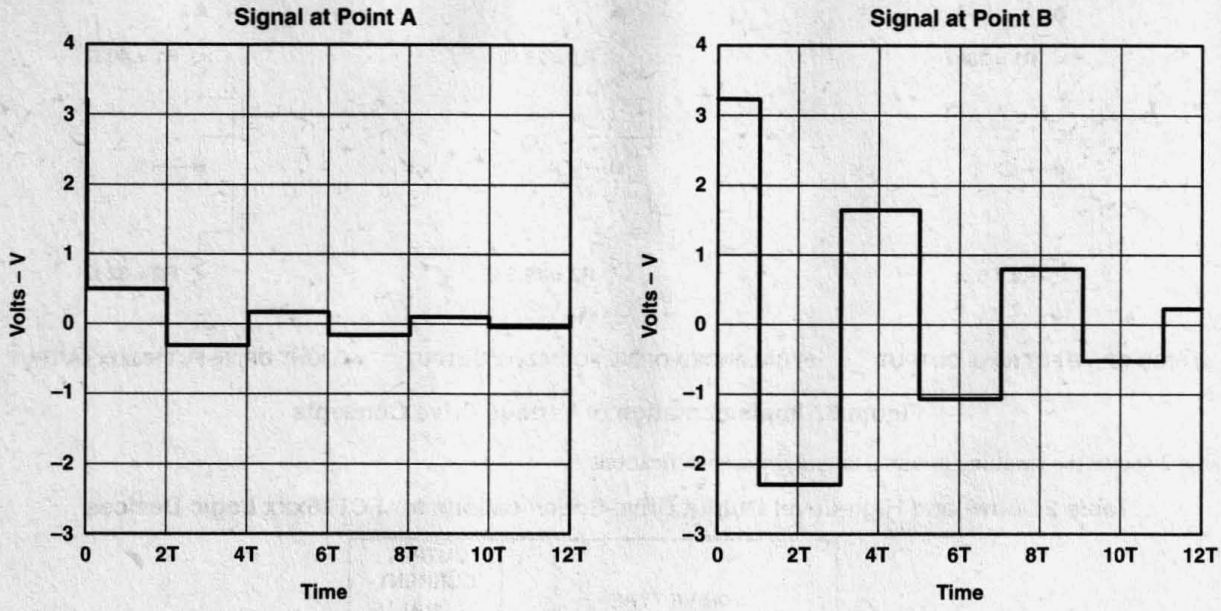


Figure 8. Signal Waveforms With High Drive (Z_O = 6 Ω, Z_L = 33 Ω)

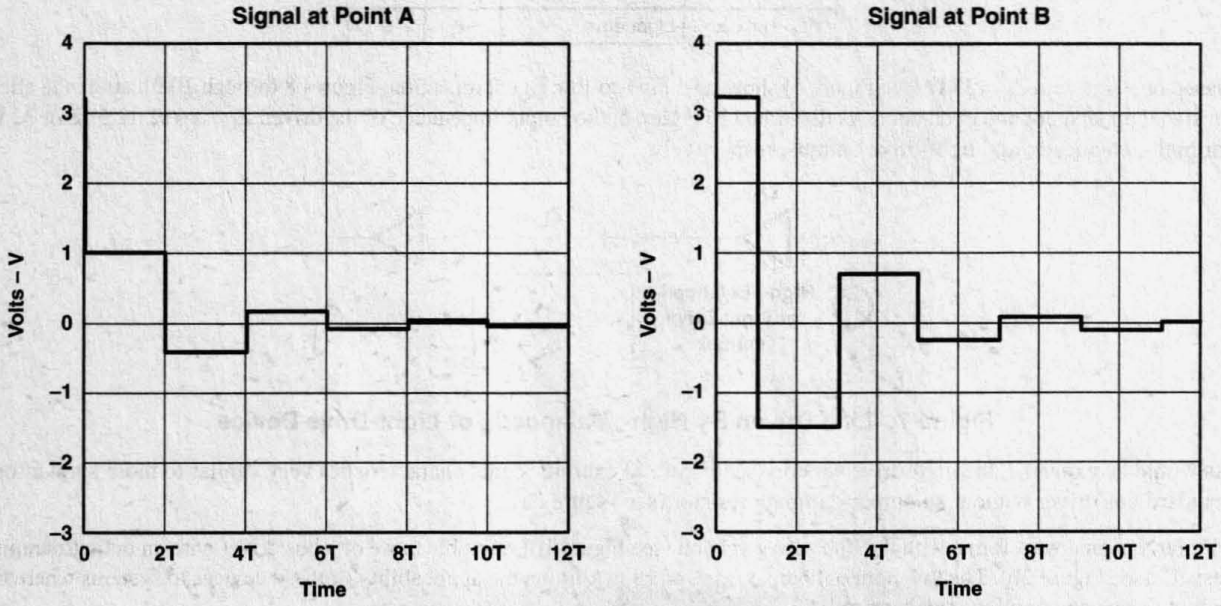


Figure 9. Signal Waveforms With Balanced Drive (Z_O = 12.5 Ω, Z_L = 33 Ω)

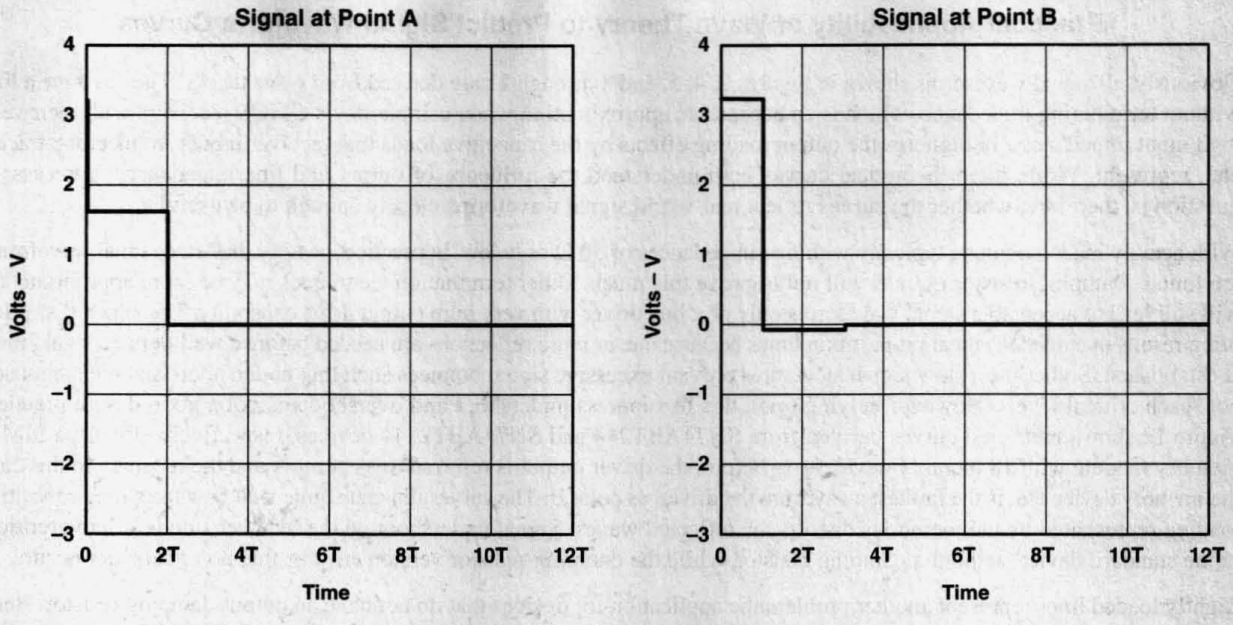


Figure 10. Signal Waveforms With Light Drive (Z_O = 32 Ω, Z_L = 33 Ω)

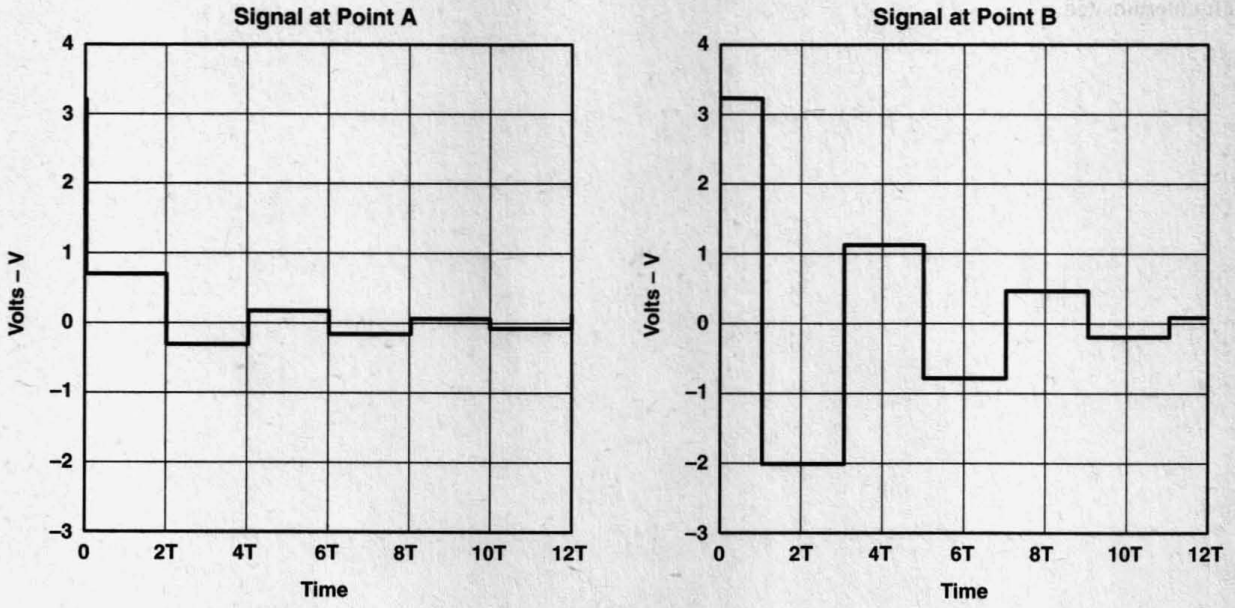


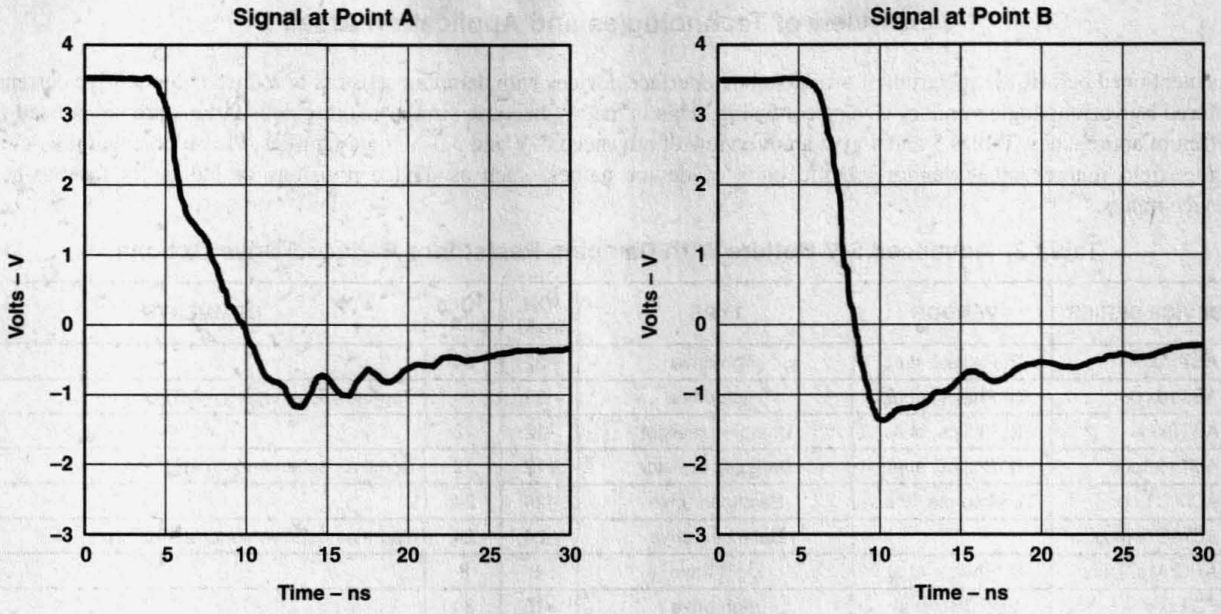
Figure 11. Signal Waveforms With Balanced Drive (Z_O = 12.5 Ω, Z_L = 50 Ω)

Practical Applicability of Wave Theory to Predict Signal Waveform Curves

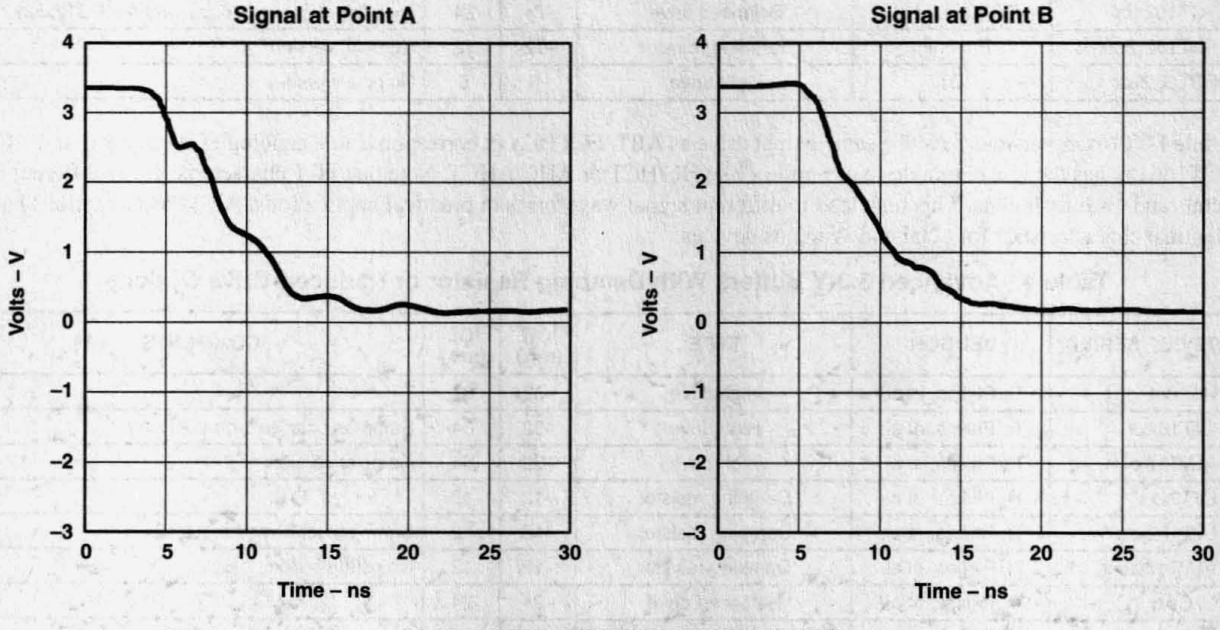
Obviously, all signal waveforms shown in Figures 2, 4, 5, and 8 through 11 are derived from wave theory. They assume a line without terminating impedance, which is an acceptable approximation when using today's CMOS receivers with their very high input impedances, but ignores the output loading effects by the capacitive loads that receiver inputs, connectors, traces, etc., represent. While these theoretical curves help understand the influence of output and line impedances, a necessary question is, therefore, whether the curves reflect real-world signal waveforms closely enough to be useful.

With heavily loaded outputs, typically with line impedances of 30 Ω or below, in practice, heavily distorted signal waveforms are found. Damping-resistor outputs will not improve this much. Other termination techniques may be more appropriate but will still lead to acceptable signal waveforms only of a line driver with very high output drive capability. The signal distortion often results in extended signal propagation times because one or more reflections are needed before a well-defined signal level is established. Sometimes, slow signal slew rates prevent excessive signal bounces such that undershoots and overshoots do not reach critical levels. However, relying upon this to suppress undershoot and overshoots is not a good design practice. Figure 12 shows measured curves derived from SN74ABT244 and SN74ABT2244 devices, respectively, driving a SIMM memory module with 18 memory devices. As before, the driver output is referred to as point A and the receiver, in this case the memory device that is the farthest away from the driver, as point B. The curves illustrate quite well how the strong capacitive loading represented by the memories distorts the reflected waves. Signal undershoot on the receiver side is still overcritical in the standard device without a damping resistor, while the damping-resistor version ensures that no undershoot occurs.

Lightly loaded lines represent another problematic application for devices that do not have an output-damping resistor. Here, the aforementioned slew-rate reduction cannot be expected to improve things more than only marginally. Therefore, with line impedances of 50 Ω or more, that is, in applications where there are only a few receiving devices connected to the line, in practice, waveforms usually are very similar to theoretical ones. Large undershoots and overshoots occur if the line is left unterminated.



a) SN74ABT244 (WITHOUT DAMPING RESISTOR)



b) SN74ABT2244 (WITH DAMPING RESISTOR)

Figure 12. Signal Waveforms for SN74ABT244 and SN74ABT2244 Driving a SIMM Module

Overview of Technologies and Application Areas

As mentioned before, the spectrum of available bus-interface devices with damping resistors or reduced output drive currently offered by various logic vendors is very confusing. This is mainly because similar naming conventions are being used for different approaches. Tables 3 and 4 give an overview of advanced 5-V and 3.3-V logic families. Please note that the device series field ignores other vendor-specific parts of device names, such as device revisions or indicators for bus-hold device inputs.

Table 3. Advanced 5-V Buffers With Damping Resistor or Reduced-Drive Options

DEVICE SERIES	VENDOR	TYPE	I_{OH} (mA)	I_{OL} (mA)	COMMENTS
ABTxxx	TI, Philips, et al.	High drive	–32	64	
ABT16xxx	TI, Philips, et al.	High drive	–32	64	Same as octal version (ABTxxx)
ABT2xxx	TI, Philips, et al.	Damping resistor	–12	12	
ABT162xxx	TI, Philips, et al.	Damping resistor	–12	12	Same as octal version (ABT2xxx)
AC/ACTxxx	TI, Motorola, et al.	Balanced drive	–24	24	
AC/ACT16xxx	TI	Balanced drive	–24	24	Same as octal version (AC/ACTxxx)
AHC/AHCTxxx	TI, Philips, et al.	Light drive	–8	8	
FCTxxx	IDT, QSI, et al.	High drive	–15	64	
FCT16xxx	IDT, QSI, et al.	High drive	–32	64	I_{OH} differs from octal version (FCTxxx)
FCT2xxx	IDT, QSI, et al.	Balanced drive	–15	12	
FCT162xxx	IDT, QSI, et al.	Balanced drive	–24	24	I_{OH}, I_{OL} differ from octal version (FCT2xxx)
FCT162Qxxx	Pericom	Damping resistor	–12	12	No octal version
FCT166xxx	IDT	Light drive	–8	8	No octal version

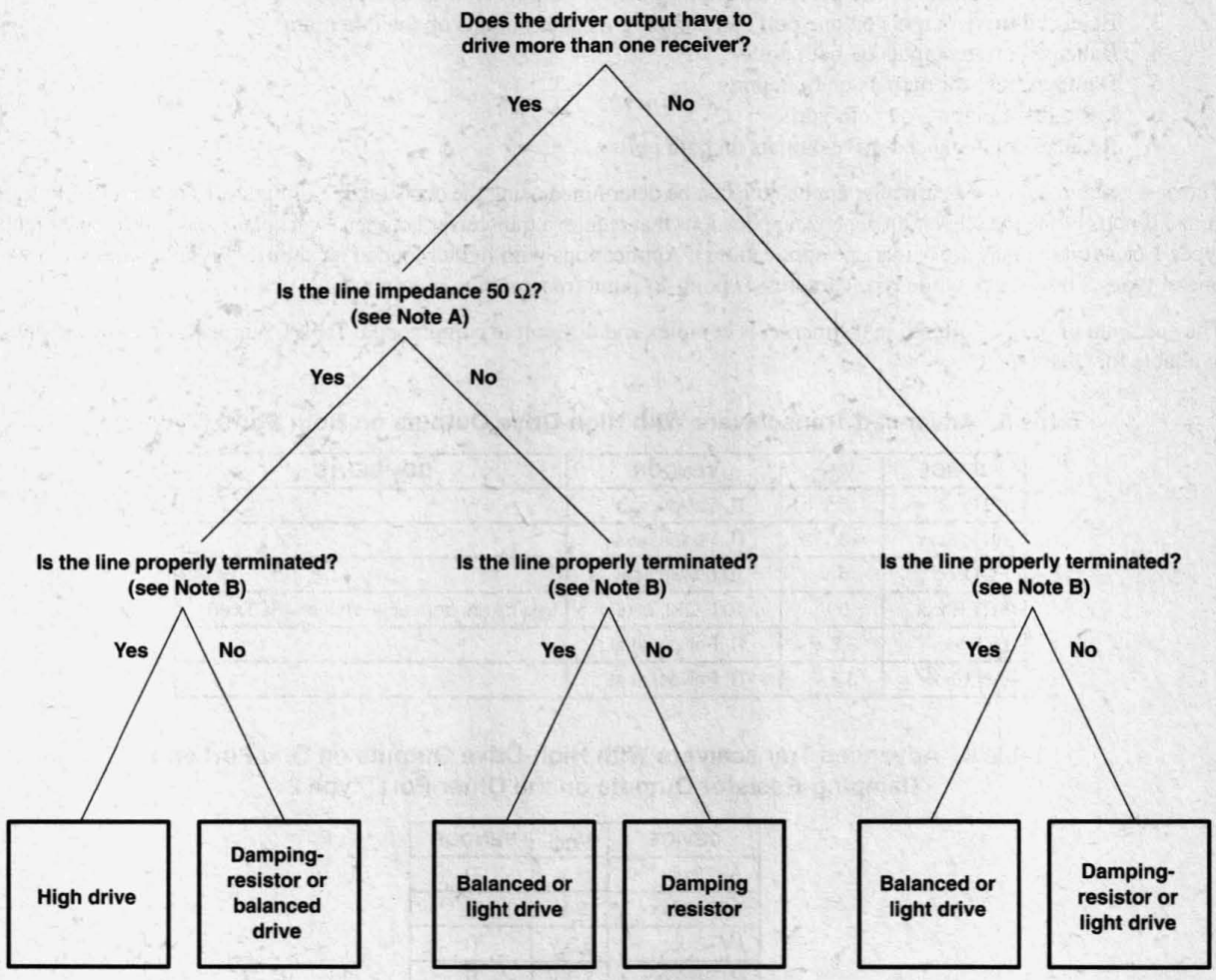
While FCT16xxx versions have the same output drive as ABT, FCT162xxx corresponds to technologies such as AC and ACT. FCT166xxx has the low output drive of families like HC/HCT or AHC/AHCT. Note that FCT characteristics are different for octals and 16-bit versions. This may lead to different signal waveforms in practical applications. All TI logic families have identical characteristics for octal and Widebus devices.

Table 4. Advanced 3.3-V Buffers With Damping Resistor or Reduced-Drive Options

DEVICE SERIES	VENDOR	TYPE	I_{OH} (mA)	I_{OL} (mA)	COMMENTS
LVTxxx	TI, Philips, et al.	High drive	–32	64	
LVT16xxx	TI, Philips, et al.	High drive	–32	64	Same as octal version (LVTxxx)
ALVT16xxx	TI, Philips, et al.	High drive	–32	64	No octal version
LVT2xxx	TI, Philips, et al.	Damping resistor	–12	12	
LVT162xxx	TI, Philips, et al.	Damping resistor	–12	12	Same as octal version (LVT2xxx)
ALVT162xxx	TI, Philips, et al.	Damping resistor	–12	12	No octal version
LVCxxx	TI, Philips, et al.	Balanced drive	–24	24	
LVC16xxx	TI, Philips, et al.	Balanced drive	–24	24	Same as octal version (LVCxxx)
LVC2xxx	TI	Damping resistor	–12	12	
LVC162xxx	TI	Damping resistor	–12	12	Same as octal version (LVC2xxx)
ALVC16xxx	TI, Philips, et al.	Balanced drive	–24	24	No octal version
ALVC162xxx	TI	Damping resistor	–12	12	No octal version
LVxxx	TI, Philips, et al.	Light drive	–8	8	
LCXxxx	Fairchild, et al.	Balanced drive	–24	24	No reduced-drive versions available
LCX16xxx	Fairchild, et al.	Balanced drive	–24	24	Same as octal version (LCXxxx)
FCT3xxx	IDT, QSI, et al.	Reduced, unbalanced drive	–8	24	No high-drive versions available
FCT163xxx	IDT, QSI, et al.	Reduced, unbalanced drive	–8	24	Same as octal version (FCT3xxx)

LVT and ALVT are the only high-drive 3.3-V logic families available in the market. For 3.3 V, only the LVT, ALVT, LVC, and ALVC product families offer true damping-resistor options. FCT3xxx and FCT163xxx devices have significantly lower drive capability than their 5-V equivalents. Also, their I_{OH}/I_{OL} drive currents are unbalanced, which limits their use in certain applications.

Application areas for damping-resistor and reduced-drive line buffers and transceivers cover many different types of end equipment. In addition to required device function, output loading (line impedance) and available termination are the decisive factors when choosing a device. The decision tree shown in Figure 13 provides a general guideline. However, specific requirements may represent further constraints.



NOTES: A. If exact line impedance is unknown, a good rule of thumb is that line impedance is lower than 50 Ω if more than four or five receiver inputs are connected to the line.

B. Examples of other line-termination methods are a split-resistor (Thevenin) network, an R-C combination, or clamping diodes. A more detailed discussion of advantages and disadvantages of these and other termination methods is found in reference 3.

Figure 13. Decision Tree for Selecting Driver Output Type

Transceivers With Output-Damping Resistors or Reduced-Drive Outputs

So far, this report has dealt with buffers and line drivers only. As has been shown, several different output versions support a wide range of output load configurations.

The number of choices is even larger when looking at transceivers because any combination of output versions can be chosen independently for the A port and B port of the device. Not all possible combinations are being offered in the market, but the list of drive types is fairly long.

1. High-drive outputs on both ports
2. High-drive outputs on one port and damping-resistor outputs on the other port
3. Balanced-drive outputs on one port and damping-resistor outputs on the other port
4. Balanced-drive outputs on both ports
5. Damping-resistor outputs on both ports
6. Light-drive outputs on both ports
7. Reduced-, unbalanced-drive outputs on both ports

The best combination for a particular application can be determined using the decision tree in Figure 13 independently for the A and B ports of the transceiver. In general, applications that require a transceiver between a backplane and a local board require types 1 or 2 (type 3 may work in some applications). Applications with lighter loaded local buses on both sides require any one of types 2 through 5, while type 6 addresses point-to-point transmission requirements.

The spectrum of devices offered in the market is complex and difficult to comprehend. Tables 5 through 11 show the options available for each type.

Table 5. Advanced Transceivers With High-Drive Outputs on Both Ports (Type 1)

DEVICE	V_{CC}	VENDOR	COMMENTS
ABTxxx	5 V	TI, Philips, et al.	
ABT16xxx	5 V	TI, Philips, et al.	
FCTxxx	5 V	IDT, QSI, et al.	
FCT16xxx	5 V	IDT, QSI, et al.	I_{OH} differs from octal version (FCTxxx)
LVTxxx	3.3 V	TI, Philips, et al.	
LVT16xxx	3.3 V	TI, Philips, et al.	

Table 6. Advanced Transceivers With High-Drive Outputs on One Port and Damping-Resistor Outputs on the Other Port (Type 2)

DEVICE	V_{CC}	VENDOR
ABT2xxx	5 V	TI
ABT162xxx	5 V	TI
LVT2xxx	3.3 V	TI
LVT162xxx	3.3 V	TI
ALVT162xxx	3.3 V	TI

Table 7. Advanced Transceivers With Balanced-Drive Outputs on One Port and Damping-Resistor Outputs on the Other Port (Type 3)

DEVICE	V_{CC}	VENDOR
LVC2xxx	3.3 V	TI
LVC162xxx	3.3 V	TI
ALVC162xxx	3.3 V	TI

Table 8. Advanced Transceivers With Balanced-Drive Outputs on Both Ports (Type 4)

DEVICE	V_{CC}	VENDOR	COMMENTS
AC/ACTxxx	5 V	TI, Motorola, et al.	
AC/ACT16xxx	5 V	TI	
FCT2xxx	5 V	IDT, QSI, et al.	
FCT162xxx	5 V	IDT, QSI, et al.	I_{OH}, I_{OL} differ from octal version (FCT2xxx)
LVCxxx	3.3 V	TI, Philips, et al.	
LVC16xxx	3.3 V	TI, Philips, et al.	
ALVC16xxx	3.3 V	TI, Philips, et al.	
LCXxxx	3.3 V	Fairchild, et al.	
LCX16xxx	3.3 V	Fairchild, et al.	

Table 9. Advanced Transceivers With Damping-Resistor Outputs on Both Ports (Type 5)

DEVICE	V_{CC}	VENDOR	COMMENTS
ABTRxxx	5 V	TI	Same nomenclature, but different type from TI ABT162xxx
ABT162xxx	5 V	Philips	
FCT162Qxxx	5 V	Pericom	
LVCR2xxx	3.3 V	TI	
LVCR162xxx	3.3 V	TI	
ALVCR162xxx	3.3 V	TI	
ALVC162xxx	3.3 V	Philips	Same nomenclature, but different type from TI ALVC162xxx
LVT162xxx	3.3 V	Philips	Same nomenclature, but different type from TI LVT162xxx
ALVT162xxx	3.3 V	Philips	Same nomenclature, but different type from TI ALVT162xxx

Table 10. Advanced Transceivers With Light-Drive Outputs on Both Ports (Type 6)

DEVICE	V_{CC}	VENDOR
AHC/AHCTxxx	5 V	TI, Philips, et al.
FCT166xxx	5 V	IDT
LVxxx	3.3 V	TI, Philips, et al.

Table 11. Advanced Transceivers With Reduced-, Unbalanced-Drive Outputs on Both Ports (Type 7)

DEVICE	V_{CC}	VENDOR	COMMENTS
FCT3xxx	3.3 V	IDT, QSI, et al.	
FCT163xxx	3.3 V	IDT, QSI, et al.	I_{OH}, I_{OL} differ from octal version (FCT3xxx)

The majority of solutions offered are symmetrical, that is, they use the same output type on the A port and on the B port. While this may appear logical, it does not address the needs of most backplane-based applications where the backplane usually requires a high-drive output. TI was the first to introduce a transceiver with output-damping resistors, the SN74BCT2245, and ever since has used the AAA2xxx or AAA162xxx concept (AAA = family indicator, xxx = device number) to indicate a device with standard (high or balanced) drive on one side and damping-resistor outputs on the other side. Others, including Philips, use the same nomenclature to indicate both output sides having damping resistors. TI uses AAAR2xxx or AAAR162xxx for this arrangement.

Conclusion

While buffers or transceivers with integrated output-damping resistors or reduced-drive outputs are required by many applications, the system designer needs to carefully choose a solution because vendors' denomination methods for these devices may be confusing. In particular, the difference between true damping resistors, i.e., integrated series resistors in the output path, and reduced-drive outputs, where the output drive is limited through changing the dimensioning and/or adding a resistor to the upper and lower transistor of the output stage, needs to be understood relative to different applications.

TI is the only vendor who offers 5-V and 3.3-V versions of all driver output types discussed in this report.

Acknowledgment

The author of this document is Lothar Katz.

References

1 Curtis, Rick; Forstner, Peter; "Memory Driver Application Report", EB 205E, Texas Instruments (www.ti.com/sc/docs/asl/lit/eb205.htm).

2 Texas Instruments, "ABT Enables Optimal System Design", SCBA001 (www.ti.com/sc/docs/psheets/appnote.htm).

3 Texas Instruments, "Proper Termination of Outputs", *LVC Designer's Guide*, SCBA010, page 1–27ff.

4 Hronik, Stanley, "Effective Use of Line Termination in High Speed Logic", Integrated Device Technology, Inc., Conference Paper CP-23 (www.idt.com/cgi–bin/dsq.pl?mkgkey=logicgen).

5 Texas Instruments, SN74ABTxxx, SN74LVCxxx, SN74ALVCxxx, and SN74LVTxxx data sheets (www.sc.ti.com/sc/docs/psheets/pids2.htm).

6 Integrated Device Technology, IDT54/74FCTxxx data sheets (www.idt.com/logic/Welcome.html).

7 Pericom, PI74FCTxxx data sheets (www.pericom.com/products/sinter).

8 Philips Semiconductors, 74ABTxxx, 74LVCxxx, 74ALVCxxx, and 74ALVTxxx data sheets (www.semiconductors.philips.com/philips54.html#3).

Designing With Logic

SDYA009B
March 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title *Page*

Abstract **1–51**

1 Introduction **1–51**

2 Behavior With the Supply Voltage Reduced **1–51**
2.1 Behavior With the Supply Voltage Switched Off 1–51
2.1.1 Bipolar Circuits 1–51
2.1.2 CMOS Circuits 1–53
2.2 Behavior With Low Supply Voltages 1–53
2.3 Supply Voltages Partially Switched Off 1–54
2.4 Changing Powered-Up Subsystems 1–56

3 Unused Inputs **1–56**

4 Excessive Input Currents **1–58**

5 Transition Times **1–59**

6 Propagation Delay Times **1–62**
6.1 Propagation Delay Times With Several Outputs Switching Simultaneously 1–62
6.2 Propagation Delay Times With Negative Undershooting at the Outputs 1–64
6.3 Propagation Delay Times With Large Capacitive Loads 1–65
6.4 Input and Output Capacitances of Digital Devices 1–68

7 Bus Conflicts **1–69**

8 Backdriving **1–74**

9 Summary **1–77**

Acknowledgment **1–77**

List of Illustrations

Figure *Title* *Page*

1 Input Circuit of a Bipolar IC 1–51
2 IC Output From SN74 Family (Standard TTL) 1–52
3 Output of Schottky TTL ICs 1–52
4 3-State Output of Schottky TTL Devices 1–53
5 Diode Paths in CMOS Devices 1–53
6 Behavior of a TTL Device at Low Supply Voltages 1–54
7 Feeding Back With CMOS Devices 1–55
8 Ideas for Protecting CMOS Devices 1–55
9 Interconnection of Unused Inputs With AND and OR Gates 1–57
10 Fixed Potential Connected to Unused Inputs 1–57
11 Series Resistor Connected to Unused Inputs of Multiple-Emitter Transistors 1–57

Widebus is a trademark of Texas Instruments Incorporated.

List of Illustrations (continued)

Figure	*Title*	*Page*
12	Parasitic Transistors in CMOS Input Stages	1–58
13	Parasitic Transistors in Bipolar Input Circuits	1–59
14	Setup for Generating an Undershoot Pulse (I = –60 mA, t = 100 ns)	1–59
15	Definition of Signal Amplitude and Pulse Width	1–60
16	Two-Stage Shift Register	1–61
17	Incorrect Operation of a Shift Register	1–62
18	Inductances in the Lines Supplying a Package	1–62
19	Increase of the Delay Time When Several Outputs Are Switched Simultaneously	1–63
20	Increase of the Propagation Delay Time With a Widebus™ Circuit (74AC16240)	1–64
21	Currents in the Output Stage of a Bus Driver With Negative Undershoot	1–64
22	Measurement Setup	1–65
23	Waveforms for Various Line Lengths	1–65
24	Bipolar Output Stage With Output Characteristics at a High Level	1–66
25	Waveform at SN74LS00 Output (C_L = 10 pF, 56 pF, and 616 pF)	1–68
26	Determining the Short-Circuit Current With a Bus Conflict	1–69
27	ABT Output-Stage Circuit Diagram	1–70
28	Bus Supervision During Power On	1–74
29	Feeding Test Signals Into a Node Test Point	1–75
30	Low-Logic-Level Output Characteristics of SN74AS645	1–75
31	Thermal Resistances in an IC	1–76
32	Thermal Behavior in an IC	1–76

List of Tables

Table	*Title*	*Page*
1	Required Minimum Input Rise/Fall Rates for Logic Families	1–61
2	Short-Circuit Current and Internal Resistance of Logic Families	1–67
3	Capacitances of Digital Devices	1–69
4	Output-Stage Conditions During a Bus Conflict	1–70
5	Thermal Resistance of Plastic Packages in Still Air	1–72

Abstract

Information in data sheets, which usually give information on device behavior only under recommended operating conditions, may only partially answer engineering questions that arise during the development of systems using integrated circuits (ICs). However, information is frequently needed regarding the behavior of the device outside the conditions in the data sheet. Such questions might be: "How does a bus driver behave with reduced (or even switched-off) supply voltage?" or "How does the delay time of a gate with a large capacitive load change?" or "What must be considered when using so-called *backdriving*?".

This report gives information on a number of questions that frequently arise. In addition, it provides examples that explain phenomena that the designer should be aware of when using ICs outside their recommended operating conditions.

1 Introduction

The function and behavior of digital ICs are described fully in data sheets. Most questions regarding the behavior of the device that arise when developing a system can be answered with the information given. However, the devices might be operated under conditions not covered by the data sheet. This report addresses this issue and provides information on the behavior of ICs under such conditions.

Many parameter values in data sheets are not measured when the circuits are tested. The information is based on typical values that have been established experimentally and that are applicable to the majority of devices of the same type or family. In individual cases it might be necessary to interpret data and make measurements to accurately forecast the behavior of the complete system.

2 Behavior With the Supply Voltage Reduced

Although not specifically mentioned in data sheets, additional components, some of them parasitic, influence operational characteristics of ICs. These components can affect the function of a system if the devices are not operated within the recommended operating conditions. For example, large systems often require that parts of the system be shut down while other parts continue to operate. Frequent problems occur at the interfaces between subsystems, which are operated with different supply voltages, or whose supply voltages are switched off. This section describes the behavior of digital circuits operated with low supply voltages.

2.1 Behavior With the Supply Voltage Switched Off

Because many circuits can be used with the various logic families, no general rule applies to the behavior of systems with supply voltages switched off. For this reason, only the most important circuits and their behavior are discussed.

2.1.1 Bipolar Circuits

Figure 1 shows the simplified circuit of a TTL device with diode inputs, such as used with devices in the SN74LS (Low-Power Schottky TTL) logic family. However, the following comments apply to all other bipolar logic families.

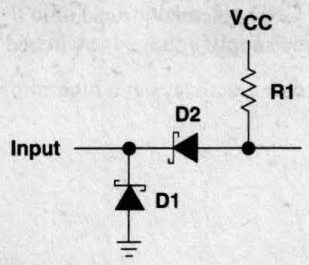


Figure 1. Input Circuit of a Bipolar IC

When the supply voltage in a system is switched off ($V_{CC} = 0$ V), the V_{CC} pin of an IC is short circuited to ground via the other components in the system. If a voltage is then applied to the input of an IC, as shown in Figure 1, and if this voltage lies within the logic-level range ($V_I = 0$ to 5.5 V), diode D2 is blocking and the clamping diode D1 is biased into a blocking state. Therefore, a very small current flows into the IC, corresponding to the leakage current of these diodes. The value for this current given in the data sheets for the corresponding input voltage can be used. This statement applies, without exception, to all TTL devices.

Figure 2 shows the output stage of circuits from the SN74 (Standard TTL) series. Parasitic collector-substrate diode D2 and diode D3 are in a blocking position between the V_{CC} and GND connections of all ICs. If the V_{CC} pin is at GND potential and a positive voltage is applied to the output, diode D1 is blocking and the output is in the high-impedance state.

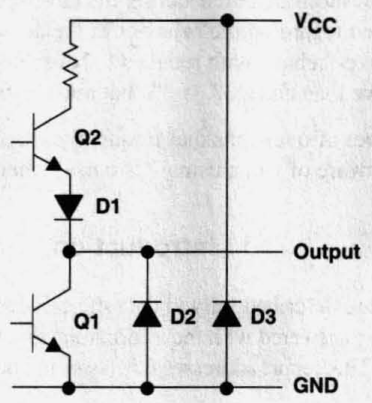


Figure 2. IC Output From SN74 Family (Standard TTL)

Other bias relationships result when supply voltages are switched off to Schottky TTL devices (SN74LS, SN74S, SN74ALS, SN74AS, and SN74F series). Figure 3 shows the important parts of the output stage. If a voltage is applied to the output of the device whose supply voltage is switched off, parasitic diode D1, which is in parallel with resistor R, becomes conductive. The output is then at a low impedance.

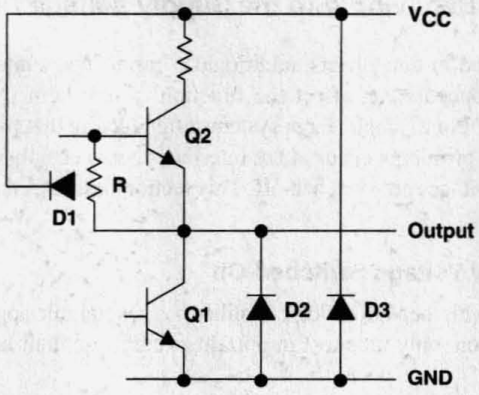


Figure 3. Output of Schottky TTL ICs

If the circuit in Figure 3 is modified for bipolar devices using 3-state outputs, parasitic diode D1 at the output is no longer significant. One possibility is to tie resistor R to GND potential instead of to the output of the circuit (see Figure 4). In this case, the output remains at a high impedance when the supply voltage is switched off.

The outputs of TTL circuits with an open collector are always at a high impedance when the supply voltage is switched off.

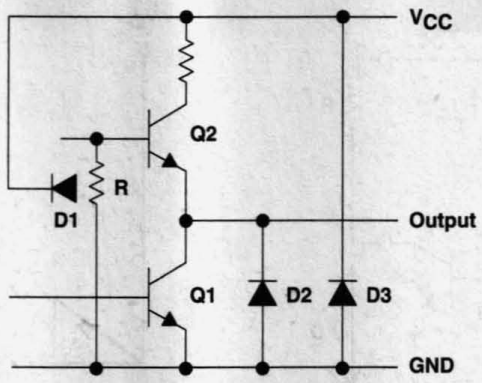


Figure 4. 3-State Output of Schottky TTL Devices

2.1.2 CMOS Circuits

The behavior of CMOS devices when the supply voltage is switched off is essentially determined by the protective circuits at the inputs and outputs. These circuits are intended to protect the device from damage from electrostatic discharge. Figure 5 shows, in simplified form, the construction of a CMOS circuit with additional diode paths at the input and output. Both the input, via diode D1, and the output, via diode D3, are at a low impedance when the supply voltage is switched off. Diode D3 also exists in circuits having an open drain at the output.

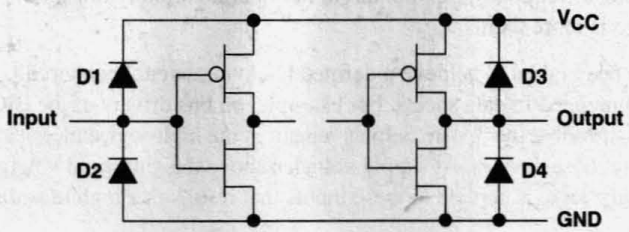


Figure 5. Diode Paths in CMOS Devices

2.2 Behavior With Low Supply Voltages

The behavior of ICs at low supply voltages is difficult to predict because a detailed knowledge of the internal circuit, including its dimensions, is necessary. An example is the behavior of a noninverting buffer with open-collector outputs (SN7407) when the supply voltage is switched on and off. Figure 6 shows the internal circuit of the SN7407. At supply voltages lower than the forward voltage of the diode path (base-emitter path), all transistors are blocking. Therefore, the output voltage (V_O) first follows the supply voltage (V_{CC}). When the latter reaches about 0.7 V, current flows via resistor R3 into the base of transistor Q4 and the output switches to a low level. If the supply voltage reaches a value of $3 \times V_{be}$, and if a logic high is applied to the input, current flows into the base of transistor Q3 (via transistors Q1 and Q2), which switches. Output transistor Q4 is again switched off, causing the output voltage to rise to the value of V_{CC}. In the previous analysis, the voltage drop necessary for a sufficient base current to switch on the transistor is neglected. TTL devices attain stability with a supply voltage of about 3.5 V, and are fully functional at a typical voltage of 4 V. However, with supply voltages below the minimum specified in data sheets, not all parameters can be attained. This applies to both dc parameters, such as output currents and voltages, and to ac parameters, such as propagation delay time and maximum clock frequency.

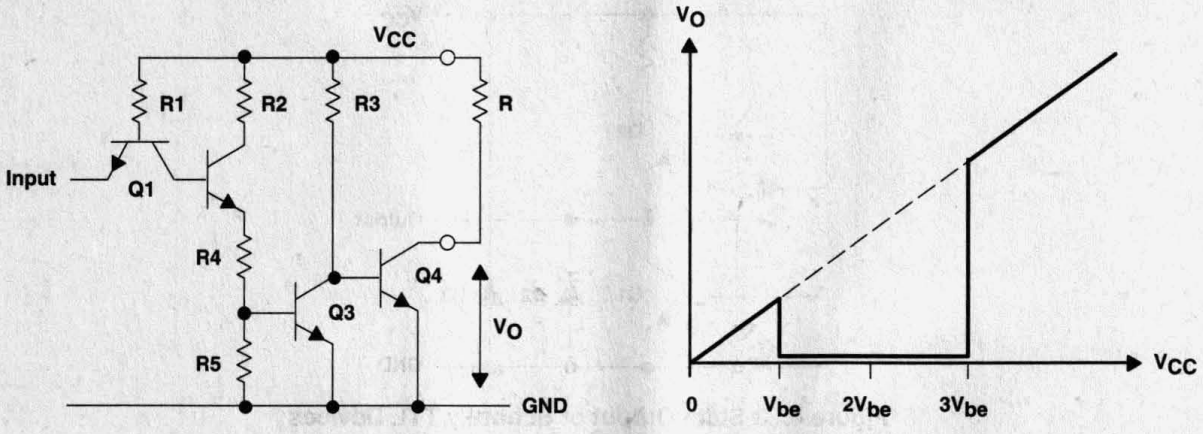


Figure 6. Behavior of a TTL Device at Low Supply Voltages

In a manner similar to TTL devices, CMOS devices also fail to operate at supply voltages below the threshold voltages of the MOS transistors. If the supply voltage is further increased, parts of the circuit are activated (see Figure 6). As previously mentioned, the precise circuit configuration of the device determines the circuit behavior. Full functionality of CMOS devices from the SN74HC family is ensured from V_{CC} = 2 V, whereas the 74AC family can only be ensured from 3 V, although the latter is also stable, with a supply voltage of only 2 V. Since the maximum clock frequency of CMOS devices is dependent on the supply voltage, at a high clock frequency, circuits might not operate reliably during the switch-on or switch-off phases, even though the supply voltage is more than 2 V.

Special design measures have been taken to achieve a defined behavior, even when circuits are operated at supply voltages far below the conditions recommended in data sheets. For example, on bus drivers of the BiCMOS series (SN74ABT/BCT), a voltage-monitoring circuit ensures that the 3-state outputs remain in the high-impedance state at supply voltages below about 3.5 V, regardless of the inputs to these devices. At supply voltages above this threshold voltage, the control inputs (enable and disable) are effective. If a voltage level is applied to these inputs that results in a high impedance at the output, the same state is implemented at the output.

2.3 Supply Voltages Partially Switched Off

In large systems, often part of the voltage supply is switched off, while other parts of the system continue to operate. Then, the critical part of the system is the interface between the device that is supplied and the device that is not supplied with voltage. In such a case, two requirements must be met. First, the part of the system that continues to operate must not be disturbed by the part that is switched off. Second, the switched-off part must not be disturbed by voltages fed back from the operating part.

These requirements can be met with bipolar circuits. As mentioned previously, the inputs of switched-off bipolar circuits are at a high impedance and do not influence parts of the device that are still active. With outputs of switched-off parts of devices that are connected to active parts, only the outputs of bus drivers (e.g., SN74xx240 or SN74xx245) are at a high impedance. Therefore, only such devices should be used for bus lines connecting systems. For unidirectional lines that connect switched-off and active devices, it must be determined in each case whether the operation of the system could be influenced by the outputs being at a low impedance when switched off. If this is not the case, then at this position in the system, any kind of device, including CMOS, can be used.

As mentioned previously, when switching the supply on and off, the logic state of the devices concerned cannot be ensured. Therefore, undefined states can arise during this time at the interfaces and cause malfunction of the system (see Figure 6). The use of SN74ABT/BCT-series bus drivers provides a solution, since the outputs of these parts go into the high-impedance inactive state at supply voltages below about 3.5 V. A difficult situation arises when using CMOS devices. As shown in Figure 5, these parts have protective diodes, that are connected to the supply rails, at both inputs and outputs. If the supply voltage V_{CC2} of this circuit is switched off (see Figure 7) while the supply voltage V_{CC1} remains switched on, a current (I) flows out of gate G1, via diode D1, into the next circuit. This current can rapidly overload protective diode D1 (the maximum current of the input clamp diodes of CMOS devices is only 20 mA) and destroy the device. Remember that, in general, the next device represents a short circuit and, apart from the output resistance of gate G1, there is no current-limiting circuit element.

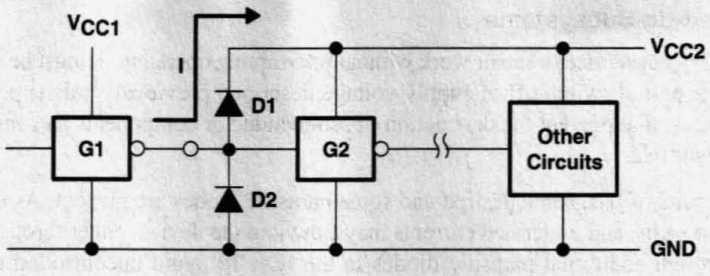


Figure 7. Feeding Back With CMOS Devices

Figure 8 shows recommended design ideas, with reservations, to provide some current limiting. In Figure 8a, the input current of the switched-off device is limited by resistor R. Using this, the input current of the circuit to be protected can be limited to a permissible value. The input current of CMOS devices is extremely low and series resistors of several ohms usually have no negative effect on the function of the part. However, feeding of the next device, via input clamping diode D1, is not prevented entirely.

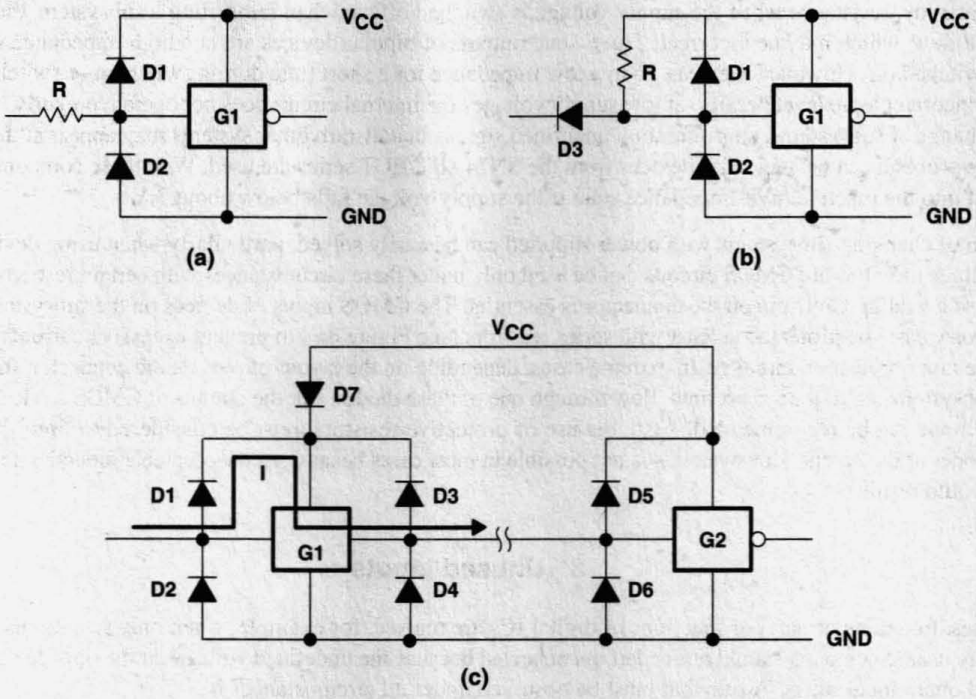


Figure 8. Ideas for Protecting CMOS Devices

In the circuit of Figure 8b, the flow of current into the device to be protected when the supply voltage V_{CC} is switched off, is prevented by diode D3. However, to ensure a high level at the input of gate G1 with normal operation, a pullup resistor is needed, and this significantly increases the power consumption of the CMOS circuit. D3 also shifts the logic level at the input of the gate, and as a result, reduces the noise margin of the circuit. Apart from the noise-margin restriction, this circuit is effective, because it prevents feedback into the switched-off part of the device.

The diode in Figure 8c has no effect if gate G1 has a noninverting function. Even so, the flow of current via clamping diode D1 and the V_{CC} rail of gate G1 into the next circuit is prevented. Instead, the current flows via the output of gate G1, which, in this case, is at a high logic level, and into the following circuit.

2.4 Changing Powered-Up Subsystems

In many applications, to carry out service or repair work without interrupting operation, it must be possible to change individual subsystems. Because of the partial switch off of supply voltage described previously, this is permissible only when circuit design modifications are made that prevent the destruction of semiconductor components and ensure that the operation of the rest of the system is not disturbed.

In the input and output circuits of ICs, some desired and some parasitic diodes are present. As explained, these components represent additional current paths, and undefined currents may flow into the device, either through the clamping diodes to the inputs and outputs, or through additional parasitic diodes in the ICs. To avoid uncontrolled operational states, changing subsystems while powered up is permissible only if the subsystems have a leading GND pin as a reference potential.

If the connection of the GND reference potential is made first when inserting subsystems, and broken only after removing them, the operational state that results when changing subsystems can be limited to the cases previously mentioned. This assumes that parts of the system that have the same reference potential are not supplied with voltage.

The inputs of bipolar logic circuits, including devices in the SN74ABT/BCT series that are in subsystems to be changed, are at a high impedance under all conditions and, therefore, no problems should be expected. The totem-pole outputs of most TTL devices are at a low resistance when the supply voltage is switched off, so when reinserting a subsystem, the line concerned is switched to low, which may be incorrect. Three-state outputs of bipolar devices are at a high impedance when the supply voltage is switched off. However, they can go to a low impedance for a short time during switch on or switch off. This could generate an incorrect logic level because at low supply voltages the internal circuit does not operate properly. The result is that during the change of subsystems, short-duration undefined signals that disturb other systems may appear at the corresponding outputs. This problem can be avoided if devices from the SN74ABT/BCT series are used. With these components, the outputs are switched into the inactive high-impedance state if the supply voltage falls below about 3 V.

The problem of changing subsystems with power supplied can be easily solved, particularly when using devices that include a supply-voltage monitor, but CMOS circuits can be used only under these circumstances with certain restrictions. In this case too, the use of a leading GND pin on the connector is essential. The CMOS inputs of devices on the subsystem to be changed should, in every case, be protected at least with series resistors (see Figure 8a), to prevent excessive currents in the clamping diodes of the input protection circuitry. In extreme cases, depending on the layout of pins on the connector, the current for the complete subsystem could, for a short time, flow through one of these diodes. For the outputs of CMOS devices, no practicable protection circuit can be recommended. Also, the use of protective resistors must be considered to limit the current in the clamping diodes at the output. However, this is not possible in most cases because an unacceptable reduction in the output drive capability would result.

3 Unused Inputs

In many cases, functions or parts of functions of digital ICs are unused, for example, when only two inputs of a triple-input AND gate are used. Such parts should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. A rule that must be observed under all circumstances is:

> At all unused inputs of digital ICs, defined logic levels (low or high) must be applied in every case.

The logic level that should be applied to any particular unused input depends on the function of the device. As a result of the input circuits of bipolar ICs, a high level is established at open-circuited inputs. The voltage at such an input corresponds to the threshold voltage of the input circuit (about 1.4 V or 1.1 V with devices from the SN74LS family). In a test of the function of such a circuit, this order of voltage at the input, in general, indicates that this circuit is open. CMOS inputs are of such high impedance that the smallest change on the open input can generate any undesired logic level. A slight change of the capacitance at the unconnected input, for example, by bringing the hand close to the package, can so change the effective voltage at the input that a high level can change into a low level, or vice versa. Additionally, for the same reasons mentioned, unconnected inputs may react to all kinds of coupled-in interference voltages, and the behavior of the circuit can no longer be predicted.

With gates, the best solution is to connect unused inputs to inputs that are in use. The function of the device is unaffected. This circuit arrangement can be used equally well with AND (NAND) as with OR (NOR) gates (see Figure 9). Here, connecting the inputs together increases the capacitive load on the driver stage and, with bipolar circuits, also increases the dc current drain.

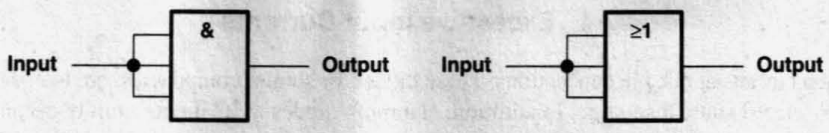


Figure 9. Interconnection of Unused Inputs With AND and OR Gates

In many cases, the simple method shown here cannot be used, especially if the unused inputs are not part of gate functions. In this case, a defined logic level must be applied to the inputs. If a low level is required, the input should be directly connected to GND; if a high level is required, it should be connected with a voltage source corresponding with a high level. In general, this is the positive supply voltage V_{CC}. Figure 10 shows how, in the previously mentioned cases, a fixed potential should be connected to unused inputs. Note that a high level should be applied to the unused inputs of an AND (NAND) function and a low level to unused inputs of an OR (NOR) function.

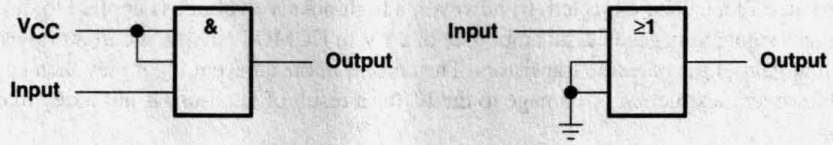


Figure 10. Fixed Potential Connected to Unused Inputs

Devices with multiple-emitter inputs (SN74 and SN74S series) are exceptions to the above. Since no voltage greater than 5.5 V should be applied to the inputs (because if exceeded, the base-emitter junction at the inputs breaks down), the inputs of these devices must be connected to the supply voltage V_{CC} via series resistor R_S (see Figure 11). This resistor should be dimensioned such that the current flowing into the gate or gates, which results from overvoltage, does not exceed 1 mA. But, because the high-level input current of the circuits connected to the gate flows through this resistor, the resistor should be dimensioned so that the voltage drop across it still allows the required high level. Equations 1 and 2 are for dimensioning resistor R_S, and several inputs can be connected to a high level via a single resistor, provided the following conditions are met:

$$R_{S(min)} = \frac{V_{CCP} - 5.5\ V}{1\ mA} \quad (1)$$

$$R_{S(max)} = \frac{V_{CC(min)} - 2.4\ V}{n \times I_{IH}} \quad (2)$$

Where:

n = number of inputs connected
I_{IH} = high input current (typical 40 µA)
$V_{CC(min)}$ = minimum supply voltage V_{CC}
V_{CCP} = maximum peak voltage of the supply voltage V_{CC} (about 7 V)

If whole parts of an IC are unused, the unused-input rules should be applied. If, for example, in an application only one flip-flop from a dual flip-flop type SN74ALS74 is used, all inputs of the unused flip-flop should be connected to a defined logic level, which, in this case, could be either low or high.

NOTE:
Unused outputs of a device should not be left unconnected.

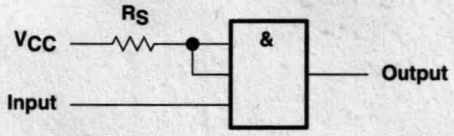


Figure 11. Series Resistor Connected to Unused Inputs of Multiple-Emitter Transistors

4 Excessive Input Currents

All ICs have protection circuits at outside connections. These diodes, or similar components, are intended to protect the device against destruction by electrostatic discharge. In addition, clamping diodes at IC inputs limit overvoltage and undervoltage resulting from line reflections and divert the currents that flow, in consequence, to either the negative (GND) or positive (V_{CC}) supply rails. Currents that flow in these circuit parts can, under certain circumstances, activate so-called parasitic transistors, which results in incorrect operation of the circuit.

Examples of this are the clamping diodes at the inputs of HCMOS devices, which are intended to limit overvoltages resulting from reflections. These diodes are created with a P-doped region in an N-doped substrate which, in turn, is connected to the positive supply voltage (see Figure 12). Between two adjacent diodes and in conjunction with the substrate, a parasitic PNP transistor is effectively created. A part of the current in one of the two clamping diodes is, therefore, not diverted to the V_{CC} rail but, instead, flows to an adjacent input. The current gain of this transistor is small (about 0.01), so that under normal operating conditions no effect can be expected. If, however, a high positive voltage is applied to the input of a circuit, as in Figure 12, which adapts signal voltages with an amplitude of 24 V to HCMOS circuits, a current flows into the adjacent input, despite the low current gain of the parasitic transistors. The current in the adjacent input may then be sufficient to generate a false input signal. However, destruction or damage to the IC (as a result of latch-up) is not likely to occur.

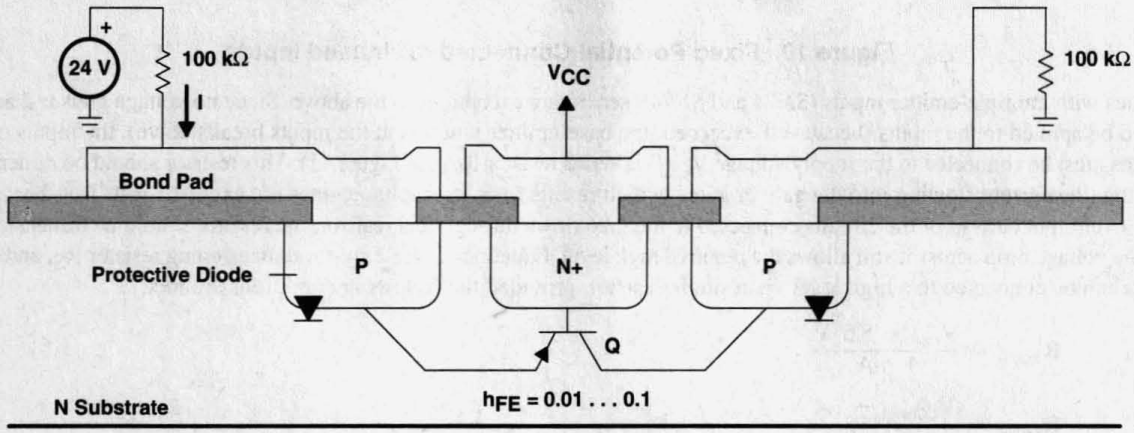


Figure 12. Parasitic Transistors in CMOS Input Stages

Similar effects caused by parasitic transistors can also be observed with bipolar transistors. Figure 13 shows a bipolar input that includes Schottky clamping diodes, realized with an N-doped region covered by a metallic contact. With a small negative input current, the forward voltage of the Schottky diode is about 400 mV, and the current in such an input is diverted, via the diode, to the GND pin of the device. If this current is increased, the forward voltage of the diode increases accordingly, and at a certain amplitude exceeds 700 mV. At this point, the silicon diode (which results from the N-doped region and the P-doped substrate under it, connected to the GND of the device) conducts. Here, also, a parasitic transistor is activated, whereby the whole adjacent N-doped region, comprising the collectors of active transistors, functions as a collector. This collects together a part of the current circulating in the substrate. If the amplitude of the negative current is sufficient, incorrect operation of the circuit can be expected.

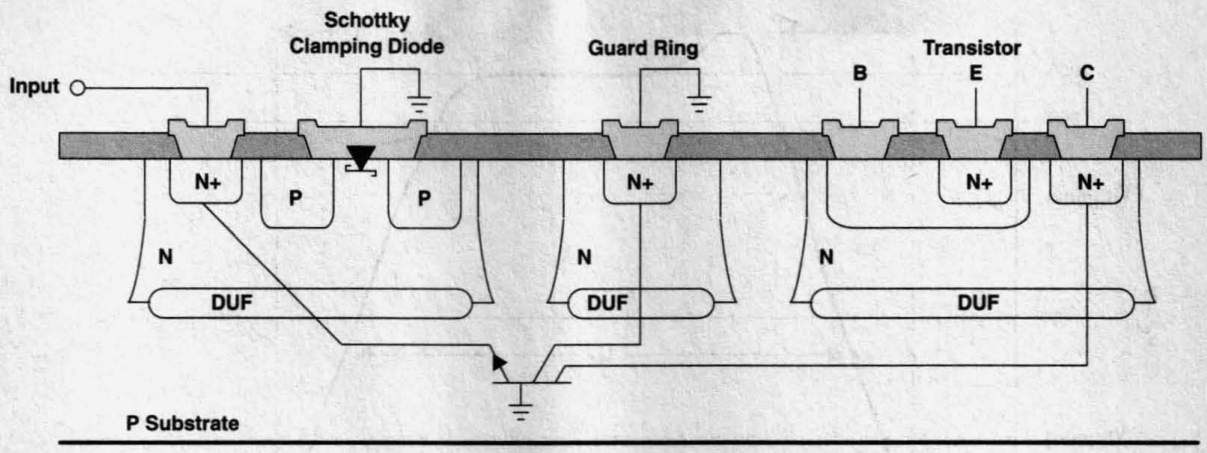


Figure 13. Parasitic Transistors in Bipolar Input Circuits

Negative voltage undershoot of considerable amplitude must be expected in practical operation of logic devices. Therefore, the semiconductor manufacturer must take the steps necessary to ensure reliable operation. Guard rings, which are placed in a ring around the circuit in question (see Figure 13), ensure reliable operation. In this example, these guard rings consist of an N-doped region connected to GND potential, which has the effect of an additional collector for the parasitic transistors, collecting the majority of the current circulating in the substrate and diverting it to GND potential. These guard rings are constructed so that a negative input current of $I_{IN} = -60$ mA with a duration t = 100 ns does not cause an incorrect function of the circuit. These values are again reflected in Figure 14. Here, a TTL device with a signal amplitude of 3 V drives a 10-meter-long coaxial cable with a characteristic impedance of Z = 50 Ω, at the end of which the input circuitry (with clamping diode) of the device in question is connected. High-amplitude current pulses, such as those generated by line reflection, are captured with this measuring setup.

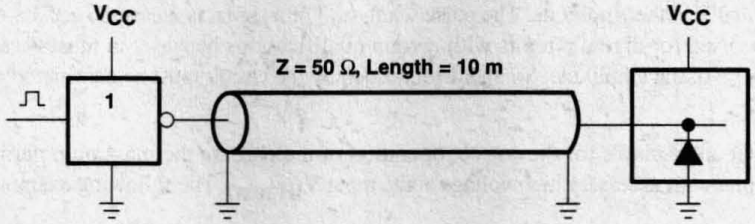


Figure 14. Setup for Generating an Undershoot Pulse (I = –60 mA, t = 100 ns)

Negative input currents with an amplitude of only a few milliamperes, but with a duration of several microseconds, can cause incorrect operation of the device. Since the transit frequency of the parasitic transistors is only about 1 MHz, the circuit and dimensioning of guard rings are simplified. A certain duration of the undershoot pulse is necessary to switch on the parasitic transistors, and possibly to cause abnormal operation of the circuit.

5 Transition Times

Correct operation of the circuit can be ensured only if the rise and fall times of the signal at the input do not exceed certain values. With CMOS devices (SN74HC and 74AC/SN74AC), these values are given in the data sheets. For devices from the SN74HC series, a rise and fall time (transition time) less than 500 ns is specified at $V_{CC} = 4.5$ V, while for ACL devices (74AC/SN74AC series), a value of 10 ns/V is given. Figure 15 shows this in more detail.

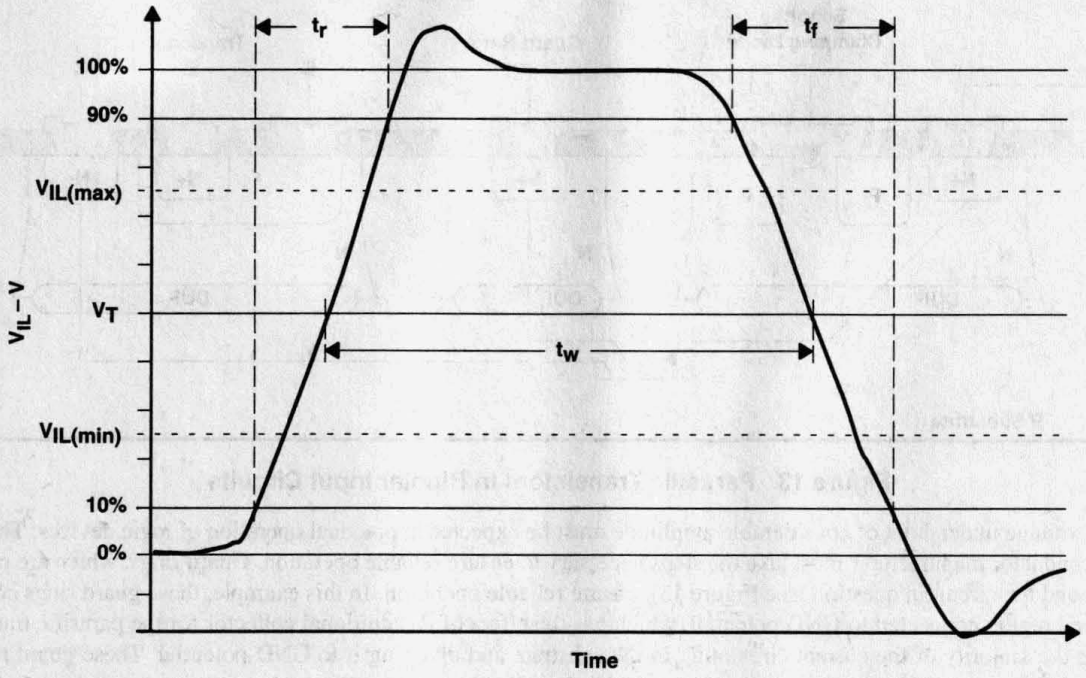


Figure 15. Definition of Signal Amplitude and Pulse Width

The signal amplitude is specified as the difference between the two stable signal levels for high (V_H) and low (V_L); overshoot and undershoot of the signal are not taken into account. The difference $V_H - V_L$ is taken as 100% of the amplitude. The rise time of the signal is defined as the time taken to rise from 10% to 90% of the full amplitude; similarly, the fall time is the time taken to fall from 90% to 10% of the amplitude. The pulse width (t_w) of a signal is measured at 50% of the amplitude. However, these definitions must be used for digital circuits with certain qualifications because, in most cases, the switching threshold (V_T) of the input is not 50% of the amplitude. So, the level needed by the circuit must be considered and, from this, the required signal waveform derived.

The values of voltage that are decisive for the correct operation of the part are the maximum permissible low voltage at the input $V_{IL(max)}$ and the minimum necessary high voltage at the input $V_{IH(min)}$. The following example applies for a device from the SN74HC series:

$V_{IL(max)} = 0.9$ V

$V_{IH(min)} = 3.15$ V at $V_{CC} = 4.5$ V

However, the rise and fall times are specified between 10% ($0.1 \times V_{CC} = 0.45$ V) and 90% ($0.9 \times V_{CC} = 4.05$ V) of the amplitude. The voltage waveform below 0.9 V (low level) and above 3.15 V (high level) has no influence on the function of the device, as long as the absolute maximum ratings are not exceeded. Therefore, it is better to define rise and fall times over the range between $V_{IL(max)}$ and $V_{IH(min)}$, which must be adhered to in order to ensure correct functioning of the device. From the amplitude (4.5 V) and the rise time specified in the data sheet ($t_r = 400$ ns), the transition time (dt/dv) rate can be derived as follows:

$$dv/dt = \frac{400 \text{ ns}}{(0.9 \times V_{CC}) - (0.1 \times V_{CC})} = \frac{400 \text{ ns}}{3.6 \text{ V}} = 110 \text{ ns/V} \quad (3)$$

The input signal must cross the region between $V_{IL(max)}$ and $V_{IH(min)}$ (and vice versa) at the transition rate or faster. This value is comparable to the transition rate given in 74AC-series data sheets of dt/dv = 10 ns/V. The pulse width (t_w) is measured at the actual threshold voltage (V_T) of the circuit and with CMOS devices at 50% of the amplitude. Bipolar and TTL-compatible CMOS devices have a switching threshold that is shifted considerably from the middle of the signal amplitude. This shift must then be taken into account when determining the pulse width. Table 1 shows the necessary minimum transition rise/fall rates for various logic families.

Table 1. Required Minimum Input Rise/Fall Rates for Logic Families

SERIES	V_{CC} (V)	$V_{IL(max)}$ (V)	$V_{IH(min)}$ (V)	V_T (V)	dt/dv (ns/V)
SN74	4.75–5.25	0.8	2	1.4	15
SN74LS	4.75–5.25	0.8	2	1.4	15
SN74S	4.75–5.25	0.8	2	1.4	15
SN74ALS	4.5–5.5	0.8	2	1.4	15
SN74AS	4.5–5.5	0.8	2	1.4	15
SN74F	4.5–5.5	0.8	2	1.4	15
SN74HC	2	0.3	1.5	1.4	625
	4.6	0.9	3.15	2.25	110
	6	1.2	4.2	3	80
SN74HCT	4.5–5.5	0.8	2	1.4	125
74AC	3	0.9	2.1	1.5	10
	4.5	1.35	3.15	2.25	10
	5.5	1.65	3.85	2.75	10
74ACT	4.5–5.5	0.8	2	1.4	10
SN74BCT	4.5–5.5	0.8	2	1.4	10
SN74ABT	4.5–5.5	0.8	2	1.4	5/10
SN74LV	2.7–3.6	0.8	2	≈1.5	100
SN74LVC	2.7–3.6	0.8	2	≈1.5	5/10
SN74LVT	3.0–3.6	0.8	2	1.4	10

The values for the transition rise/fall rates (dt/dv) are understood to be a level that ensures the function of individual components if the circuit is controlled with these rates. This does not necessarily mean that the device operates correctly under all circumstances in a large system. Figure 16 shows this in more detail. It shows two D-type flip-flops connected as a two-stage shift register. The first flip-flop is the TTL-compatible device 74ACT11074 (input threshold voltage = 1.5 V), but the second flip-flop (74AC11074) has CMOS-compatible inputs with an input threshold voltage of $0.5 \times V_{CC}$.

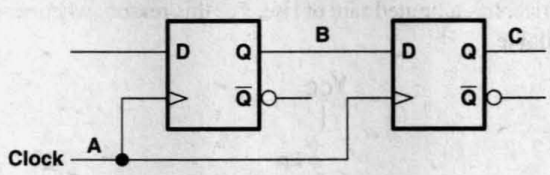


Figure 16. Two-Stage Shift Register

According to Table 1, devices from the 74ACT series must be controlled with a transition rate of at least 10 ns/V, if the function of individual parts is to be ensured. If, however, the behavior with time of the circuit is analyzed, it is found that the shift register does not behave as required (see Figure 17). When the clock signal reaches 1.5 V (having the required transition rate of 10 ns/V), the first flip-flop switches. The output typically reacts about 5 ns later. Only after another 5 ns does the voltage of the clock signal reach a value of 2.5 V, so that the second flip-flop switches. As a result of this late triggering, it accepts incorrect information: namely, the state that the first flip-flop has reached after the switching clock edge, and not the state that the flip-flop had before the clock edge.

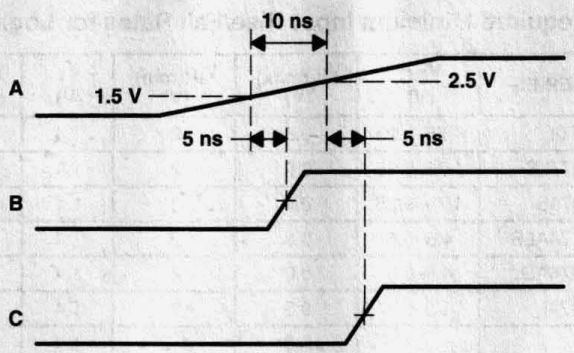


Figure 17. Incorrect Operation of a Shift Register

Under typical operating conditions, the circuitry would, however, operate correctly. The output signals of advanced CMOS devices have a rise time <5 ns (typical 2 ns). At the clock signal, a voltage change of 1.5 V to 2.5 V takes place in about 1.25 ns. A 74ACT11074 flip-flop has a minimum delay time of 1.5 ns, and under these circumstances correct functioning of the circuit is ensured.

Similarly, problems need not be expected when using devices from other families under similar conditions, as long as the signals have nominal rise and fall times. Under extreme conditions (for example, with unfavorable line routing), the switching times can be so lengthened that faults of the kind just described may occur.

6 Propagation Delay Times

6.1 Propagation Delay Times With Several Outputs Switching Simultaneously

The propagation delay times of circuits given in data sheets apply when only one output switches at a time. The reason for this is that the production equipment used to test circuits can test only one transmission channel at a time. If several outputs switch simultaneously, the propagation delay times given in data sheets can be used only with reservations. The reason for this is that the package inductances (L_P) of the supply-voltage lines, as well the output lines (see Figure 18), have a significant influence on the circuits and, thus, on the delay times. These inductances have the effect that the current in the power supply lines, and consequently in the output of the device, has a limited rate of rise. For this reason, when several outputs switch simultaneously, only a limited output current is available.

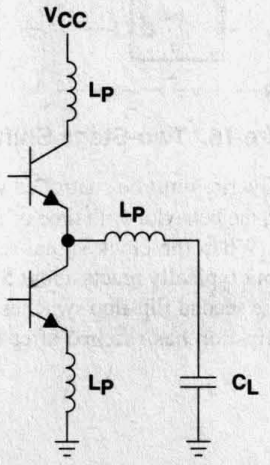


Figure 18. Inductances in the Lines Supplying a Package

Figure 19 shows the influence on the delay time of the number of outputs that are switched simultaneously. When packages having two supply-voltage pins (V_{CC} and GND) are used, as is the case with the majority of digital ICs, an increase of the delay time of 150 ps to 200 ps for each additional output that is simultaneously switched must be expected. With an octal bus driver, such as an SN74xx240, the delay time is increased by 1 ns to 1.4 ns when all eight outputs switch simultaneously. In those cases where there are several supply-voltage pins, such as the advanced CMOS devices in the 74ACT series from Texas Instruments (TI), the result influences speed of the circuit. As shown in Figure 19, the loss of speed of the components is halved when several outputs switch simultaneously.

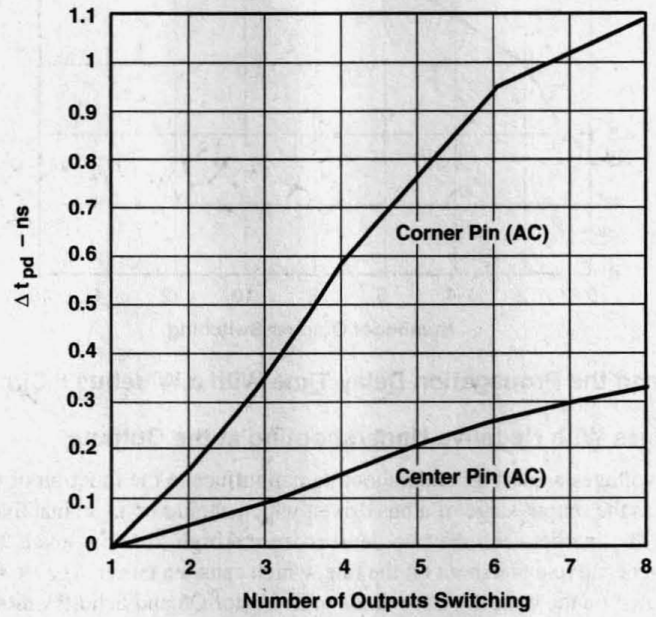


Figure 19. Increase of the Delay Time When Several Outputs Are Switched Simultaneously

With bus drivers and also VLSI circuits that have more than eight outputs that switch simultaneously, an appropriate number of additional supply-voltage pins are provided. A good example is given by the Widebus™ circuits from TI, which are bus drivers with 16, 18, or 20 outputs. To keep the loss of speed (because of so many outputs) within limits, about 25% of all pins of these devices are reserved for the provision of supply voltage. Figure 20 shows the increase of the delay time of a 74AC16240 as a function of the number of outputs that are switched simultaneously.

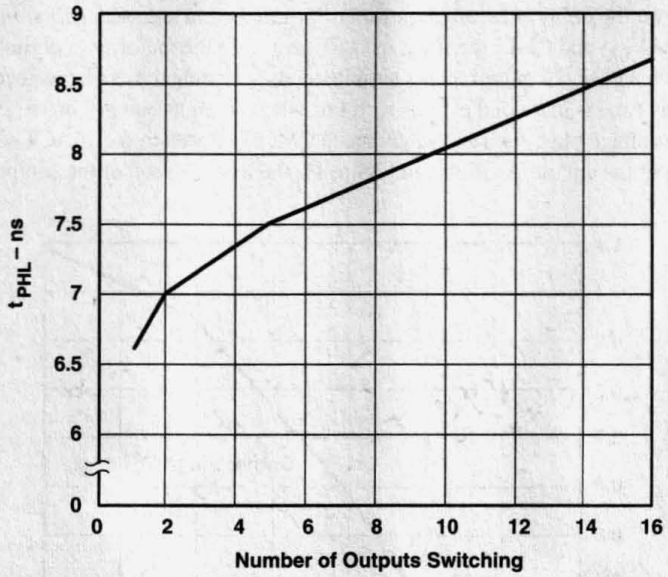


Figure 20. Increase of the Propagation Delay Time With a Widebus™ Circuit (74AC16240)

6.2 Propagation Delay Times With Negative Undershooting at the Outputs

With bipolar circuits, negative voltages caused by undershooting can influence the function of the device. Figure 21 shows this effect. This circuit represents the output stage of a bus driver, which should be in an inactive and high-impedance state. Active bus driver U1 switches the line between the two devices from a high to a low level. As a result of an inadequate termination of the line, there is a negative undershoot on the line, which causes a current (I_X) to flow in the internal circuit of the output stage. This current flows via the collector-base diode of transistor Q5 and Schottky diode D1, in parallel with it and via transistor Q1 to the base node of transistor Q2. Now this node is clamped to a low level. If this output stage should again be switched to the active state (output enable switches from low to high), the output does not follow until the capacitance of the bus line is charged through resistor R to the extent that the collector base diode of transistor Q5 is turned off again, which takes, typically, 5 ns to 10 ns. Apparently, the delay time to again switch on the output stage is increased by approximately this amount.

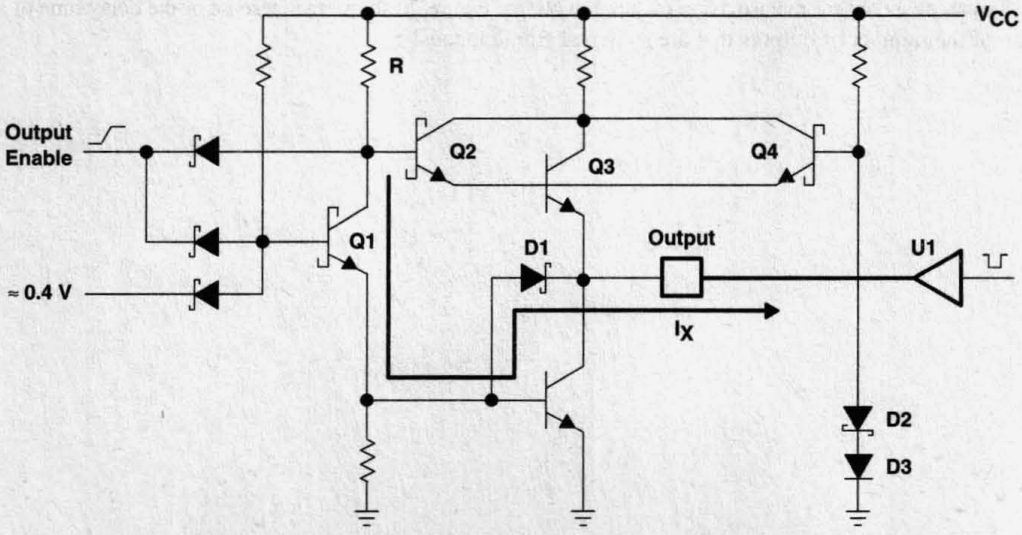


Figure 21. Currents in the Output Stage of a Bus Driver With Negative Undershoot

To prevent this delay, a clamping circuit (D2, D3, and Q4 in Figure 21) is integrated into modern bus drivers. This ensures that, should the output voltage go below –0.3 V, transistor Q3 switches on the output stage and the current I_X is diverted to the positive supply-voltage rail V_{CC}. With ABT devices, clamping is unnecessary and a different circuit that can be more effective is used.

6.3 Propagation Delay Times With Large Capacitive Loads

In digital IC data sheets, propagation delay times are specified with a capacitive load of 50 pF (15 pF on older logic families). This value represents the capacitive load of the test circuit on the output of the IC being tested. This value is also the capacitive load when the output drives five inputs of other circuits and this assumes that the length of the connecting lines is only a few centimeters, as is typically the case on printed circuit boards (PCBs). With such short lines, the first assumption is that the line itself behaves like a capacitor, which additionally loads the output and influences the propagation delay time accordingly. However, with long lines, this assumption leads to errors, because the signal delay is actually determined by the propagation speed of the electrical wavefront along the line. In fact, the propagation delay time of the IC is determined by the loading of the output, that is, by the characteristic impedance of the line to which it is connected, not by its length or capacitance. When driving a line terminated at its end with a resistance of 100 Ω and lengths of 0 (resistor connected directly to the output), 1 m, and 11 m (see Figure 22), an SN74LS00 device has the output waveforms shown in Figure 23. The three resulting output signals are shown staggered, and are practically identical, i.e., the propagation delay time of the IC is not influenced. The length of the line and the resulting signal propagation time (5 ns/m) influence the delay time of the system. The propagation time of the wave along an 11-m transmission line is 55 ns. Add the propagation delay time of the SN74LS00 of about 10 ns for a total delay of 65 ns.

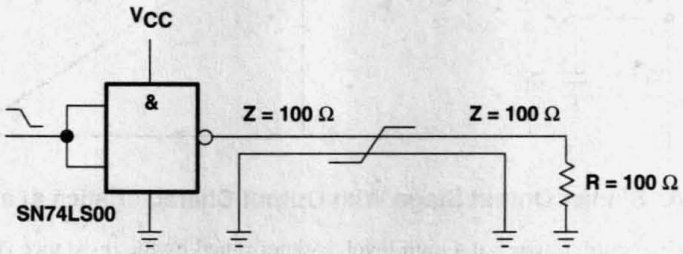


Figure 22. Measurement Setup

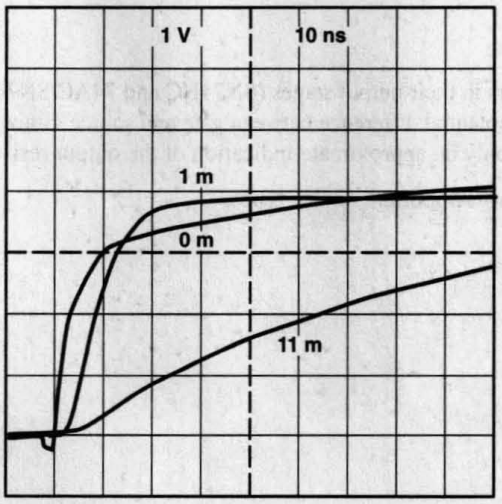


Figure 23. Waveforms for Various Line Lengths

If the capacitive load connected to the output of a device is represented as a single capacitor, the resulting propagation delay time can be calculated. A purely capacitive load can be assumed if the output of the IC controls a MOS power transistor with a relatively large input capacitance. To a first approximation, this assumption is correct if an output drives adjacent inputs over a line length of only a few centimeters. The propagation delay times given in data sheets consider the following:

- Propagation delay time through the internal circuitry of the IC
- Delay resulting from the switching time of the output stage
- Time needed to charge and discharge the capacitance of the load (typically 50 pF)

The first two considerations are independent of the load that is connected. The last consideration must account for the actual load, of which a load capacitance of C1 = 50 pF (15 pF) is already given in data sheets. The time taken to charge the additional capacitance is determined by the current that the device is able to deliver. For the high level, this value can be deduced indirectly from the data sheet. Figure 24 shows the relevant part of the circuit of a bipolar output stage and the resulting output characteristics.

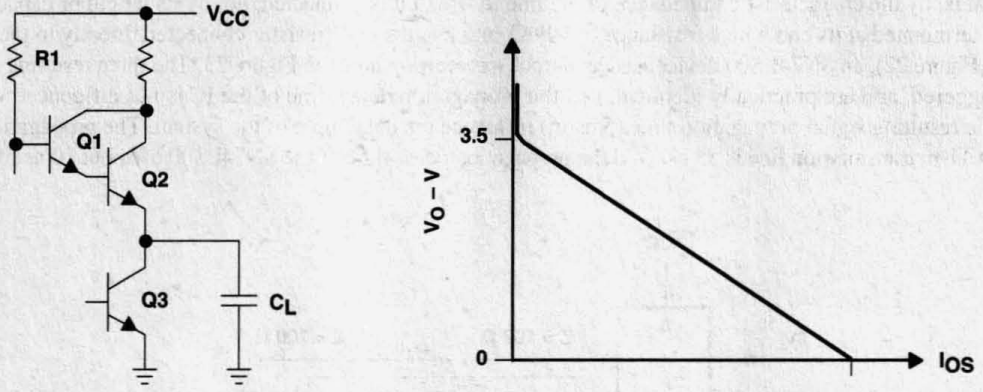


Figure 24. Bipolar Output Stage With Output Characteristics at a High Level

The short-circuit current of the output, when at a high level, is determined by the resistance (R1) and the saturation voltage of Darlington transistors Q1 and Q2 with collector-path resistance. Using the following equation, the internal resistance (R_O) of a circuit can be determined from the open-circuit output voltage (typically 3.5 V) and from the short-circuit current (I_{OS}) given in the data sheet:

$$R_O = \frac{3.5\ V}{I_{OS}} \quad (4)$$

With circuits that use MOS transistors in their output stages (SN74HC and 74AC/SN74AC), the output current is determined by the size of the transistors and the potential difference between gate and source. Since there is no linear relationship between this voltage and the output current, only an approximate indication of the output resistance can be made.

Table 2 shows I_{OS} and R_O for the most important device types.

Table 2. Short-Circuit Current and Internal Resistance of Logic Families

TYPE	SHORT-CIRCUIT CURRENT I_{OS} (mA)	INTERNAL RESISTANCE R_O (Ω)
SN7400	35	50
SN7440	45	75
SN74LS00	35	100
SN74LS40	65	53
SN74LS240	70	50
SN74S00	65	53
SN74S40	140	25
SN74S240	60	58
SN74ALS00	50	70
SN74ALS40	60	58
SN74ALS240	100	35
SN74ALS1000	120	29
SN74AS00	100	35
SN74AS240	140	24
SN74AS1000	160	21
SN74F00	85	41
SN74F40	140	25
SN74F240	140	25
SN74BCT240	140	25
SN74BCT25240	700	5
SN74ABT240	120	29
SN74HCT00	60	40–120
SN74HCT240	80	30–100
74ACT11000	220	4–25
74ACT11240	220	4–25
SN74LV00	35	35–100
SN74LV240	55	25–80
SN74LVC00	85	16–40
SN74LVC240	85	16–40
SN74LVT240	400	8

The typical output voltage of a bipolar device at a low level is about $V_{OL} = 0.3$ V. The increase of the delay time resulting from the capacitive load (C_L) is determined by the time until the external load capacitance has been charged by an external voltage source from V_{OL} to the threshold voltage of the circuit, typically $V_S = 1.5$ V. The external voltage source is described by an internal voltage (V_{OH}) and an internal resistance (R_O). In this way, the delay time (t_d) resulting from the load capacitance can be calculated from the following equation:

$$t_d = \ln\frac{V_{OH} - V_{OL}}{V_{OH} - V_S} \times R_O \times C_L = \ln\frac{5.5\text{ V} - 0.3\text{ V}}{3.5\text{ V} - 1.5\text{ V}} \times R_O \times C_L = 0.5 \times R_O \times C_L \quad (5)$$

Figure 25 shows the waveform of the positive edge at the output of a gate (SN74LS00) with various values of capacitive loads (C_L = 10 pF, 56 pF, and 616 pF). As expected, the rise time at the output and the resulting increase of the propagation delay time are determined by the time constant $R_O \times C_L$.

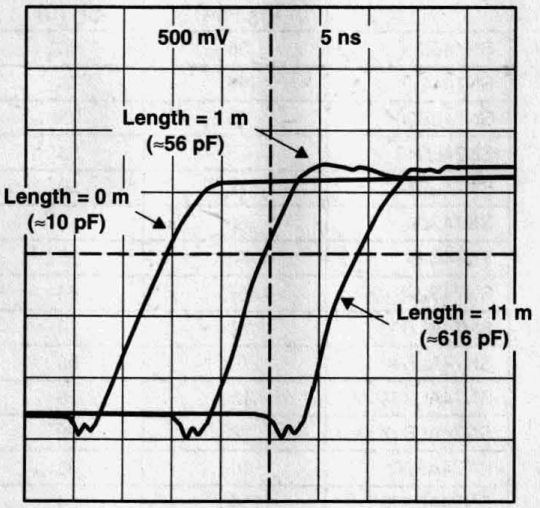


Figure 25. Waveform at SN74LS00 Output (C_L = 10 pF, 56 pF, and 616 pF)

The values for the low level of a bipolar device cannot be taken directly from data sheets. Transistor Q3 in Figure 24 is responsible for the output current I_{OL}. As with all semiconductor components, this parameter is nonlinear, and is influenced by the distribution of components in the circuit on such parameters as current gain, conductance, and resistance values. For this reason, only a rough calculation of the actual output current at low level is possible. As a first approximation, the internal resistance of the circuit at low level is lower than at high level. It follows that, in the worst case, the increase of the delay time of the negative edge is always smaller than that of the positive edge (see equation 5). The precise value must be determined in individual cases by measurement.

6.4 Input and Output Capacitances of Digital Devices

All digital devices capacitively load the outputs of the circuits driving them. The input and output capacitances are given in Table 3. These are typical average values for the logic families shown. Different circuit configurations are used within a family, depending on the function and application. Therefore, wide variations from the values given in data sheets can occur with individual devices. In specific cases for new families, the values given in data sheets should be taken as a basis. If this data is not available, for example with older families, the user must make appropriate measurements if more precise values are needed.

The capacitances given in Table 3 are measured at the following voltages:

- Bipolar devices: V = 2.5 V
- CMOS devices: V = 0 V and V = 2.5 V

Table 3. Capacitances of Digital Devices

FAMILY	INPUT CAPACITANCE (pF)	OUTPUT CAPACITANCE (pF)	
		OPEN-COLLECTOR OUTPUT†	BUS DRIVER
SN74	3	5	–
SN74LS	3.5	3.5	5
SN74S	3.5	3.5	9
SN74ALS	2	4	5
SN74AS	4	–	10
SN74F	5	5	9
SN74HC	3	3	9
74AC/SN74AC	4	–	10
SN74BCT	6	–	12
SN74ABT	4	–	8
SN74LV	3	–	8
SN74LVC	4	–	8
SN74LVT	4	–	8

† Open-collector output of gates and other devices with low drive capability (e.g., SN74xx03). Open-collector outputs of bus drivers have the same output capacitance as totem-pole (3-state) outputs.

7 Bus Conflicts

If several bus drivers with 3-state outputs are connected to a single bus, it often cannot be ensured that during the time when switching from one bus driver to another, both are not simultaneously active for a short time. For this short time, a short circuit of the outputs exists, resulting in an overload of the circuit. This situation is known as *bus conflict*.

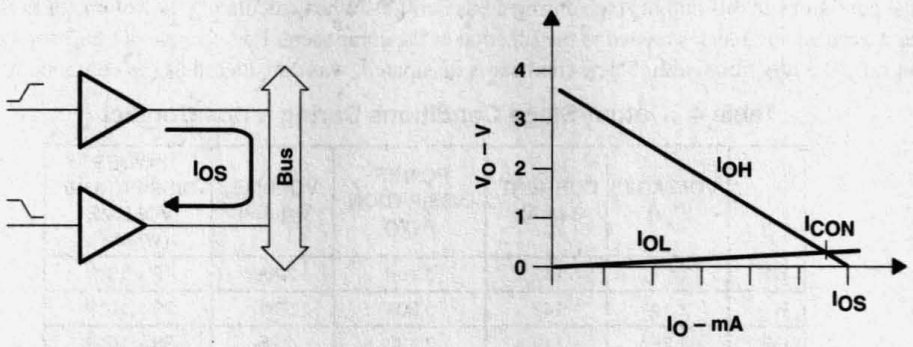


Figure 26. Determining the Short-Circuit Current With a Bus Conflict

The currents that result from bus conflict can be calculated by means of the output characteristics of the devices (see Table 2). As shown in Figure 26, the short-circuit current (I_{OS}) is limited by the high-output current of the devices involved in the bus conflict. With bus drivers having an output current of I_{OL} = 64 mA (SN74AS, SN74F, SN74BCT, SN74ABT, or SN74LVT), a current I_{OS} = 120 mA flows in such a case. The power dissipation (P_{conl}) of the output supplying the low level, as shown below, can be ignored.

$$P_{conl} = V_{OL} \times I_{OS} = 0.5\ V \times 120\ mA = 60\ mW \quad (6)$$

Even if all eight outputs of a bus driver are involved in a bus conflict, the total power dissipation is less than 500 mW. However, the situation is different at the outputs supplying the high level. In this case, the short-circuit power dissipation (P_{conh}) of each output is as follows:

$$P_{conh} = (V_{CC} - V_{OL}) \times I_{OS} = 4.5\ V \times 120\ mA = 0.54\ W \quad (7)$$

If all eight outputs of a bus driver are involved in this bus conflict, the total power dissipation is about 5 W. With Widebus circuits, it is 10 W and more.

To analyze the situation inside an IC under these extreme conditions, one has to know that the heat caused by this power dissipation is not immediately spread over the total chip. Rather, one has to consider a certain propagation speed of the heat, which is about 1 µm/µs. This means that during a bus conflict with a duration of only a few nanoseconds, the heat is not distributed over all the chip. In the first moment, the affected component inside the IC (the transistor or resistor) heats up. The resulting increase in temperature can be calculated by knowing the volume of the component in question and the thermal capacitance of silicon. By using the output stage of an ABT device (see Figure 27), this is shown in detail. Also, all voltages are shown in this circuit diagram that apply when the output, which should provide a high level, is forced to 0.5 V externally.

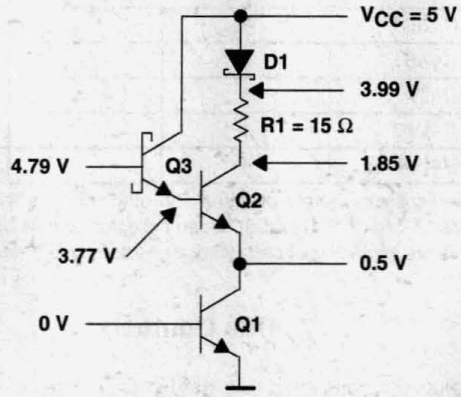


Figure 27. ABT Output-Stage Circuit Diagram

Table 4 shows the conditions in this output stage during a bus conflict. When calculating the volume of the single components, only that volume was considered that is related to the function of the component. For example, a transistor's total area was taken into account, but only the junction width, where the heat is dissipated, was considered as the component's height.

Table 4. Output-Stage Conditions During a Bus Conflict

	VOLTAGE V (V)	CURRENT I (mA)	POWER DISSIPATION P (W)	VOLUME V (μm^3)	POWER DISSIPATION/ VOLUME ($W/\mu m^3$)
D1	1.01	142	0.156	3200	46×10^{-6}
R1	2.14	142	0.304	3840	79×10^{-6}
Q2	1.35	142	0.192	495	38×10^{-3}

According to this analysis, the highest power dissipation per volume unit is found in transistor Q2. This is because the junction width of only 0.5 µm was considered as the height of this component. Using equation 8, calculate the temperature increase ($\Delta\vartheta$):

$$\Delta\vartheta = \frac{P \times t}{V \times c_P} \tag{8}$$

Where:

c_P = heat capacitance of silicon = 1.631×10^{-3} Ws/Kmm^3
P = power dissipation
t = time
V = volume

Considering a propagation speed of the heat of 1 µm/µs and a junction width of 0.5 µm, one can assume that during the first 500 ns of a bus conflict the heat is not distributed over the chip, but stays in the transistor junction. Under this condition, $\Delta\vartheta$ is calculated as follows:

$$\Delta\vartheta = \frac{0.192\ \text{W} \times 500\ \text{ns}}{495\ \mu\text{m}^3 \times 1.631 \times 10^{-3}\ \frac{\text{W} \times \text{s}}{\text{K} \times \text{mm}^3}} = 119\ \text{K} \tag{9}$$

Short bus conflicts, with a duration of a few, or of a few tens of nanoseconds, cause a temperature increase of the component in question of about 10°C. Therefore, a degradation of the reliability of the component is unlikely. Furthermore, in well-designed systems, the period of bus conflicts is high compared to the duration of the bus conflict (period:duration > 10:1). Conservatively, the mean chip temperature should be calculated to ensure that this temperature does not increase beyond 150°C. Beyond this temperature, the thermal expansion coefficient of the plastic material of the package becomes different from the expansion coefficient of silicon. This fact is likely to lead to a mechanical stress at high temperatures, which can result in failure of the bond wire.

The total power dissipation (P_T) of a bus driver is calculated by the following equation:

$$P_T = P_O + (P_S \times t_S + P_C \times 2\tau + P_{con} \times t_{con}) \times f \times n \tag{10}$$

Where:

f = frequency
n = number of outputs at which a bus conflict occurs
P_{con} = power dissipation during bus conflict
P_C = power dissipation when discharging the bus capacitance
P_O = quiescent power dissipation
P_S = power dissipation resulting from current spikes when output switches
t_{con} = duration of bus conflict
t_S = duration of current spike
τ = signal propagation time on the bus

The power dissipation of a bus driver is calculated in a practical example in accordance with the following assumptions:

- Circuit: SN74F245
- P_O = 0.45 W (from data sheet)
- P_S = 5 V × 30 mA = 0.15 mW with t_s = 5 ns (measured)

To calculate the power dissipation (P_C) that occurs when charging the capacitance of the bus line, the voltage waveform at the output with the given load (the line impedance) must be known. The easiest way to determine this is to use the Bergeron diagram. With a line impedance of 30 Ω, a stable state is reached after double the time of the signal propagation with a positive edge. That is, for this time, a current is supplied into the line from the driver circuit. The amplitude of the preceding waveform and the output voltage of the circuit is about $V_O = 2$ V. The power dissipation during this time and under these load conditions is calculated as follows:

$$P_C = (V_{CC} - V_O) \times \frac{V_o}{Z_o} = (5\text{ V} - 2\text{ V}) \times \frac{2\text{ V}}{30\ \Omega} = 0.2\text{ W} \quad (11)$$

The signal propagation time on a backplane in a 19-inch rack (wire length about 40 cm) is $\tau = 10$ ns.

Further, assuming a bus cycle time of 100 ns (f = 10 MHz), a duration of the bus conflict of 10 ns, and that all eight outputs of the device are involved, the resulting total power dissipation is calculated as follows:

$$\begin{aligned} P_T &= 0.45\text{ W} + (0.15\text{ W} \times 5\text{ ns} + 0.2\text{ W} \times 2 \times 10\text{ ns} + 0.53\text{ W} \times 10\text{ ns}) \times 10\text{ MHz} \times 8 \\ &= 0.45\text{ W} + (0.75\text{ nW/s} + 4\text{ nW/s} + 5.3\text{ nW/s}) \times 10\text{ MHz} \times 8 \\ &= 1.29\text{ W} \end{aligned} \quad (12)$$

This power dissipation results in a rise of the temperature of the chip, which, in turn, influences the reliability of the device. The chip temperature can be calculated as follows:

$$T_J = T_A + P_T \times R_{\Theta JA} \quad (13)$$

Where:

$R_{\Theta JA}$ = thermal resistance of package
T_A = ambient temperature
T_J = chip temperature

Table 5 shows the typical thermal resistance of the packages, which are mostly used for digital devices. These must be considered as typical values, because a number of factors determine the actual value, including chip size, lead-frame material, composition of the plastic, ambient air flow, and thermal properties of the circuit board. The values given apply if the device is soldered onto a PCB.

Table 5. Thermal Resistance of Plastic Packages in Still Air

NO. OF PINS	THERMAL RESISTANCE (°C/W)	
	DL PACKAGE	SO PACKAGE
14	86	117
16	80	110
20	78	95
24	73	85

According to Table 5, the thermal resistance of a 20-pin DL package is $R_{\Theta JA} = 78$°C/W. This means that, in equation 8, the chip temperature would be about 100°C above the ambient temperature. The chip temperature must not be allowed to exceed 150°C, because the reliability would be reduced significantly. Therefore, the maximum permissible ambient temperature is, in this case, 150°C – 100°C = 50°C.

In cases in which bus conflict can occur, which is in most bus applications, power dissipation is of particular importance. There is usually nothing that can be done about dynamic conditions (the frequency of operation) without adversely affecting the performance of the system. Also, the overlap of operating states cannot always be prevented if worst-case conditions are taken into account. However, bus conflicts of a duration of a few, or of a few tens of nanoseconds should not be a problem. The choice of the most suitable components allows control of the quiescent power dissipation. With fast bipolar logic families (SN74S, SN74AS, and SN74F), the permissible total power dissipation might be exceeded because of their high quiescent power dissipation. Better, in this respect, are the SN74LS and SN74ALS series. Because of their lower quiescent-current requirements, bus conflicts do not result in overdissipation in most cases. Even better are devices from the BiCMOS series and all CMOS devices, although in CMOS parts, a part of the advantage of their low quiescent current is lost by their higher dynamic power dissipation.

One critical application area is bus conflicts during the power-on phase of a system. These bus conflicts occur because, during the power-on phase (system reset), the supervising circuit does not provide defined control signals even though the rest of the system may already be functional. Therefore, there is a high probability that various bus drivers might be accidentally activated at the same time. This, again, results in bus conflicts that can last several 100 ms (duration of the power-on phase or reset time). Because the thermal time constant of an IC is about 1ms to 5 ms, after this time expect the final temperature in the device to be determined by momentary power dissipation. If a total power dissipation of 5 W in an 8-bit device during this bus conflict is assumed, a theoretical 500°C overtemperature of the chip must be considered. With Widebus circuits, the theoretical overtemperature is 1000°C. Mostly, these devices are immediately destroyed during these kinds of bus conflicts. Even if no defect is detected after such a bus conflict, a dramatic degradation of the device is likely, which leads to a final destruction of the component some time later.

An adequate design of the control logic prevents bus conflicts during the power-on phase of a system. Preventing bus conflicts is not easy because no defined supply voltage can be expected during the power-on phase. Therefore, no defined operation of the logic circuits can be expected. The supply-voltage range below 3 V usually is not critical. Many advanced bus drivers contain a supply-voltage monitor that disables the outputs (3-state) as long as the supply voltage is lower than about 3 V. Furthermore, below this voltage, an overload of the devices is unlikely, because under this condition, the drive capability is very limited. Above a supply voltage of 3 V, additional measures are necessary. One method is to connect a pullup resistor between the enable inputs of the bus-interface circuits and the positive supply rail. This may ensure a high level as long as the preceding control logic does not provide a defined logic level, but is not helpful if the control logic delivers a wrong logic level. A reliable solution is to disable all bus-interface circuits in question during the critical time with additional control logic (see Figure 28). In this circuit, a supply-voltage monitor (TLC7705) provides a signal that disables all bus drivers during the critical time period and may reset the main processor, which then resets the control logic of the system. For this kind of application, bus-interface circuits that provide two enable inputs, like the SN74ABT541, are advantageous. One control input controls the normal operation via the system-control logic. The other input is connected to the monitor device to disable the bus logic when an undefined system condition (e.g., during power on) is expected. If no second enable input is available, such as in an SN74ABT245, another gate is required to perform the additional disable function.

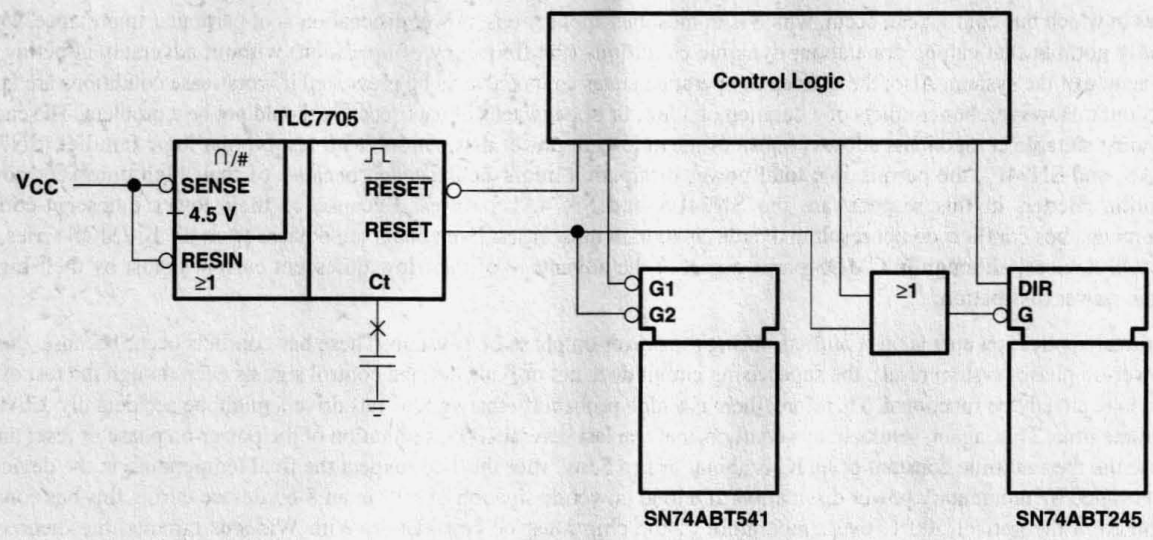


Figure 28. Bus Supervision During Power On

CAUTION:

Since considerably higher currents flow during bus conflicts on signal lines than with normal operation, the noise margin in the system is reduced accordingly. This can result in faulty operation and care should be taken to avoid bus conflicts.

8 Backdriving

The testing of highly complex electronic systems must ensure that the system or subsystem operates faultlessly. For this purpose, it is advantageous to install at the system level diagnostic programs that are able to recognize and localize faults. Certain limitations are unavoidable with self-testing because a defective system may no longer be able to seek and localize faults. This method usually breaks down completely when individual component groups are being tested because fault diagnosis on their own is generally too limited. In such cases, additional test equipment that stimulates the component group with special test signals, test samples, or patterns, and analyzes the results is necessary.

If all relevant circuit segments in the component group can be addressed via a defined interface, e.g., built-in testability (BIT), testing can be performed without additional test circuits and adapters. Test bus IEEE 1149.1 (JTAG), with an appropriate IC interface, allows testing of all circuits, the connections between them, and the complete subsystem.

If this option is not available, appropriate signals can be injected into the circuit from outside to achieve the required circuit stimulation. For this, the inputs to the circuits to be tested must be supplied with the necessary voltages (e.g., logic low or high) via nail-bed adapters and the reaction at the outputs of these circuits is monitored. In this way, the functions of complex systems can be tested step by step and the most common faults recognized, such as:

- Solder bridges and broken metallization
- Incorrect, faulty, damaged, or missing devices
- Functional disturbances and signal-processing faults

Because only a few single devices are accessed at a time, only the special, appropriate functions (e.g., the truth table of a gate) need to be known, not the function of the complete device group. In this way, standard test program libraries can be used to put together the complete test program. With this method, large systems also can be tested step by step without using excessively complex test procedures.

The stimulation of the circuit to be tested might present a problem. For example, the inputs of gate G3 (see Figure 29) must be switched to a particular potential. These same inputs are already controlled by other devices (G1 and G2), which supply their own signals to the gates to be tested. The test equipment must be able to force another voltage on to the same node as is supplied by the existing circuit. The expression commonly used here is *backdriving* or *node forcing*. The output of a device is forced from outside into a state not corresponding to its normal control-logic state.

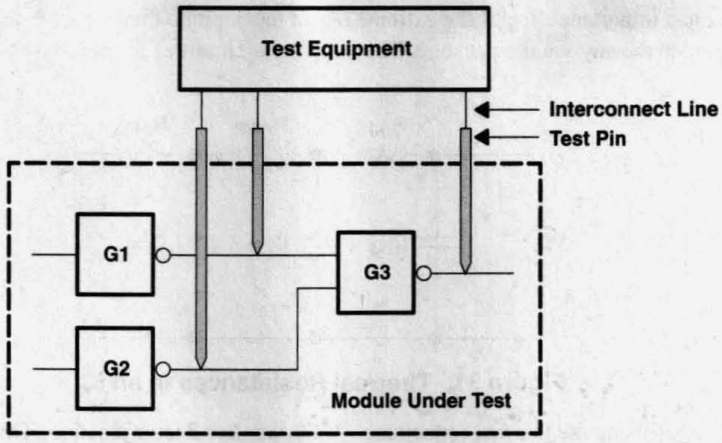


Figure 29. Feeding Test Signals Into a Node Test Point

The test equipment must have substantial drive capability to force the IC into another logic state. Table 2 gives the short-circuit current at high level of the most important logic families. The situation in which the test equipment must force an output to low level is not the most demanding requirement. Currents of up to several-hundred milliamperes must be provided to force from outside an output that is supplying a low level into a high-level state.

Serious interference arises when the high currents are switched on or off and line reflections occur on the lines connecting the test equipment and the circuit being tested. All these effects can result in a real or apparent malfunction of the circuit being tested. This test method is of limited use when the precise timing of fast circuits must be assessed.

When injecting the test-signal current into the outputs, which then must be forced into an inverted state, the devices usually are driven far outside their maximum permissible ratings. This can damage or destroy the devices. At the very least, their reliability and, therefore, their operating life, is adversely affected. In recent years, the drive capability (maximum output currents) of ICs has been steadily increased in the interest of improved technical performance. Modern bus-driver currents of 500 mA and more are needed to force the outputs of devices to particular logic levels (see Figure 30). The high current densities in the internal connections of ICs can cause a drift of metallic ions, or so-called electromigration. This effect begins at current densities of 3×10^5 to 10^6 A/cm^2. Metallic ions are released from the grain boundaries and then drift in the inverse direction of current flow (in the direction of the electron flow). If the excessive current density lasts long enough, the interconnections are eroded.

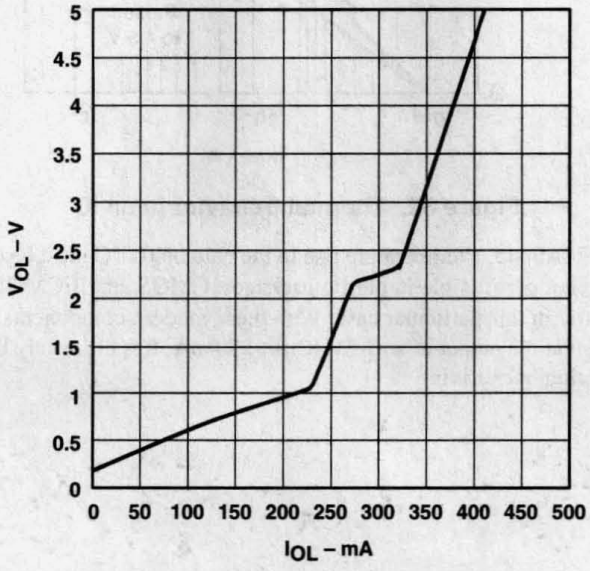


Figure 30. Low-Logic-Level Output Characteristics of SN74AS645

When backdriving, the most important effect is the extreme rise in temperature that occurs in the chip during the test. The heat that results must be conducted away via the package. The equivalent circuit of Figure 31 shows the thermal relationships in the package.

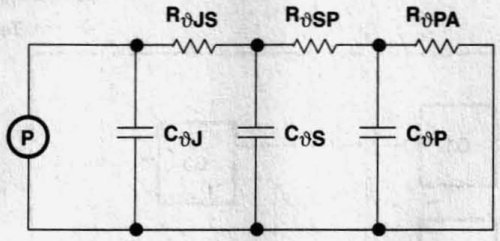


Figure 31. Thermal Resistances in an IC

The thermal source (P) first fills up the thermal capacitance of the semiconductor junction. The heat spreads, via $R_{\vartheta JS}$, in the complete substrate (chip) of the IC. From there, the heat flows, via the resistance ($R_{\vartheta SP}$), into the package and then, via the resistance ($R_{\vartheta PA}$), to the ambient environment. Only the sum of the thermal resistances $R_{\vartheta JU} = R_{\vartheta JS} + R_{\vartheta SP} + R_{\vartheta PA}$ (thermal-resistance junction ambient) is given in data books (see Table 5). This resistance is not helpful for the problem under consideration but it can be used to calculate the temperature in a stable state. Rapid temperature increases, such as result from backdriving, cannot be calculated from the sum of thermal resistances. The thermal capacitance and thermal conductivity of the chip can be calculated, but it is better to determine the thermal behavior through measurements (see Figure 32).

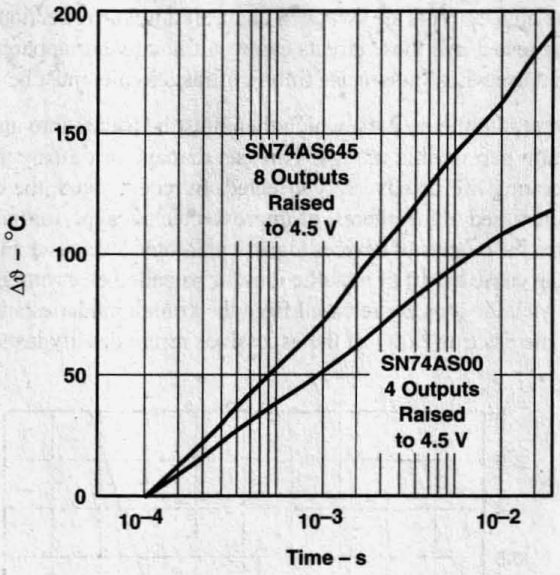


Figure 32. Thermal Behavior in an IC

Figure 32 shows that, with an SN74AS645, a temperature rise in the chip of 100°C must be expected after 2 ms. After 10 ms, temperatures are attained that are not permissible in plastic packages. CMOS and BiCMOS circuits have a very low power dissipation and do not behave better in this particular case. With these modern components, expect at least the same driving capability. The short-circuit current at the output of an ACL IC is >250 mA. It is ultimately these currents that are responsible for the high power dissipation during backdriving.

The following rules always should be observed when using the test methods discussed:

- Backdriving should be used only when the state required at the node point in question can be reached in no other way.
- The maximum permissible power dissipation of an IC should not, under any circumstances, be exceeded.
- Outputs that are at a low-level state, as a result of their logic functions, can be raised to a level of $V_O = 3$ V for a short period by backdriving. The energy, which as a result of this backdriving is injected into the device ($V_O \times I_{OL} \times t_{pd}$), must not exceed 25 mW/s. The current that results in an output should not exceed a value of $I_{OL} = 300$ mA. The pulse duration must not exceed $t_d = 100$ ms. To keep the thermal stress within acceptable limits, the duty cycle of the pulses (duration of the pulse ÷ duration of the period) should be less than 1:10.
- Outputs that are in a high-level state as a result of their logic functions can be lowered to a level of 0 V for a short time by means of backdriving. One output of a device can be short circuited to ground, in such a case, for maximum $t_d = 100$ ms. The product of the output current, the supply voltage, and the pulse duration ($I_{OH} \times V_{CC} \times t_{pd}$) must not exceed 25 mW/s. If n outputs are simultaneously short circuited to ground, limit the total energy injected into the device under test ($I_{OH} \times V_{CC} \times t_{pd}$) to 25 mW/s. To keep the thermal stress within reasonable limits, the duty cycle of the short circuit (short-circuit duration ÷ repetition time) should be less than 1:10.
- All voltages, including peak voltages of overshoots/undershoots, must be within the absolute maximum ratings on data sheets.
- Simultaneous backdriving of several outputs in parallel (wired OR) with a common current source is not permissible. Since current sharing cannot be predicted, there is danger of overloading the circuit.
- The chip temperature of the circuit under test must not exceed 125°C.
- Open-circuit (unterminated) lines should be avoided to prevent faults caused by reflection.

Semiconductor device manufacturers consider testing with backdriving as involving a measure of risk. The danger of overloading devices cannot be excluded since they are operated in regions that can lie far outside those for which they were designed. For this reason, no statement about the reliability of devices that are subjected to this test procedure can be made. TI does not use such test methods. Such test methods are not permissible in many (e.g., military) areas of application.

9 Summary

This report provides the designer of digital systems information that is not found in data books, but which is of interest and necessary in many applications. The differences between individual circuit families have been discussed. The circuit design techniques used with various devices, combined with the different technologies used to manufacture them, often make it difficult to give specific design rules; in many cases it is possible to give only very general guidance. In practice, few parameters are actually measured, particularly with older devices. In all such cases, this report provides guidelines that enable the designer to predict the behavior of circuits in a system.

Acknowledgment

The author of this document is Eilhard Haseloff.

General Design Considerations 1
Backplane Design 2
Device-Specific Design Aspects 3
5-V Logic Design 4
3.3-V Logic Design 5
Clock-Distribution Circuits (CDC) 6
Boundary-Scan IEEE Std 1149.1 (JTAG) Logic 7
Packaging 8
Index 9

Contents

GTL/BTL: A Low-Swing Solution for High-Speed Digital Logic 2–3

Next-Generation BTL/Futurebus Transceivers Allow Single-Sided SMT Manufacturing .. 2–19

The Bergeron Method:
A Graphic Method for Determining Line Reflections in Transient Phenomena 2–31

Live Insertion 2–59

GTL/BTL: A Low-Swing Solution for High-Speed Digital Logic

SCEA003A
March 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**2–7**
Test Setup	**2–7**
Advantages of GTL or BTL Over CMOS/TTL	**2–8**
GTL Family Input and Output Structure	**2–8**
BTL Family Input and Output Structure	**2–9**
Power Consumption	**2–10**
Simultaneous Switching	**2–11**
Output Capacitance	**2–13**
Slew Rate	**2–13**
Signal Integrity	**2–15**
Design Considerations	**2–15**
Summary	**2–17**
References	**2–17**

List of Illustrations

Figure	*Title*	*Page*
1	Backplane Model With All Four Boards Connected	2–7
2	Point-to-Point Model With Only One Driver and One Receiver Connected	2–7
3	Typical GTL Input and Output Cells	2–9
4	Typical BTL Input and Output Cells	2–9
5	FB1650 and GTL16612 Power Consumption With All Outputs Switching	2–10
6	FB1650 High Output Voltage Peak and Valley Noise on an Unswitched Output	2–11
7	GTL16612 High Output Voltage Peak and Valley Noise on an Unswitched Output	2–12
8	FB1650 Low Output Voltage Peak and Valley Noise on an Unswitched Output	2–12
9	GTL16612 Low Output Voltage Peak and Valley Noise on an Unswitched Output	2–12
10	Capacitance Variation Across Process	2–13
11	FB1650 Fall Time Measured Between 1.3 V and 1.8 V	2–14
12	GTL16612 Fall Time Measured Between 0.5 V and 1 V	2–14
13	FB1650 Rise Time Measured Between 1.3 V and 1.8 V	2–14
14	GTL16612 Rise Time Measured Between 0.5 V and 1 V	2–14
15	FB1650 Signal Integrity at the Receiver Input Using Different-Length Cables	2–15
16	GTL16612 Signal Integrity at the Receiver Input Using Different-Length Cables	2–15
17	Proposed Circuit to Generate V_{REF}	2–16

Introduction

This application report examines the requirements for a low-swing interface in high-speed digital systems and how well this need is addressed by two interface standards: backplane Transceiver Logic (BTL) and Gunning Transceiver Logic (GTL). Both interface standards attempt to improve the performance of high-speed digital systems by reducing the difference between the logic high-voltage level and the logic low-voltage level.

A comparison of various performance criteria, such as power consumption, noise immunity, capacitive loading, speed, and packaging, shows that GTL and BTL provide a compelling solution in both point-to-point and backplane environments. Guidelines for system designs using Texas Instruments (TI) GTL and BTL products are addressed, including associated voltage supplies and proper termination techniques.

Test Setup

The TI GTL16612 and FB1650 were used to study the various performance levels. A backplane-like design has been established to perform the laboratory work supporting this application report. Four boards with 2-in. stubs and 50-Ω interconnecting transmission lines were used to simulate the backplane environment. A 50-MHz frequency was used unless otherwise noted. The output supply voltage (V_{TT}) was supplied through a resistor at each end of the backplane (50-Ω to 1.2 V for GTL and 33-Ω to 2.1 V for BTL) for both families as specified in both IEEE (BTL) and JEDEC (GTL) standards. Figure 1 shows the backplane model with all four boards connected.

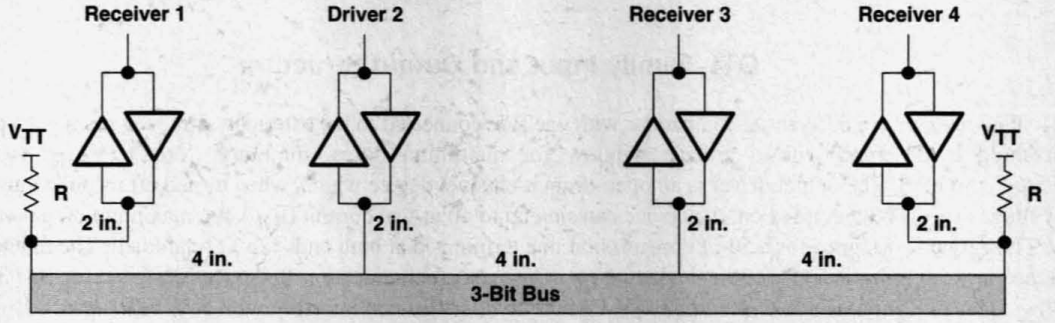


Figure 1. Backplane Model With All Four Boards Connected

Another design has been used to simulate the transmission-environment effect when transferring data across a longer point-to-point transmission line. Figure 2 shows the same backplane model with only one driver and one receiver used to transfer the data across 12-in., 28-in., and 48-in. transmission lines.

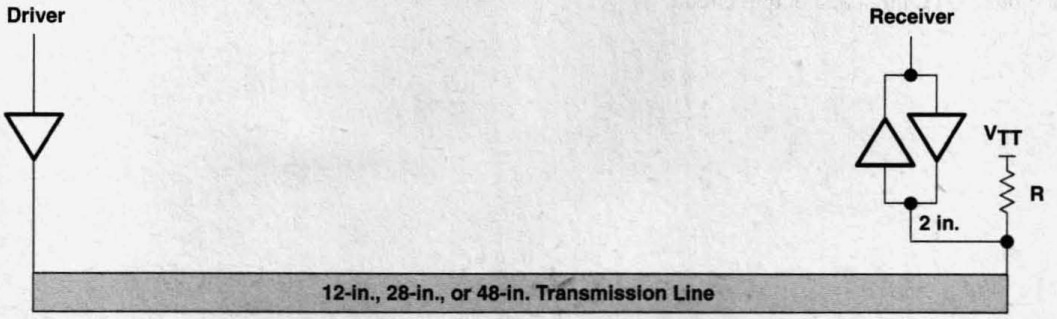


Figure 2. Point-to-Point Model With Only One Driver and One Receiver Connected

Advantages of GTL or BTL Over CMOS/TTL

BTL and GTL were developed to solve the bus-driving problem associated with TTL and to enhance the performance of point-to-point and backplane applications. BTL and GTL also eliminate the need for the extra time required for the TTL signal to settle due to reflection and noise generated when switching. The 1-V swing of both signals versus the 3-V to 5-V swing of TTL and CMOS signals helps reduce the noise generated on the bus when the outputs are switching simultaneously. Table 1 shows the minimum high-level output voltage (V_{OH}) and the maximum low-level output voltage (V_{OL}) of CMOS, TTL, BTL, and GTL signals.

Table 1. V_{OH} and V_{OL} Levels for Various Families

LOGIC LEVEL	V_{OH}min (V)	V_{OL}max (V)
CMOS	3.8	0.44
TTL	2.4	0.55
BTL	2.1	1
GTL	1.2	0.4
GTL+	1.5	0.4

BTL and GTL buffers are designed with minimal output capacitance (5 pF maximum) compared to a TTL output buffer (8 pF to 15 pF typical). A TTL or CMOS output capacitance, coupled with the capacitance of the connectors, traces, and vias reduces the characteristic impedance of the backplane. For high-frequency operation, this phenomenon makes it difficult for the TTL or CMOS driver to switch the signal on the incident wave. A TTL or CMOS device needs a higher drive current than presently available to be able to switch the signal under these conditions. However, increasing the output drive clearly increases the output capacitance. This scenario again reduces the characteristic impedance even more. That is why a lower signal-swing family with reduced output capacitance, such as BTL or GTL, is recommended when designing high-speed backplanes.

GTL Family Input and Output Structure

The GTL input receiver is a differential comparator with one side connected to the externally provided reference voltage, V_{REF}. The threshold is designed with a precise window for maximum noise immunity ($V_{IH} = V_{REF} + 50$ mV and $V_{IL} = V_{REF} - 50$ mV). The output driver is an open-drain n-channel device which, when turned off, is pulled up to the output supply voltage (V_{TT}). When turned on, the device can sink up to 40 mA of current (I_{OL}) at a maximum output voltage (V_{OL}) of 0.4 V. The output is designed for a 50-Ω transmission line terminated at both ends (25-Ω total load). The inputs and outputs are designed to work independently of the device's V_{CC}. They can communicate with devices designed for 5-V, 3.3-V, or even 2.5-V V_{CC}. The TTL input is a 5-V tolerant 3.3-V CMOS inverter that can interface with 5-V TTL signals. Bus hold is also provided on the TTL port to eliminate the need for external resistors when the inputs and outputs are unused or floating. The TTL output is a bipolar output. It is similar to the LVT output structure.[1] At this time, the GTL16612 and GTL16616 devices require two power supplies to function: a 5-V supply ($V_{CC(5)}$) for the GTL and a 3.3-V supply ($V_{CC(3.3)}$) for the LVTTL. The maximum operating frequency of the family is 95 MHz (GTL16612 and GTL16616). The GTL16622 and GTL16923 will operate up to 200 MHz in both directions (GTL to TTL or TTL to GTL) and will have a single 3.3-V power supply.[1] Figure 3 shows a typical GTL input and output circuit.

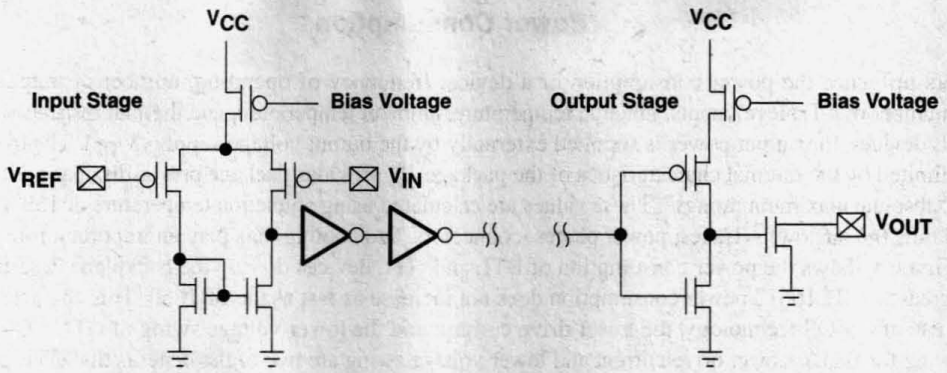


Figure 3. Typical GTL Input and Output Cells

BTL Family Input and Output Structure

The BTL input receiver is a differential amplifier with one side connected to an internal reference voltage. The threshold is designed with a narrow window (V_{IH} = 1.62 V and V_{IL} = 1.47 V). Unlike GTL, BTL requires a separate supply voltage for the threshold circuit to eliminate any noise generated by the switching outputs. The output driver is an open-collector output with a termination resistor selected to match the bus impedance. When the device is turned off, the output is pulled up to the output supply voltage (V_{TT} = 2.1 V typical). The inputs and outputs work independently of the device's V_{CC}. They can communicate with devices designed for 5-V or 3.3-V V_{CC}. The TTL input is a 5-V CMOS inverter, and the output is a bipolar output similar to the ABT output structure.[1] BTL requires three power supplies: the main power supply (V_{CC}), the bias generator supply (BG V_{CC}), and the bias supply voltage (BIAS V_{CC}) that establishes a voltage between 1.62 V and 2.1 V on the BTL outputs when V_{CC} is not connected. The maximum operating frequency of the BTL family is 75 MHz, depending on the application as well as the board layout. Figure 4 shows a typical BTL input and output circuit.

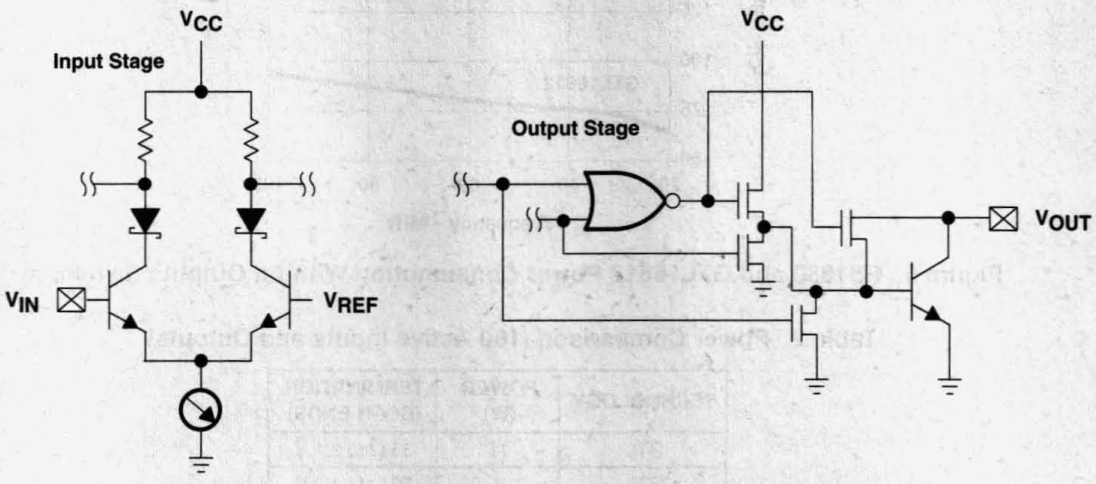


Figure 4. Typical BTL Input and Output Cells

Power Consumption

Several factors influence the power consumption of a device: frequency of operation, number of outputs switching, load capacitance, number of TTL-level inputs, junction temperature, ambient temperature, and thermal resistance of the device. For BTL and GTL devices, the output power is supplied externally by the output voltage supply (V_{TT}). The maximum operating frequency is limited by the thermal characteristics of the package. TI provides package power-dissipation information in data sheets under "absolute maximum ratings". These values are calculated using a junction temperature of 150°C and a board trace length of 750 mils (no airflow).[2] Traces, power planes, connectors, and cooling fans play an important role in improving heat dissipation. Figure 5 shows the power consumption of BTL and GTL devices driving the backplane described above. As the frequency increases, GTL16612 power consumption does not increase as fast as the FB1650. This characteristic is due to the predominant use of CMOS technology, the lower drive current, and the lower voltage swing of GTL (0.8-V swing for GTL versus 1-V swing for BTL). Lower drive current and lower voltage swing are two of the benefits that GTL provides over BTL drivers. A power-consumption comparison (see Table 2) illustrates the advantage of GTL over BTL when 160 active inputs and outputs are switching.[3] Another benefit GTL offers is that the family uses the common 56-pin SSOP and TSSOP packages rather than the 100-pin thin quad flat package (TQFP) with a heat slug mounted above the die in BTL parts. The pin count on the TQFP package is almost twice the pin count of the SSOP or TSSOP packages.

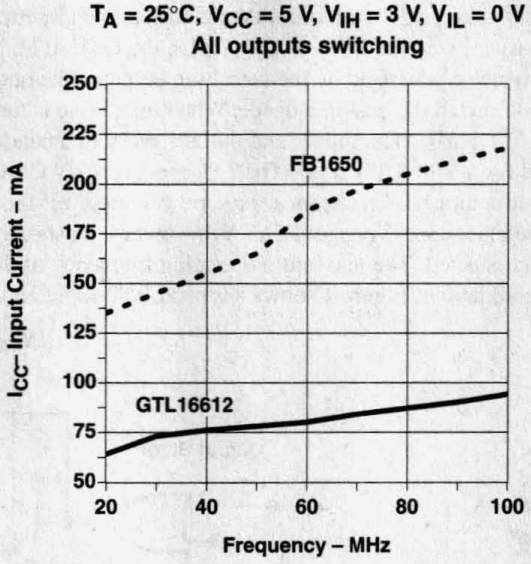


Figure 5. FB1650 and GTL16612 Power Consumption With All Outputs Switching

Table 2. Power Comparison (160 Active Inputs and Outputs)

TECHNOLOGY	POWER (W)	TERMINATION (BOTH ENDS)
BTL	11	33 Ω to 2.1 V
GTL	2	50 Ω to 1.2 V

Simultaneous Switching

In a given digital circuit, there is a large change in current over a very short time when multiple outputs switch simultaneously. As this increased current flows through the bond wires and the leadframe, it develops a voltage across the wire's inductance. This feedback mechanism is known as simultaneous switching noise (SSN). This noise manifests itself as V_{OL} or V_{OH} voltage bounce at the package pin(s).

From basic circuit analysis, the induced voltage across an inductor is defined as:

$$v = L\frac{di}{dt} \quad (1)$$

Where:

L = Inductance
di/dt = Rate of change of the current

The current through an output is dependent on the voltage level and the load at the output, which can be expressed mathematically as:

$$i = C\frac{dv_{out}}{dt} \quad (2)$$

Analysis of equations (1) and (2) clearly shows that because of the lower voltage swing, GTL and BTL offer better noise immunity compared to TTL or CMOS outputs.

As the speed of today's circuits increases, the current rate of change (di/dt) increases and so does the susceptibility to SSN, i.e., voltage bounce (GND and V_{CC}). The standard methodology devised by the industry to measure voltage bounce is to keep one output at either logic high (V_{OH}) or logic low (V_{OL}) and to switch all other outputs at a predefined frequency. Figures 6 through 9 compare both GTL and BTL for noise immunity as 17 outputs are switching simultaneously.

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω

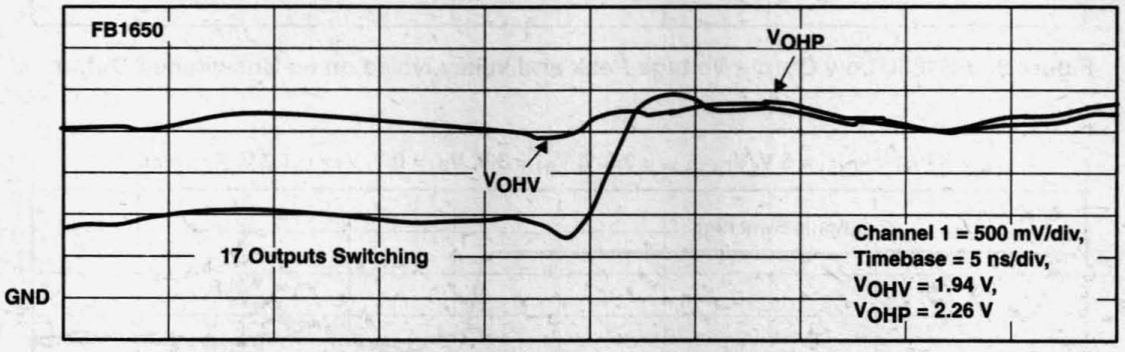


Figure 6. FB1650 High Output Voltage Peak and Valley Noise on an Unswitched Output

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω

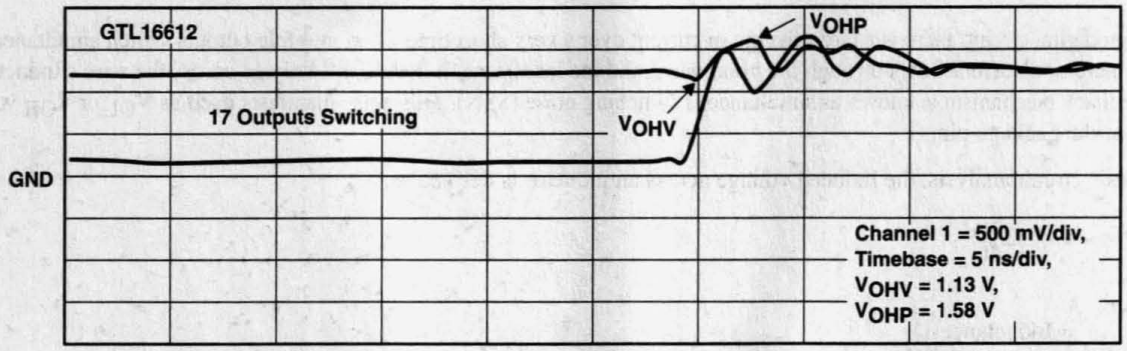


Figure 7. GTL16612 High Output Voltage Peak and Valley Noise on an Unswitched Output

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω

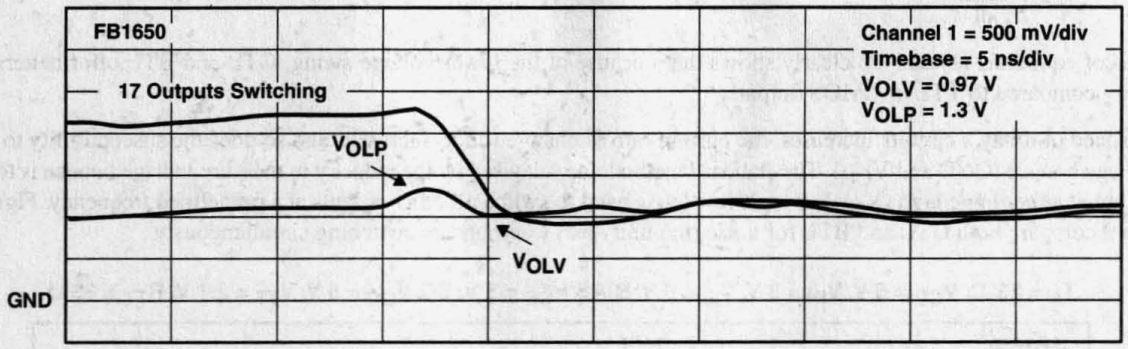


Figure 8. FB1650 Low Output Voltage Peak and Valley Noise on an Unswitched Output

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω

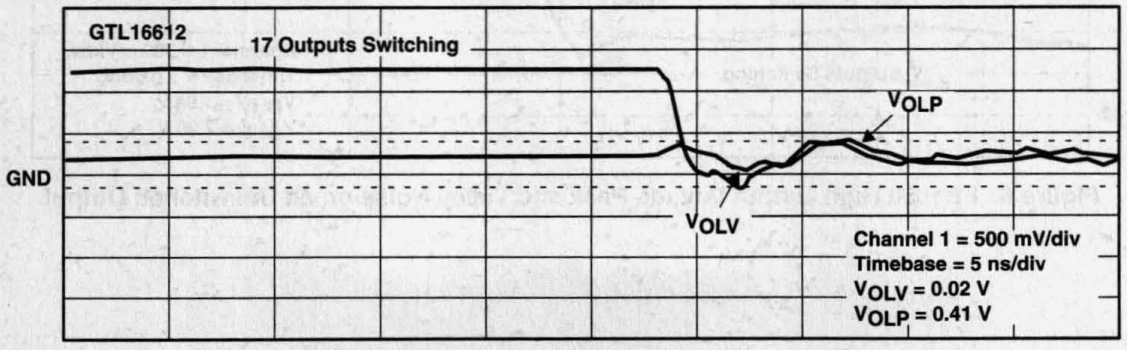


Figure 9. GTL16612 Low Output Voltage Peak and Valley Noise on an Unswitched Output

Output Capacitance

GTL and BTL devices are designed to meet a 5-pF capacitance on their input and output ports (B port). Figure 10 shows the variation of the output capacitance across both processes.

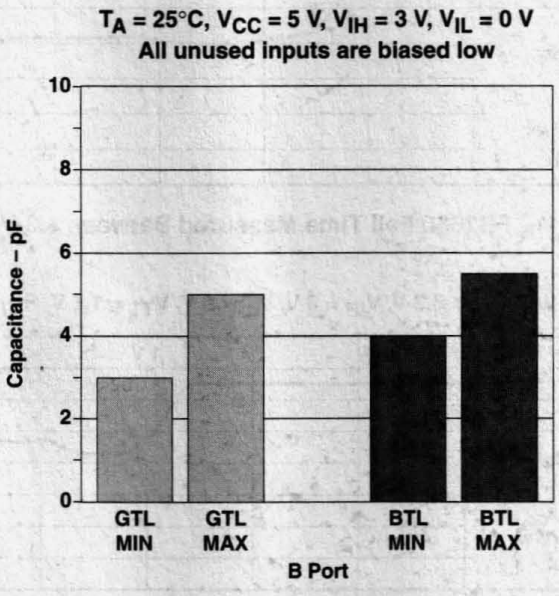


Figure 10. Capacitance Variation Across Process

Slew Rate

Slew rate plays an important role in backplane or point-to-point application designs. The slower the output slew rate of a device, the less susceptible the signal is to reflections and noise. Using the backplane model (see Figures 1 and 2), the output slew rate (t_r and t_f) of the driving device was taken under the following conditions: a 10-in., 50-Ω transmission line and a single termination to V_{TT} at the receiver end. Figures 11 through 14 show the rise and fall times of both devices taken between the two specified voltages of 0.5 V to 1 V for GTL and 1.3 V to 1.8 V for BTL. Both the BTL and GTL slew rates are acceptable.

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω, Frequency = 10 MHz

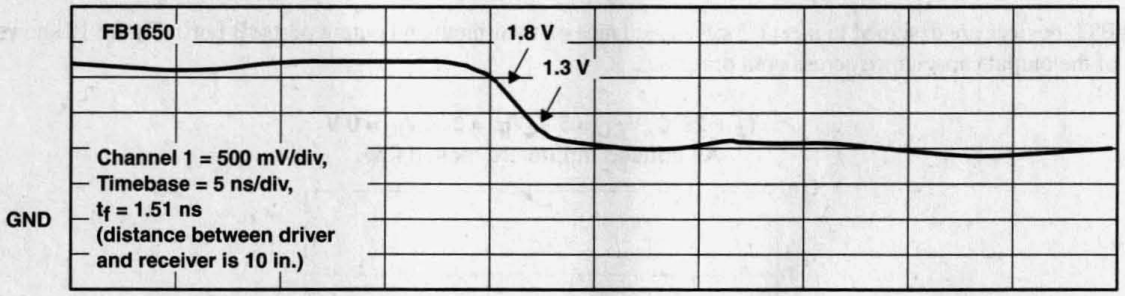


Figure 11. FB1650 Fall Time Measured Between 1.3 V and 1.8 V

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω, Frequency = 10 MHz

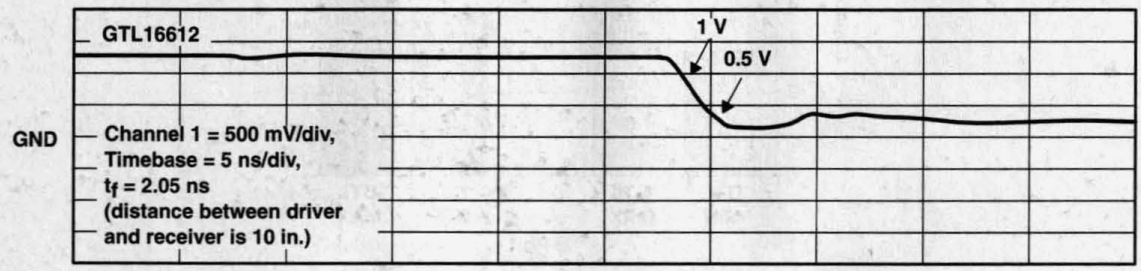


Figure 12. GTL16612 Fall Time Measured Between 0.5 V and 1 V

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω, Frequency = 10 MHz

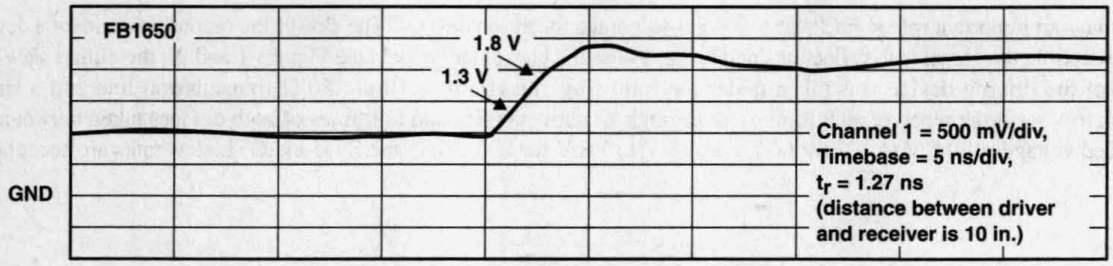


Figure 13. FB1650 Rise Time Measured Between 1.3 V and 1.8 V

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω, Frequency = 10 MHz

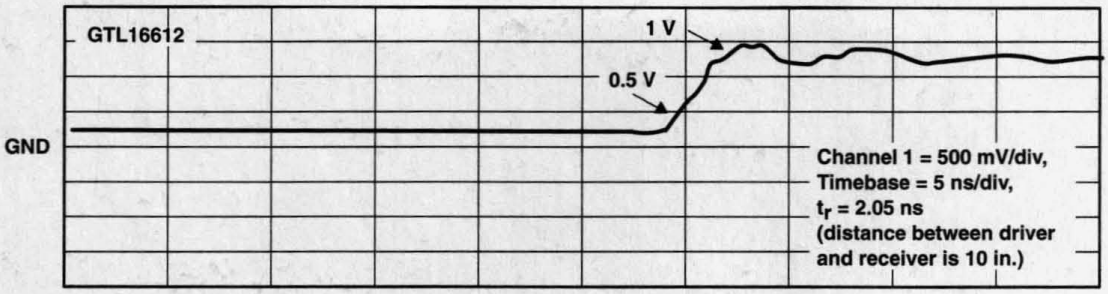


Figure 14. GTL16612 Rise Time Measured Between 0.5 V and 1 V

Signal Integrity

Figures 15 and 16 show the signal integrity of data propagating across the 50-Ω transmission line using three cable lengths (A = 12 in., B = 28 in., and C = 46 in.). The clock frequency is 75 MHz. The measurement was taken at the receiver end of the cable. The GTL output waveform has kept its input square-wave shape better than the BTL waveform has. The cable and the termination resistors used in this laboratory are not precisely matched; that is why a small reflection can be seen on the GTL outputs when switching low to high. In real systems, where both the termination resistor and the traces are matched, these reflections will be reduced.

T_A = 25°C, V_{CC} = 5 V, V_{IH} = 3 V, V_{IL} = 0 V, BIAS V_{CC} = 5 V, BG V_{CC} = 5 V, V_{TT} = 2.1 V, R_{TT} = 33 Ω, Frequency = 75 MHz

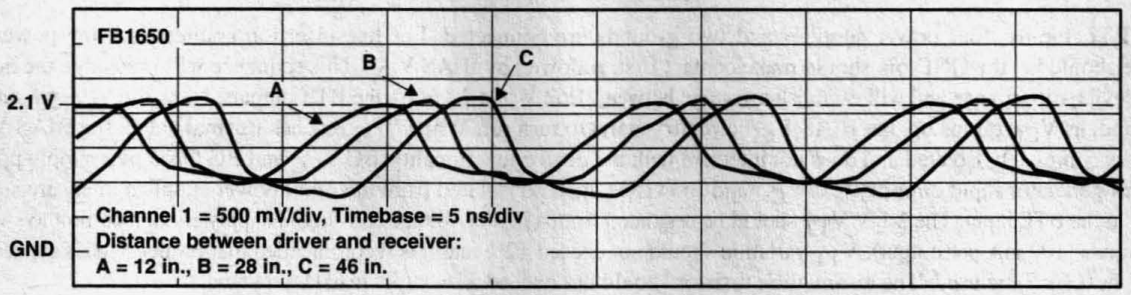


Figure 15. FB1650 Signal Integrity at the Receiver Input Using Different-Length Cables

T_A = 25°C, $V_{CC(5)}$ = 5 V, $V_{CC(3.3)}$ = 3.3 V, V_{IH} = 3 V, V_{IL} = 0 V, V_{TT} = 1.2 V, R_{TT} = 50 Ω, Frequency = 75 MHz

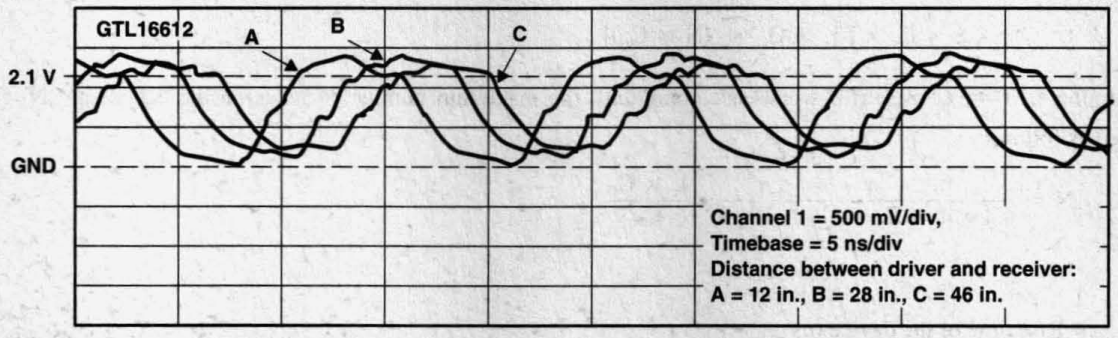


Figure 16. GTL16612 Signal Integrity at the Receiver Input Using Different-Length Cables

Design Considerations

To successfully design with the GTL family, several rules and techniques with regard to voltage generation and proper termination must be followed. First, both 3.3-V and 5-V V_{CC} are needed in the present generation of GTL devices (only the 3.3-V V_{CC} will be needed in the next-generation GTL). Second, the termination voltage (V_{TT}) should be regulated from the 5-V V_{CC}, keeping in mind the current requirements of the outputs (40 mA per output). There are several linear regulators that are capable of performing this function. Depending on the design, the regulator could be either on the backplane itself or on the individual cards. Third, the reference voltage (V_{REF}) must be generated from V_{TT}. The V_{REF} voltage can be generated using a simple voltage-divider circuit with an appropriate bypass capacitor (0.01 µF or 0.1 µF) placed as close as possible to the V_{REF} pin. The V_{REF} input circuitry consumes very little power (1 µA maximum). This enables several devices to have their V_{REF} pin connected to the same voltage-divider circuit, thus eliminating the need for multiple voltage-divider circuits (see Figure 17).

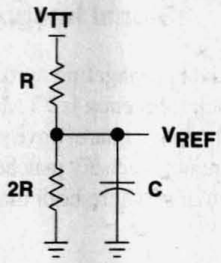


Figure 17. Proposed Circuit to Generate V_{REF}

For the BTL family, four power supplies and two grounds are connected. For live-insertion applications, the power-up sequence should be: the GND pin should make contact first, followed by BIAS V_{CC}. This sequence will precharge the board and the device capacitance and will establish a voltage between 1.62 V and 2.1 V on the BTL outputs. Next, the V_{CC} pin makes contact and, as V_{CC} ramps up, the BIAS V_{CC} circuitry starts to turn off. When V_{CC} reaches its final value, the BIAS V_{CC} circuitry is completely isolated and does not interfere with the device functionality. BG V_{CC} and BG GND pins supply power to the bias generator input circuitry. BG V_{CC} and BG GND must be isolated from the other power supplies to ensure signal integrity at the BTL input. The 2.1-V V_{TT} should be regulated from a higher voltage and should supply enough current to switch all 18 outputs (100 mA per output). V_{TT} variation should not exceed ±2% and it is recommended that proper bypass capacitors (0.01 µF or 0.1 µF) be used. The termination resistor should not exceed ±1% of its resistance value.

Table 3 gives the designer an estimate of the maximum number of loads allowed when designing with GTL and BTL families.[4] Note that crosstalk and poor board layout can degrade the overall quality of the backplane, thereby affecting the number of loads.

Using the formula:

$$t_r,\ t_f = 2.2 \times Z_S \times [(L \times C_O) + (N \times C_N)] \quad (3)$$

and assuming $t_r,\ t_f = t_p = \frac{1}{2f}$ (for worst-case condition), the maximum number of loads on the backplane (N) can be calculated as follows:

$$N = \frac{1}{4.4 \times f \times Z_S \times C_N \times 10^{-6}} - \frac{L \times C_O}{C_N} \quad (4)$$

Where:

t_r = Rise time of the device (ns)
t_f = Fall time of the device (ns)
Z_S = Output impedance of the source (Ω), 25 Ω for GTL, 16.5 Ω for BTL
C_O = Characteristic capacitance per unit length of the transmission line (pF/in.) (see Table 3)
L = Length of the backplane (in.)
N = Maximum number of loads on the backplane
C_N = Capacitance for each load (pF), 5 pF for the device, 5 pF for the connector
t_p = Pulse width of the signal (ns)
f = Frequency of the signal on the backplane (MHz)

Table 3. Typical Strip-Line Characteristics†

DIMENSIONS (mils)			LINE IMPEDANCE Z_O (Ω)	CAPACITANCE C_O (pF/in.)	t_{pd} (ns/in.)	MAXIMUM NUMBER OF LOADS		
						GTL		BTL
T	H	W				L = 12 in.	L = 16 in.	L = 24 in.
1.5	6	20	27	6.67	0.18	10	8	12
1.5	6	15	32	5.83	0.186	11	9	14
1.5	10	20	34	5.58	0.189	11	9	14
1.5	12	20	37	4.75	0.176	12	11	16
1.5	10	15	40	4.67	0.187	13	11	16
1.5	12	15	43	4	0.172	13	12	18
1.5	20	20	44	4	0.176	13	12	18
1.5	20	15	51	3.5	0.179	14	13	19
1.5	30	20	55	3.25	0.179	14	13	20
1.5	30	15	61	2.92	0.178	15	14	21

† The characteristic impedance of the strip line is based on the following:
er = 5, relative dielectric constant of the board material (G10 glass epoxy)
H = thickness of the insulation dielectric
T = cross-sectional length of the strip line
W = cross-sectional width of the strip line
Frequency of the signal on the backplane is 50 MHz.

Summary

Today's high-speed backplane and point-to-point applications require devices that can provide high performance, excellent signal integrity, and cost effectiveness. GTL and BTL transceivers are designed to meet these characteristics. Both transceiver families show similar skew, slew rate, and SSN performance. BTL is generally used for heavily loaded backplanes (100-mA I_{OL}) and for frequencies less than 75 MHz. However, the laboratory data presented in this report show that GTL is more suitable for designs that require high performance (up to 100 MHz for the GTL16612 and GTL16616 and 200 MHz for the GTL16622 and GTL16923) and low power consumption at low cost and minimum board space.

References

1. Texas Instruments Incorporated, *ABT Advanced BiCMOS Technology Data Book,* 1994, literature number SCBD002B.
2. Texas Instruments Incorporated, "Package Thermal Considerations", *ABT Advanced BiCMOS Technology Data Book,* 1994, literature number SCBD002B, pg. 13–97.
3. Gunning, Bill; Yuan, Leo; Nguyen, Trung; Wong, Tony, *GTL: A Low-Voltage Swing Transmission Line Transceiver,* March 15, 1991.
4. Texas Instruments Incorporated, *Advanced Schottky Load Management,* 1987, literature number SDAA006.

Next-Generation BTL/Futurebus Transceivers Allow Single-Sided SMT Manufacturing

SCBA003C
March 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**2–23**
Current Generation of BTL/Futurebus Transceivers	**2–23**
A New Generation of BTL/Futurebus Transceivers	**2–27**
Summary	**2–30**

List of Illustrations

Figure	*Title*	*Page*
1	Comparison of TTL and BTL Switching Standards	2–23
2	Slew-Rate Control (OEC™) Diagram	2–24
3	Uncached 64-Bit Futurebus Layout With Texas Instruments Controller Chipset and Today's Most Integrated Transceivers	2–25
4	Functional Differences Between FB2040 Control Transceiver and FB2031 Address/Data Transceiver	2–26
5	Cross Section of Thermally Enhanced EIAJ 100-Pin TQFP	2–27
6	Functional Circuit Diagram of FB1650	2–28
7	Uncached 64-Bit Futurebus Layout With Texas Instruments Chipset and FB16xx Transceivers	2–29

OEC and UBT are trademarks of Texas Instruments Incorporated.

Introduction

BTL (IEEE 1194.1-1991) and Futurebus designs offer significant performance advantages over conventional TTL backplane implementations, but these advantages come with trade-offs. Switching noise in the form of ground bounce and EMI must be controlled, and proper termination schemes must be employed to ensure signal integrity in this high-speed switching environment. Trade-offs for price in the form of total system solution versus overall system performance are also of concern. This paper begins with the historical perspective on signal-integrity issues addressed by the IEEE and follows with new pioneering bus-interface solutions to help reduce overall BTL or Futurebus system costs and design complexities.

Current Generation of BTL/Futurebus Transceivers

A number of suppliers have developed BTL and Futurebus transceiver solutions that comply with IEEE 1194.1. These devices share the same reduced output swing and tight switching thresholds shown in Figure 1 and a slew-rate control (see Figure 2). The various devices differ considerably in wafer-fab process technology, propagation-delay performance, and other performance metrics (see Table 1).

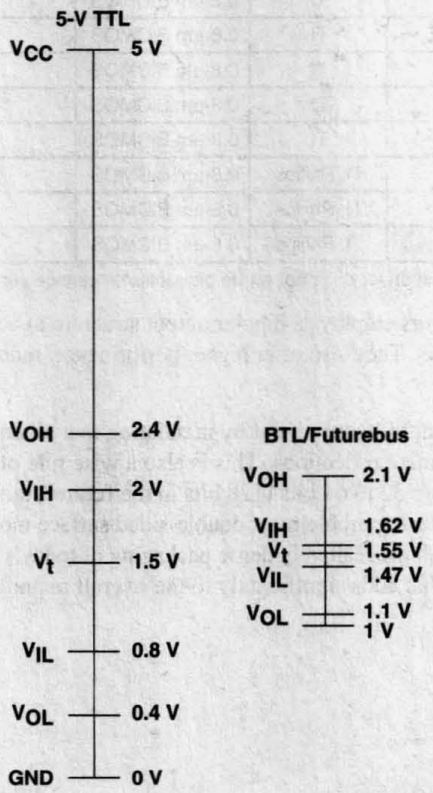


Figure 1. Comparison of TTL and BTL Switching Standards

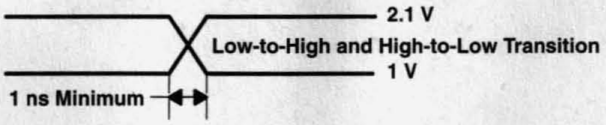


Figure 2. Slew-Rate Control (OEC™) Diagram

Table 1 shows an evolutionary progression in bipolar wafer-fab technology and improved propagation-delay performance. Bipolar fab technologies are chosen for this class of device for their high drive capability, low switching noise, and relative ease of designing (relative to pure CMOS) the analog circuitry required to meet the slew-rate control requirement (see Figure 2). Bipolar circuits have the disadvantage of relatively high power dissipation. The heat generated by this high power dissipation, coupled with the large switching currents coming from the bus termination, place a thermal limitation on the numbers of bits that can be integrated into a single, standard integrated-circuit package (typically, only four bits).

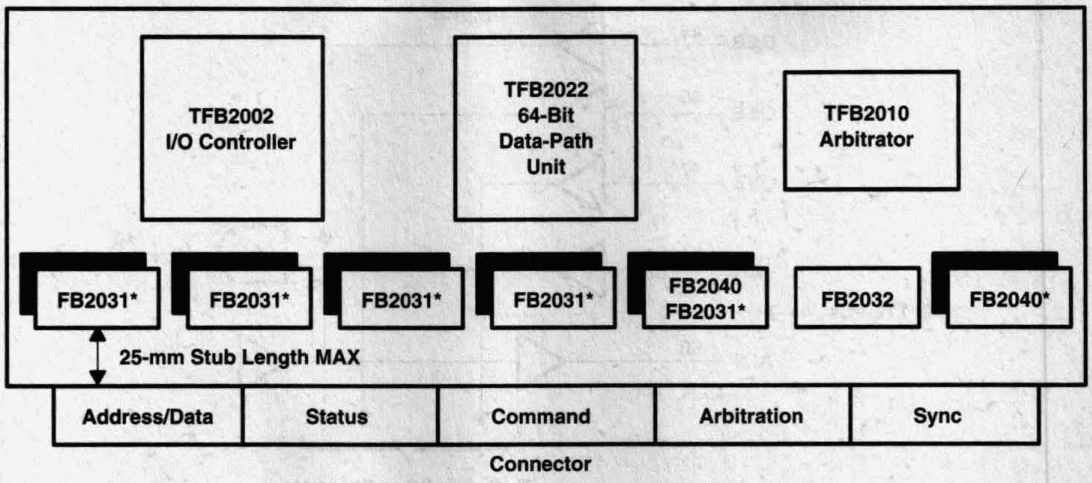
Table 1. BTL/Futurebus Transceiver Offering Available Today

TRANSCEIVER	SUPPLIER	TECHNOLOGY	BITS/PACKAGE	t_{pd} (ns)
ALS056/057	TI, NSC	3-µm Bipolar	4/8	20
DS3890	NSC	2-µm Bipolar	8†	15
DS3896/7	NSC	1.5-µm Bipolar	4/8	12
DS3893A	NSC	1.2-µm Bipolar	4	7
FB1650	TI	0.8-µm BiCMOS	18	7.2
FB1651	TI	0.8-µm BiCMOS	17	7.2
FB1653	TI	0.8-µm BiCMOS	17	6.6
FB2032	TI	0.8-µm BiCMOS	9	8.3
FB2033A	TI	0.8-µm BiCMOS	8	5.6
FB2031	TI, Philips	0.8-µm BiCMOS	9	6.6
FB2040	TI, Philips	0.8-µm BiCMOS	8	6.5
FB2041A	TI, Philips	0.8-µm BiCMOS	7	5.6

† Unidirectional driver only; not a true bidirectional transceiver

The newer class of BiCMOS transceivers employs a bipolar output structure to achieve the desired drive, noise, and slew-rate control of previous-generation products. They also offer higher performance, much lower power dissipation, and take the next step toward higher integration.

Futurebus adds an additional constraint to board layout by mandating that all compliant cards have a maximum stub length of 25 mm to reduce loading and minimize reflections. This is also a wise rule of thumb for non-BTL/Futurebus designs. As data paths have increased in width from 32 to 64 bits (128 bits in the future), this stub-length requirement has forced system designers to wrestle with the manufacturing problems of double-sided surface mounting of the transceivers on boards as large as 12 Standard Units (12SU). Even with the relatively dense packaging of today's fastest and most integrated transceivers, this can be a formidable design problem that adds significantly to the overall manufacturing cost of a board (see Figure 3).



NOTE: The second-part type descriptor (*) indicates that a second transceiver is mounted on the opposite side of the board.

Figure 3. Uncached 64-Bit Futurebus Layout With Texas Instruments Controller Chipset and Today's Most Integrated Transceivers

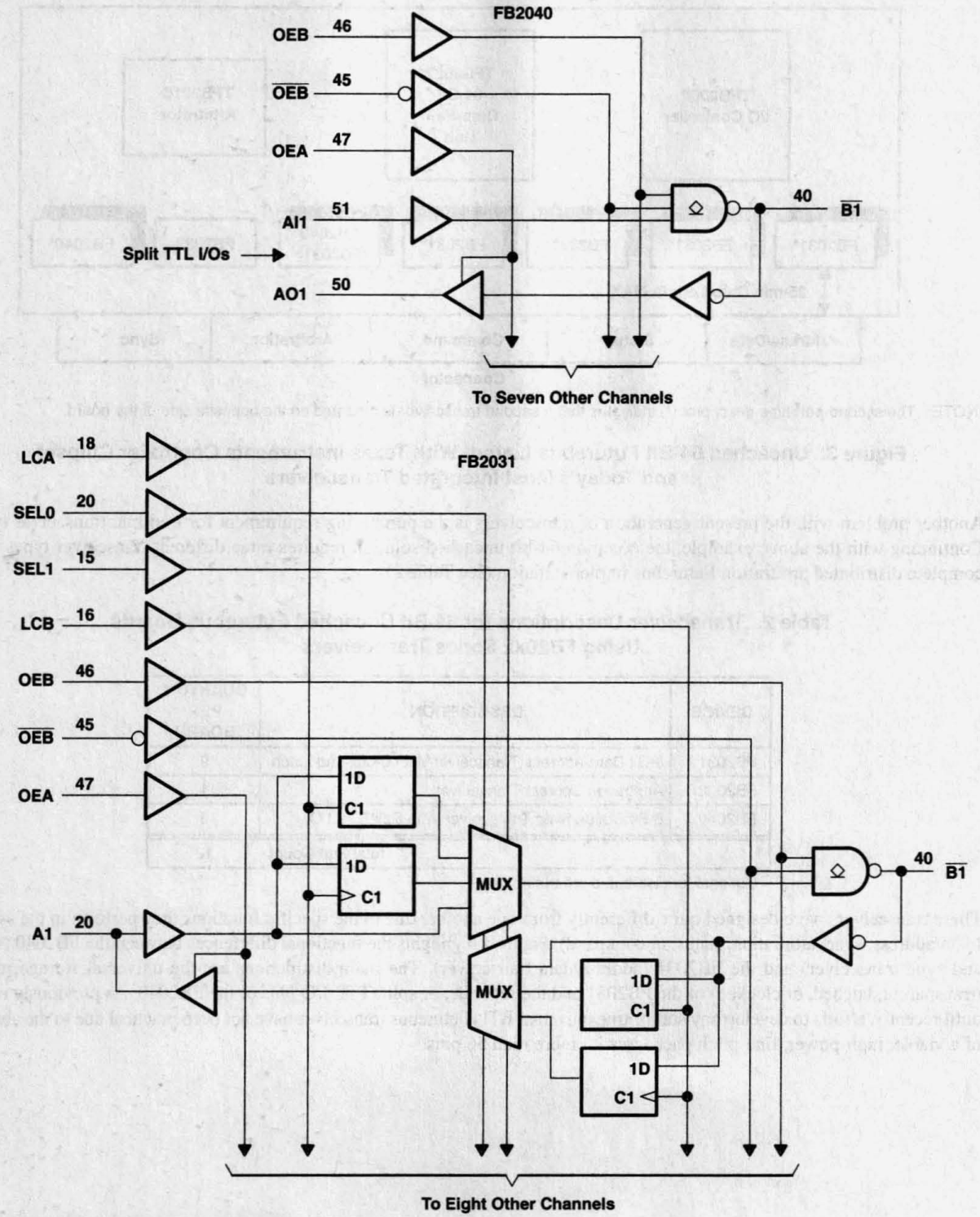
Another problem with the present generation of transceivers is the purchasing requirement for multiple transceiver types. Continuing with the above example, the common 64-bit uncached solution requires three different transceiver types for a complete distributed arbitration Futurebus implementation (see Table 2).

Table 2. Transceiver Descriptions for 64-Bit Uncached Futurebus Boards Using FB20xx Series Transceivers

DEVICE	DESCRIPTION	QUANTITY PER BOARD
FB2031	9-Bit Data/Address Transceiver With Clock and Latch	9
FB2032†	Arbitration Contest Transceiver	1
FB2040	8-Bit Status/Sync Transceiver With Split TTL I/O	3
	Total Part Count	13

† Optional for distributed arbitration only

These transceivers were designed quite differently from one another due to the specific functions they perform in the system (data/address, sync, arbitration, status, or command). Figure 4 highlights the functional differences between the FB2040 (status and sync transceiver) and the FB2031 (address/data transceiver). The main distinctions are the universal storage modes (transparent, latched, or clocked) of the FB2031 and the separate, or split, TTL I/O pins of the FB2040. As previously noted, until recently, efforts to develop any sort of true universal BTL/Futurebus transceiver have not been practical due to the absence of a viable, high-power, fine-pitch package with more than 56 pins.



Pin numbers shown are for the RC package.

Figure 4. Functional Differences Between FB2040 Control Transceiver and FB2031 Address/Data Transceiver

A New Generation of BTL/Futurebus Transceivers

In response to the need for single-sided surface mounting and simplified transceiver architectures, Texas Instruments has developed both a high-power package and a series of 18-channel BTL/Futurebus universal bus transceivers (UBT™). These new devices, designated as the FB16xx series, are packaged in a high-power version of the EIAJ standard 100-pin TQFP package (0.5-mm lead pitch). A package cross section, as shown in Figure 5, reveals a metal heatsink that facilitates the excellent thermal performance of the package. Refer to *Thermal Characteristics of SLL Packages and Devices*, literature number SCZA005, for θ_{JA} and reliability issues.

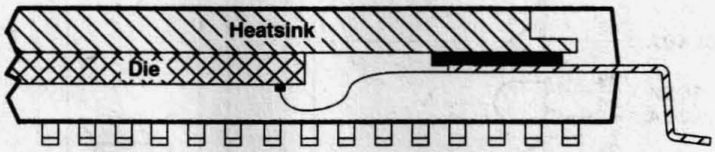
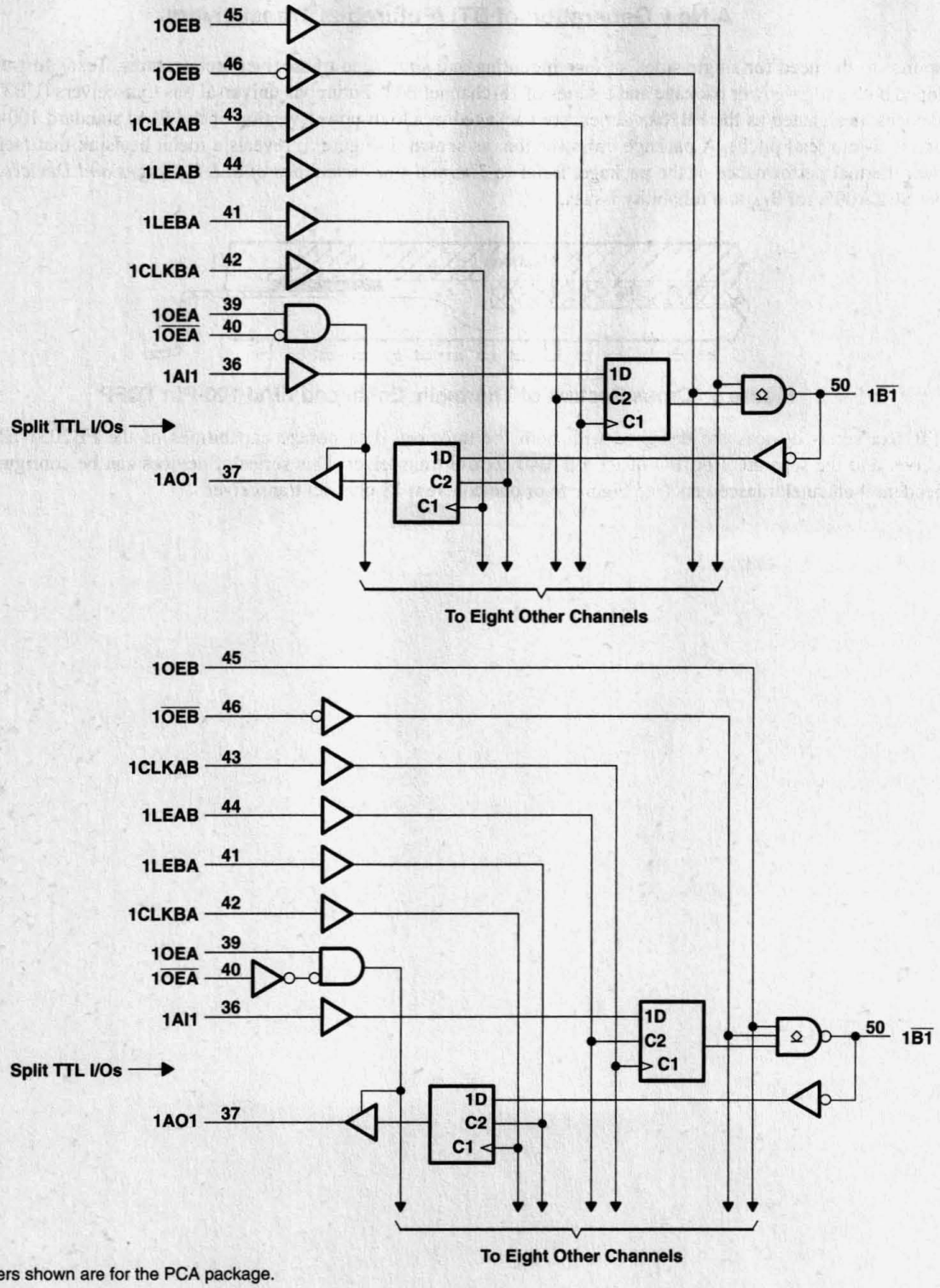


Figure 5. Cross Section of Thermally Enhanced EIAJ 100-Pin TQFP

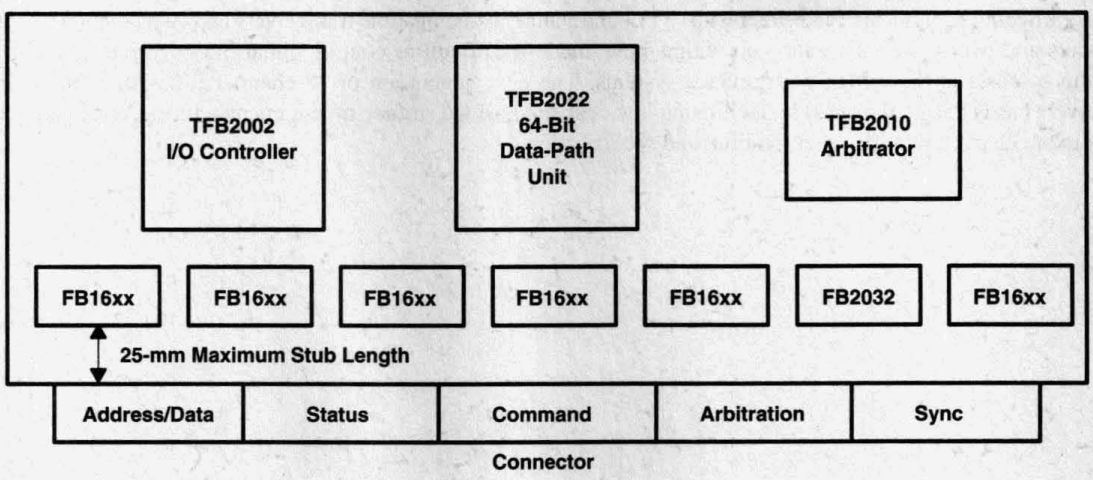
The FB16xx series devices are designed with both the universal data-storage capabilities of the FB2031 address/data transceiver and the separate TTL I/O of the FB2040 control transceiver. This series of devices can be configured as two independent 9-channel transceivers (see Figure 6) or one coherent 18-channel transceiver.



Pin numbers shown are for the PCA package.

Figure 6. Functional Circuit Diagram of FB1650

This flexible design approach eliminates the need for double-sided surface mounting, along with all of the associated manufacturing costs, and still meets the IEEE 896.2-1991 25-mm maximum-stub-length requirement (see Figure 7).



NOTE: There is no double-sided SMT requirement.

Figure 7. Uncached 64-Bit Futurebus Layout With Texas Instruments Chipset and FB16xx Transceivers

In addition, the 18-channel architecture lends itself naturally to reduced pin-to-pin signal skew. Advanced BiCMOS circuit design techniques have improved propagation-delay performance over the previous generation of BiCMOS transceivers. Table 3 shows a transceiver description for the same 64-bit uncached Futurebus example considered previously (see Table 2).

Table 3. Transceiver Descriptions for 64-Bit Uncached Futurebus Board Using FB16xx Series Transceivers

DEVICE	DESCRIPTION	QUANTITY PER BOARD
FB16xx	18-Bit TTL/BTL UBT With Split TTL I/O	6
FB2032†	Arbitration Contest Transceiver	1
	Total Part Count	7

† Optional for distributed arbitration only

This is nearly a 50% reduction in component count and approximately 15% in cost savings on the transceivers alone. Significant savings (tens of dollars per board) in manufacturing costs also are realized by moving to single-sided SMT manufacturing. Other members of the FB16xx family include system clock-distribution features that lend themselves to more specific end-system applications such as ATM hubs and routers (see Table 4).

Table 4. Transceiver Descriptions for Other Members of the FB16xx Series

DEVICE	DESCRIPTION
FB1650	18-Bit TTL/BTL UBT With Split TTL I/O
FB1651	17-Channel UBT With Separate Buffered and Delayed Clock Bit
FB1653	17-Channel UBT With Separate Buffered Clock Bit (variable delay lines)

Summary

The high-speed data-communication requirements of today's fastest board-level computers and telecommunications and network switching equipments can be met with BTL- and Futurebus-compatible transceivers and switching levels. Stub-length constraints and ever-increasing data-path widths have made it difficult to control signal integrity and manufacturing and procurement costs in these high-performance systems. The next generation of 18-channel BTL/Futurebus universal bus transceivers meets this market need by facilitating low-cost single-sided surface-mount manufacturing, and single-device-type procurement, characterization, qualification, and specification.

The Bergeron Method

A Graphic Method for Determining Line Reflections in Transient Phenomena

SDYA014
October 1996

Texas Instruments

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title *Page*

Abstract **2–35**

1 Introduction **2–35**

2 Derivation of Method **2–35**

3 Ideal Voltage Source **2–37**
3.1 Turning On an Ideal Voltage Source (Open Circuit at End of Line) 2–37
3.2 Turning On an Ideal Voltage Source (Short Circuit at End of Line) 2–39

4 Real Voltage Sources **2–40**
4.1 Turning On a Real Voltage Source 2–40
4.1.1 Terminated Line 2–40
4.1.2 Unterminated Line 2–42
4.1.3 Matching 2–44
4.2 Turning Off a Line 2–45
4.3 Switching a Line 2–46

5 Bergeron Method With Nonlinear Line Terminations **2–47**
5.1 Gate Configuration Without Matching 2–48
5.1.1 Low-to-High Transition 2–49
5.1.2 High-to-Low Transition 2–50
5.2 Transmission Lines With Line Termination 2–50
5.3 Split Termination 2–51
5.4 Nonideal Matching 2–52
5.5 Matching by Series Resistor 2–54

Acknowledgment **2–54**

Appendix **2–55**

Bergeron Diagrams **2–55**
No Line Termination (Figures 42, 43) 2–55
Line Termination by Resistor to Ground (Figure 44) 2–56
Line Termination by Series Resistor in the Driver Output (Figure 45) 2–57
Line Termination by Resistor Network (Split Termination) (Figures 46 and 47) 2–57

List of Illustrations

Figure *Title* *Page*

1 Wave Propagation Along a Line 2–35
2 Wave Propagation 2–36
3 Function of Current and Voltage 2–36
4 Ideal Voltage Source and Open-Circuit Line 2–37
5 Voltage Current Diagram 2–37
6 Bergeron Diagram 2–38
7 Potential Gradient at Beginning and End of Line 2–38
8 Ideal Voltage Source and Short-Circuited Line 2–39
9 Bergeron Diagram for Short-Circuited Line 2–39
10 Potential Gradient for Short-Circuited Line at Beginning and End of Line 2–40
11 Current Form for Short-Circuited Line at Beginning and End of Line 2–40

List of Illustrations (continued)

Figure	*Title*	*Page*
12	Real Voltage Source and Terminated Line	2–41
13	Line in Steady-State Condition	2–41
14	Line Reflections for Terminated Line	2–41
15	Voltage and Current for Open-Circuit Line	2–41
16	Terminated Line ($R_O < Z_O < R_t$)	2–43
17	Open-Circuit Line ($R_O < Z_O < R_t$)	2–43
18	Terminated Line ($R_O < Z_O$)	2–44
19	Line Termination by Matching Generator Source Impedance	2–44
20	Line Termination by Terminating Impedance at the Line End	2–44
21	Turning Off a Line	2–45
22	Line Reflections When Turning Off a Line	2–45
23	Switching a Line	2–46
24	Line Reflections When Switching a Line ($Z_O > R_t$)	2–46
25	Line Reflections When Switching a Line ($Z_O < R_t$)	2–47
26	Definition of Current and Voltage Senses	2–47
27	Input and Output Characteristics of AS/TTL Circuits	2–48
28	Transmission Line Without Matching	2–48
29	Bergeron Diagram for Transmission Line Between SN74AS000 TTL Circuits	2–49
30	Line Reflections (Low-to-High Transition)	2–49
31	Line Reflections (High-to-Low Transition)	2–50
32	Measured Line Reflections (Line Length = 3 m, $Z_O = 50\ \Omega$)	2–50
33	Termination of Line With a Resistor	2–51
34	Characteristic of Line Termination	2–51
35	Signal Response for Matched Line	2–51
36	Line Termination by Voltage Divider (Split Termination)	2–52
37	Characteristic of Line Termination by Voltage Divider (Split Termination) and Clamping Diode	2–52
38	Typical Noise Margin of TTL Circuits	2–53
39	Line Reflections for Mismatch of 50% ($\rho = 0.2$)	2–53
40	Termination of Bidirectional Bus Lines	2–54
41	Driver Characteristics for Matching by Series Resistor	2–54
42	Line Without Termination (Low-to-High Transition, $Z_O = 100\ \Omega$)	2–55
43	Line Without Termination (High-to-Low Transition, $Z_O = 100\ \Omega$)	2–56
44	Line Termination by Resistor to Ground, Ideal Matching ($R_t = Z_O = 100\ \Omega$)	2–56
45	Line Termination by Series Resistor at the Generator Output ($Z_O = 100\ \Omega$)	2–57
46	Line Termination by Resistor Network (Low-to-High Transition, $Z_O = 100\ \Omega$)	2–58
47	Line Termination by Resistor Network (High-to-Low Transition, $Z_O = 100\ \Omega$)	2–58

Abstract

The user of modern, fast, logic systems must consider the effect of line reflections very closely. This report describes the Bergeron method of determining line reflections, then illustrates some typical examples of its use and the results it produces.

1 Introduction

The engineer designing fast digital systems must consider the response of electric signals on circuit lines very closely to avoid interference caused by signal distortions. Applications of familiar mathematic methods of line-transmission theory are limited in determining line reflections because the nonlinear input and output characteristics of digital circuits are difficult to represent in mathematical terms.

In transient phenomena on lines with defined characteristic impedances, it is simple to show the response of current and voltage as a function of time, at the beginning and end of a circuit line, in graphic form. This method is particularly suitable for the nonlinear line terminations used in digital engineering.

2 Derivation of Method

A transient phenomenon propagates (see Figure 1) along a line (A, B) in the form of a forward (v_f, i_f) and reflected (v_r, i_r) voltage and current waves as follows:

$$v_{(x,t)} = v_f + v_r \tag{1}$$

$$i_{(x,t)} = i_f + i_r \tag{2}$$

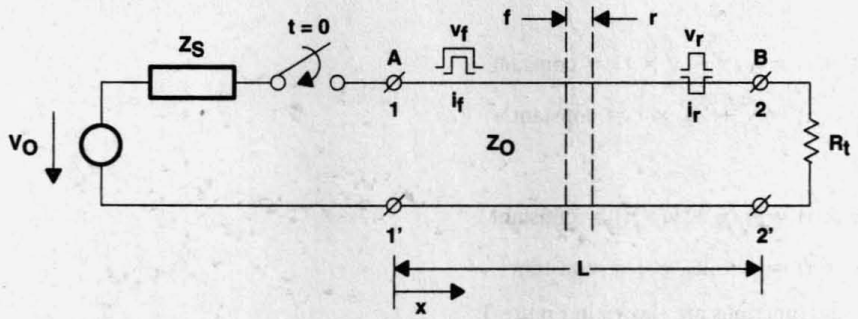


Figure 1. Wave Propagation Along a Line

The ratio of voltage to current for the traveling waves is the characteristic impedance, and the negative sign of reflected waves stems from the reversed current sense of i_r as follows:

$$Z_o = \frac{v_f}{i_f} \tag{3}$$

$$Z_o = \frac{v_r}{-i_r} \tag{4}$$

Equations 1 through 4 produce:

$$v + Z_o \times i = v_f + v_r + Z_o \times (i_f + i_r) = 2v_f(x - v \times t) \tag{5}$$

$$v - Z_o \times i = v_f + v_r - Z_o \times (i_f + i_r) = 2v_r(x + v \times t) \tag{6}$$

Whereby:

$$v = \frac{1}{\sqrt{L'C'}} \quad \text{(velocity of traveling waves)} \tag{7}$$

$$Z_O = \sqrt{\frac{L'}{C'}} \quad \text{(characteristic impedance)} \tag{8}$$

Where:

L'	=	inductance per unit of line length (nH/m)
C'	=	capacitance per unit of line length (pF/m)
$(x - v \times t)$	=	delay parameter for forward wave (f)
$(x + v \times t)$	=	delay parameter for reflected wave (r)

If an observer moves with the forward or reflected wave (i.e., observer and wave are equally fast), Figure 2 applies to the delay parameters.

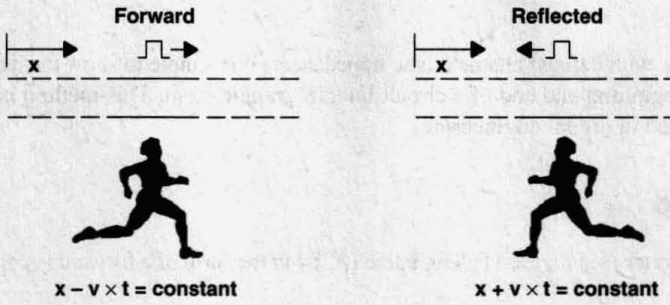


Figure 2. Wave Propagation

If the delay parameters are constant, this also applies to their functions as follows:

Forward

$$f(x - v \times t) = v_f(x - v \times t) = \text{constant} \tag{9}$$

$$f(x - v \times t) = v + Z_O \times i = \text{constant} \tag{10}$$

Reflected

$$f(x + v \times t) = v_f(x + v \times t) = \text{constant} \tag{11}$$

$$f(x + v \times t) = v - Z_O \times i = \text{constant} \tag{12}$$

The straight lines of the functions are shown in Figure 3.

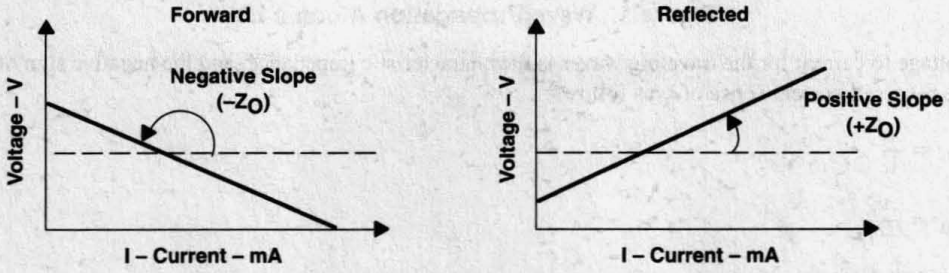


Figure 3. Function of Current and Voltage

The constants of the functions define the location of the straight lines. They are determined by the boundary conditions of the transient phenomenon. In movement with the wave, all operating values for current and voltage of the straight lines are passed through. The values for current and voltage, at the beginning or end of the line, are given by the points of intersection of the conditional straight lines with the characteristics of the line terminations (impedance and generator characteristics).

3 Ideal Voltage Source

3.1 Turning On an Ideal Voltage Source (Open Circuit at End of Line)

To begin with, consider a case in which an ideal voltage source (V_O) (source impedance = 0 Ω) is connected to a loss-free line with the characteristic impedance (Z_O) unterminated at the end (open circuit). Of course, this case is not found in actual practice because there are neither ideal voltage sources nor loss-free lines. Nevertheless, it clearly shows the influence of line reflections on signal shape in extreme cases.

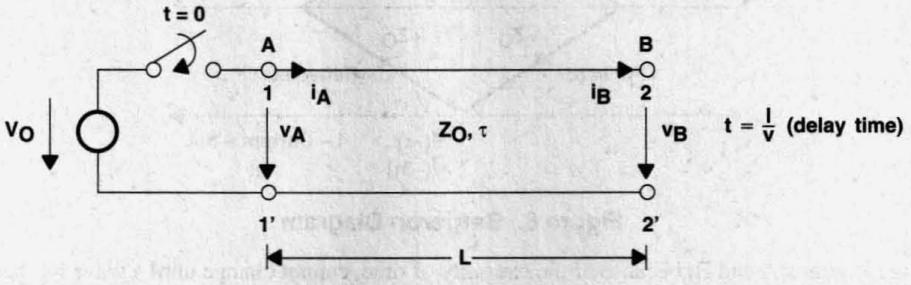


Figure 4. Ideal Voltage Source and Open-Circuit Line

To obtain the potential gradients at the beginning and end of the line, first enter (as shown in Figure 5) the generator characteristic (parallel to the I axis because source impedance = 0 Ω) and the characteristic of the line termination (coincides with the V axis because the line is open circuit). Then determine the state of the line before switching. Enter the values for voltage and current at the end of the line at the point in time $t < 0$ (in this case, the intersection of the V and I axes). These values define the starting point of reflection to the beginning of the line (Bergeron straight line) as follows:

Starting point

$$v_{B(t<0)} = 0 \tag{13}$$

$$i_{B(t<0)} = 0 \tag{14}$$

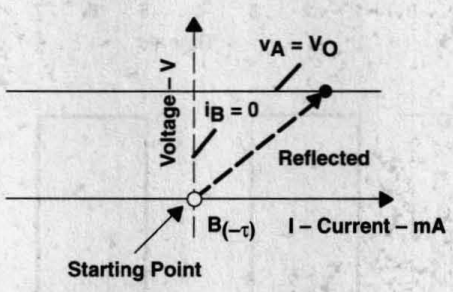


Figure 5. Voltage Current Diagram

Through this point draw a straight line with the slope Z_O (see Figure 6). The intersection of the straight line with the generator characteristic produces the voltage and current value at the beginning of the line at the point in time $t = 0$.

Ideal voltage source

$$v_A = V_O \tag{15}$$

$$i_A = \frac{V_O}{Z_O} \tag{16}$$

Through this point again draw a straight line with the slope $-Z_O$ (see Figure 6). The intersection of the line with the characteristic of the line termination produces the voltage and current value at the end of the line, when the electric wave has reached the end of the line. The line is open circuit, so the voltage that appears at its end is twice that which is at the beginning of the line (the current is 0). To continue, draw straight lines with the slope Z_O and $-Z_O$ through the respective points that have been defined. This obtains the voltage and current values at the end of the line at the points in time 1τ, 3τ, 5τ, etc., plus the corresponding values for the beginning of the line at the points in time 0τ, 2τ, 4τ, etc. In this particular case, the straight lines meet to form a parallelogram, which means that the line is not in a stationary state at any time.

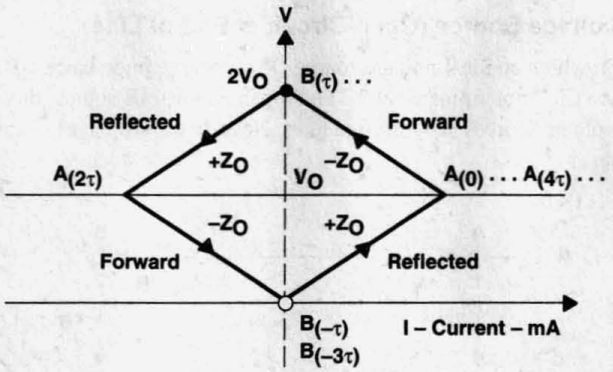


Figure 6. Bergeron Diagram

Current and voltage at points A and B, because of the causality of time, cannot change until a wave has been forwarded and reflected (2τ). Consequently, current and voltage take on a rectangular form (staircase, pulses). Since no energy is consumed at the end of the line, the wave is fully reflected. The forward and reflected waves are superimposed on one another and add to form double the amplitude $2 \times V_O$. The source impedance of the ideal voltage source ($0\ \Omega$) also prevents breakdown of the wave energy. This case results in an undamped rectangular oscillation at the end of the line with amplitude $2 \times V_O$ and period 4τ (see Figure 7).

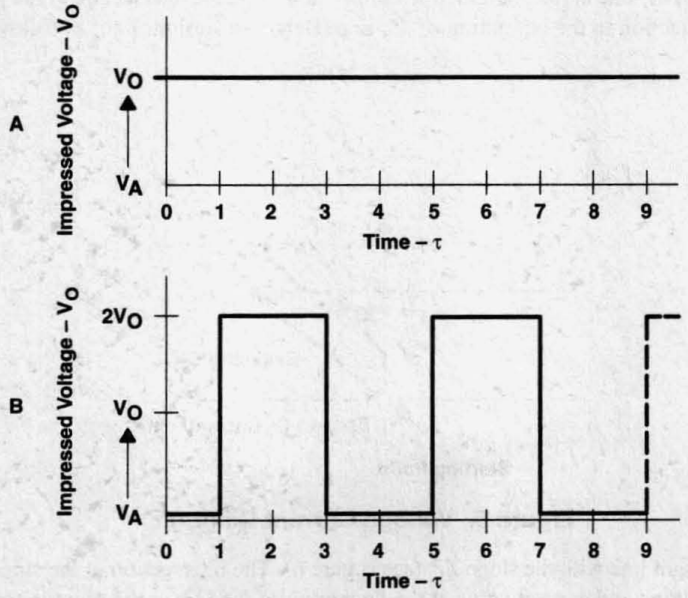


Figure 7. Potential Gradient at Beginning and End of Line

3.2 Turning On an Ideal Voltage Source (Short Circuit at End of Line)

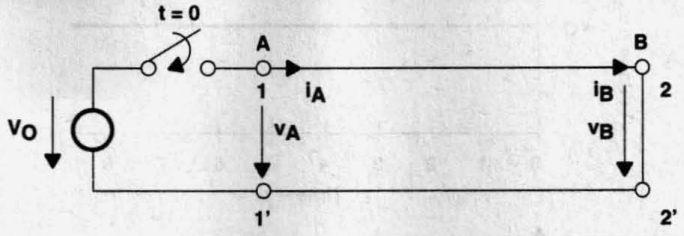


Figure 8. Ideal Voltage Source and Short-Circuited Line

The procedure is the same as in the previous example. First, establish the boundary conditions as follows:

A:

$$v_{A(t=0)} = V_O \tag{17}$$

B:

$$v_{B(t=0)} = 0 \tag{18}$$

Before turn-on, the line is without energy. For $t < 0$, therefore:

Starting point

$$v_{B(t<0)} = 0 \tag{19}$$

$$i_{B(t<0)} = 0 \tag{20}$$

Because the line is short-circuited at the end, the characteristic of the terminating impedance is coincident with the horizontal abscissa. Proceeding according to the method previously described and drawing the straight lines with the slope Z_O and $-Z_O$ in Figure 9, a zigzag line is obtained following the positive sense of current. There is no attenuation, so the current increases in steps towards infinity (see Figure 11).

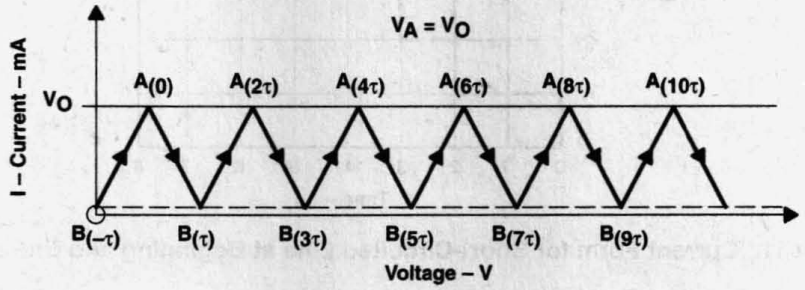


Figure 9. Bergeron Diagram for Short-Circuited Line

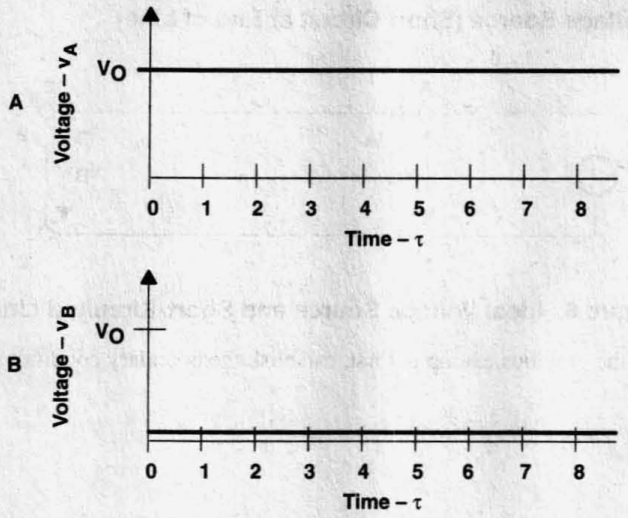


Figure 10. Potential Gradient for Short-Circuited Line at Beginning and End of Line

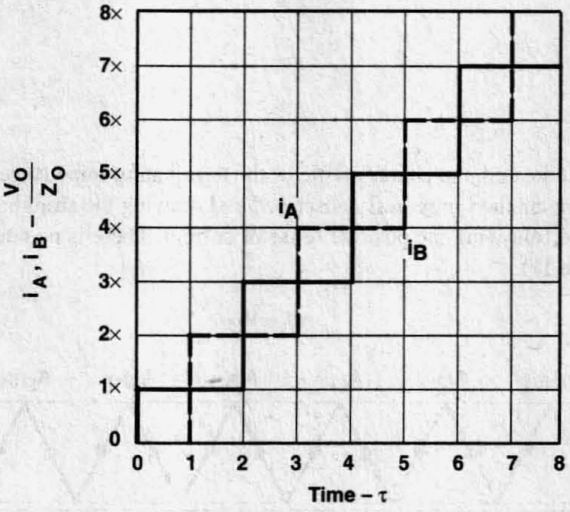


Figure 11. Current Form for Short-Circuited Line at Beginning and End of Line

4 Real Voltage Sources

4.1 Turning On a Real Voltage Source

4.1.1 Terminated Line

The examples described previously have no practical significance because there are no ideal voltage sources and the lines themselves are not loss-free either, although these losses may be neglected in the cases looked at here. Also, lines over which a signal is transmitted are terminated at the end in some form or another, if only by the input impedance of a receiver. Therefore, in what follows, the line reflections are examined that appear when a voltage source driving a line has a certain source impedance. The major cases encountered in practice are shown in Figure 12.

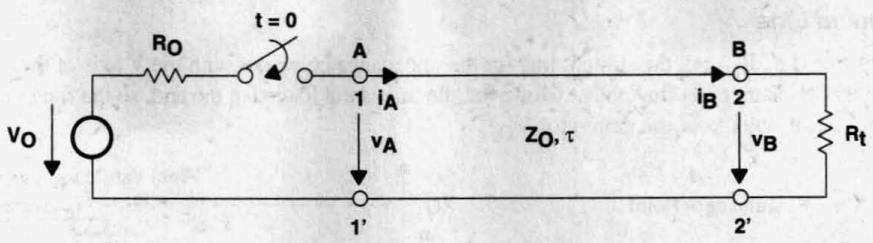


Figure 12. Real Voltage Source and Terminated Line

In a steady-state condition (i.e., t = ∞), the characteristics of the line are ineffective. Then the voltage that appears is a result of the voltage division by the voltage source impedance and the terminating impedance at the end of the line (see Figure 13).

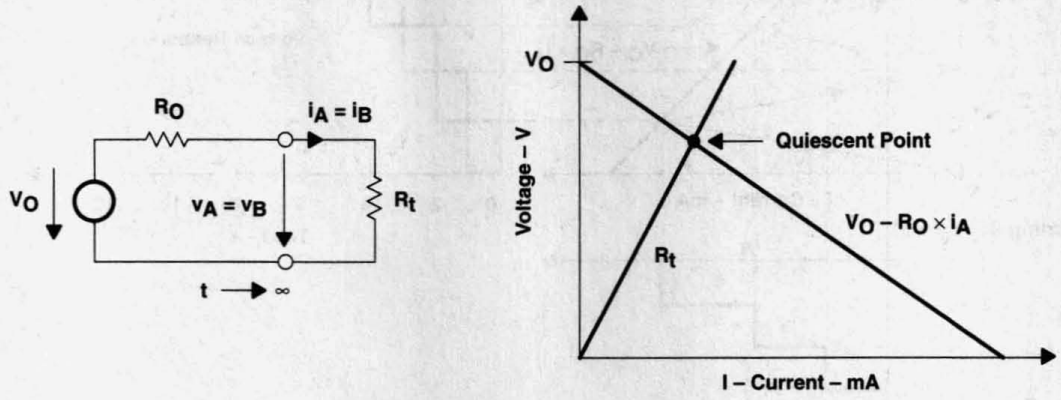


Figure 13. Line in Steady-State Condition

Determining the line reflections by the Bergeron method is performed in a manner similar to that previously described. At time $t < 0$ (switch open), the current and voltage on the line are 0. This value produces the starting point in Figure 14. The wave plan shows a zigzag form with the slope $\pm Z_O$ between the characteristics of the two line terminations. The zigzag line ends at the quiescent point. The condition on the line then is steady state, and there are, again, dc relationships.

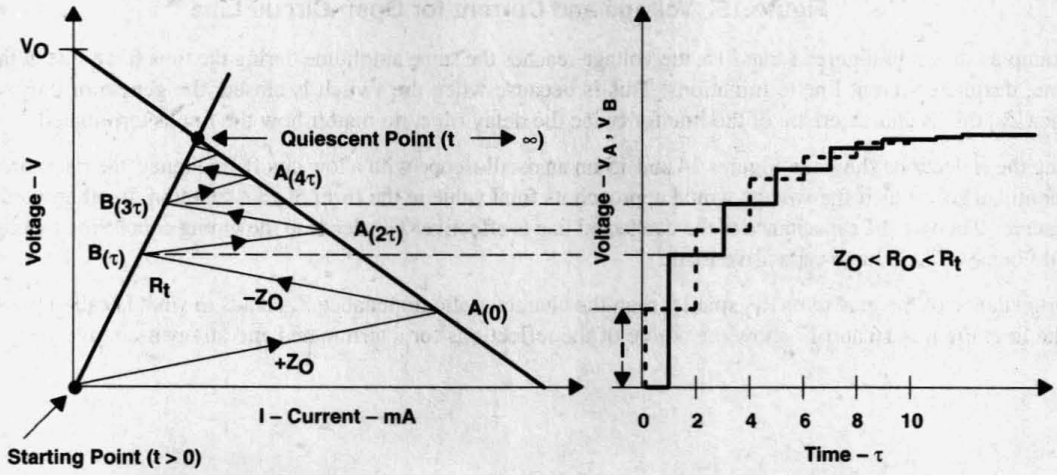


Figure 14. Line Reflections for Terminated Line

4.1.2 Unterminated Line

With an open-circuit line (i.e., $R_t = \infty$), the straight line for the impedance coincides with the V axis of the diagram. In this case, too, the voltage slowly builds up to its final value. However, the line is not loaded at the end, so the final value of the amplitude is equal to the open-circuit voltage of the generator V_O.

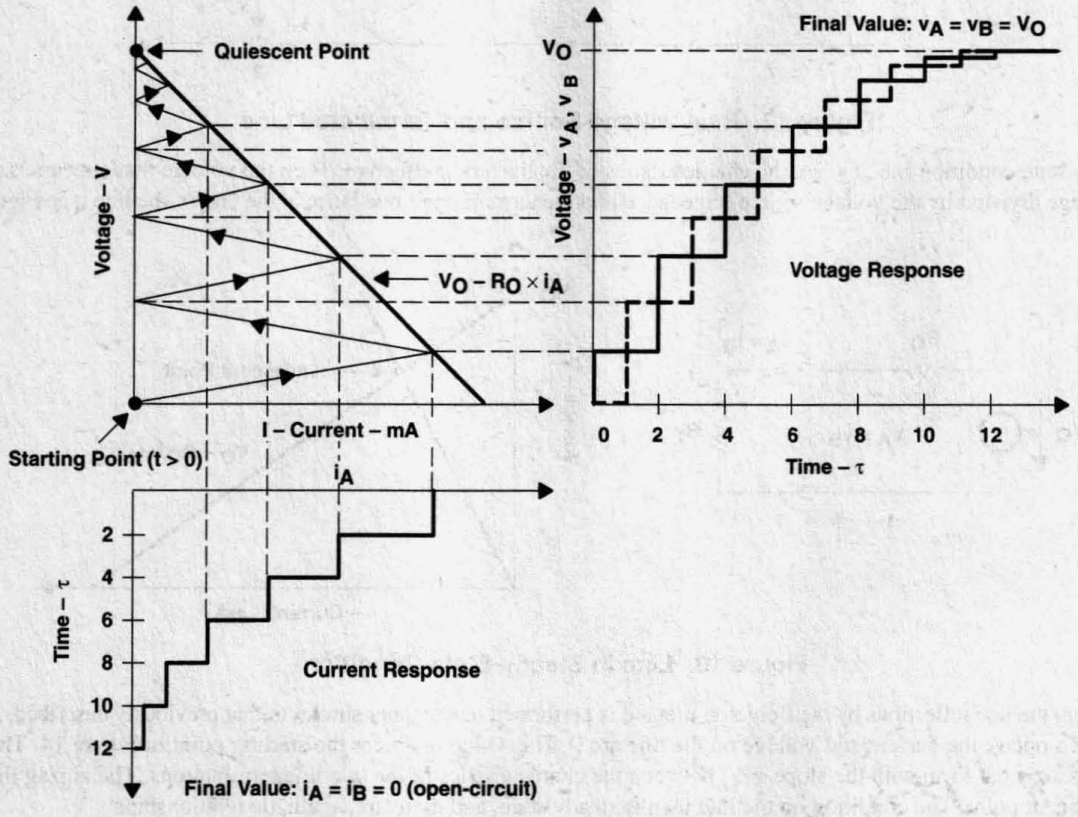


Figure 15. Voltage and Current for Open-Circuit Line

In the examples shown in Figures 14 and 15, the voltage reaches the same amplitude during the time $0 < t < 2\tau$ at the beginning of the line, despite different line terminations. This is because when the switch is closed, the generator only sees the line impedance Z_O that is characteristic of the line for twice the delay time, no matter how the line is terminated.

Observing the reflections shown in Figures 14 and 15 on an oscilloscope with a low cutoff frequency, the risers are obliterated. Consequently, it seems as if the voltage would approach its final value in the form of an e-function. In other words, it appears to the observer that only the capacitance of the connected line is effective. This leads to the wrong conclusion that the connected line would behave like a large capacitive load.

Source impedance of the generator R_O smaller than the characteristic impedance Z_O leads to what is called overshoot at the end of the line. Figures 16 and 17 show the nature of the reflections for a terminated and an open-circuit line.

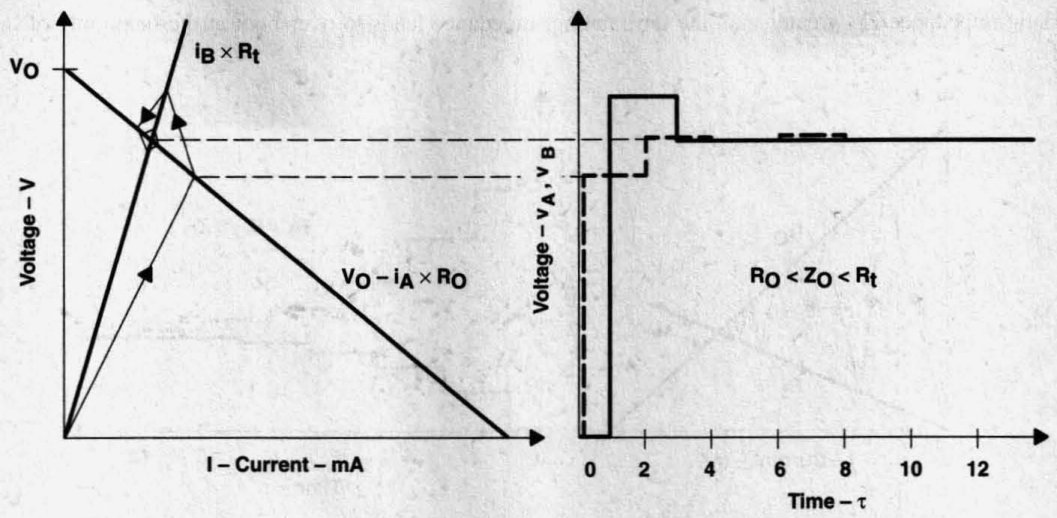


Figure 16. Terminated Line ($R_O < Z_O < R_t$)

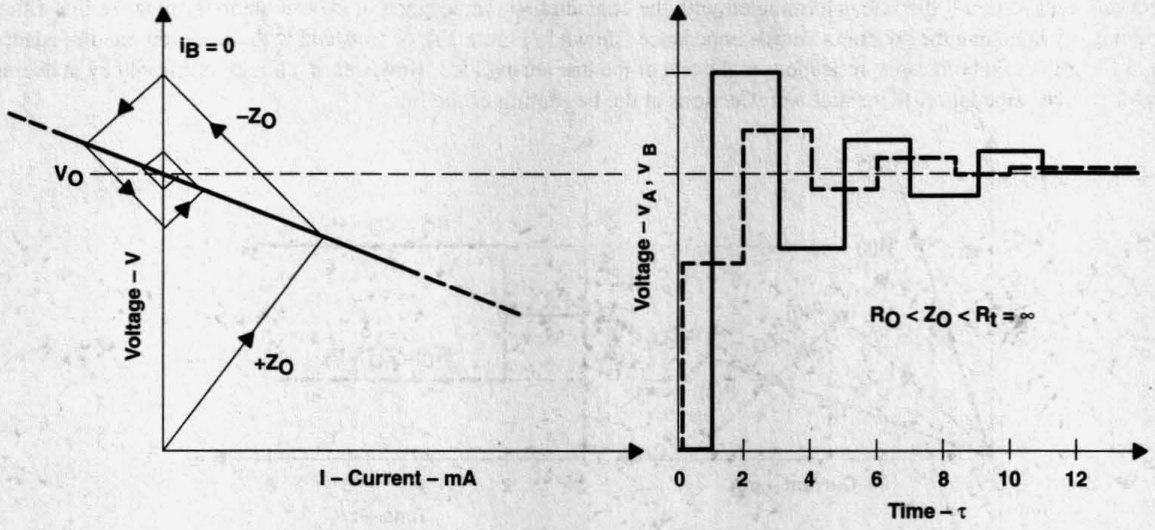


Figure 17. Open-Circuit Line ($R_O < Z_O < R_t$)

Characteristic impedance Z_O greater than the terminating impedance leads to overshoot at the beginning of the line (see Figure 18).

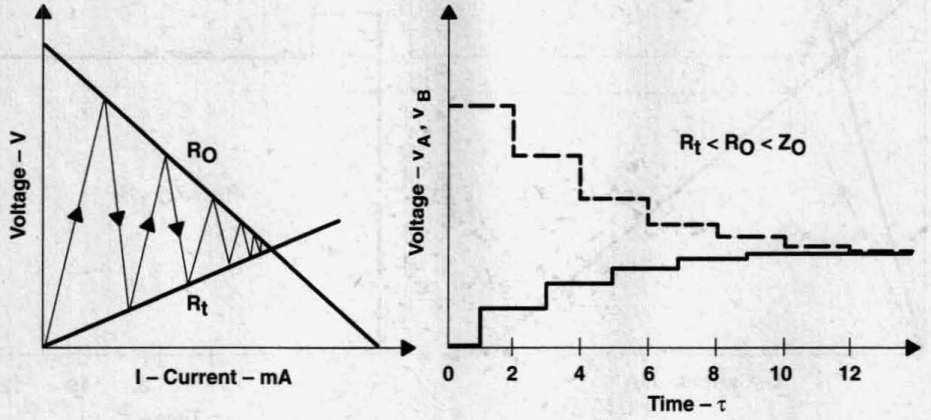


Figure 18. Terminated Line ($R_O < Z_O$)

4.1.3 Matching

Line reflections are avoided if the line is terminated with the characteristic impedance. It is possible to terminate a line either at the beginning, by matching the generator source impedance (shown in Figure 19), or at its end with an appropriate impedance (as shown in Figure 20). In both cases, reflections at the end of the line are avoided. However, if a line is terminated by matching the generator source impedance, there will be reflections at the beginning of the line.

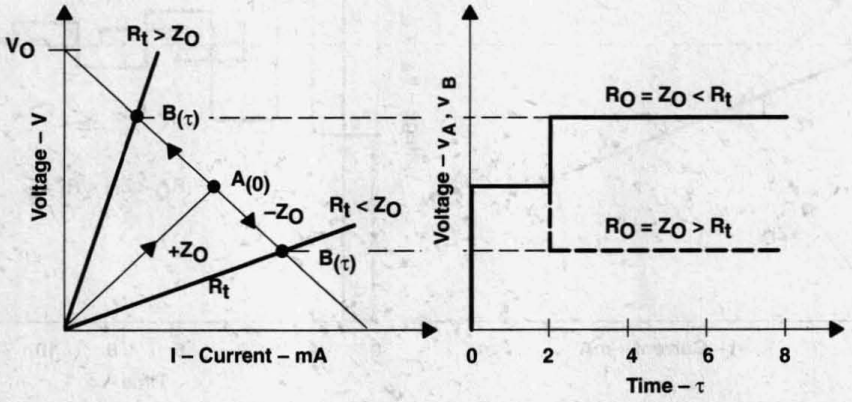


Figure 19. Line Termination by Matching Generator Source Impedance

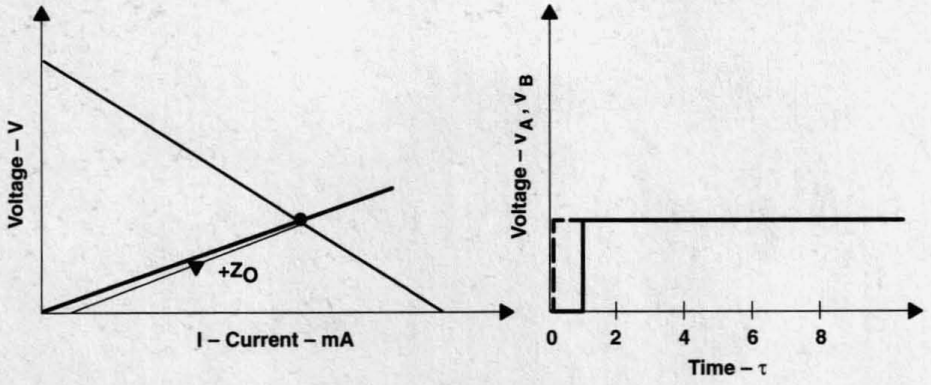


Figure 20. Line Termination by Terminating Impedance at the Line End

4.2 Turning Off a Line

The nature of the reflections on a line, when the voltage source is turned off (see Figure 21), can also be examined by the method previously described. If the switch at the generator output is opened, the energy stored in the capacitance of the line must be broken down and the voltage will not immediately fall to zero.

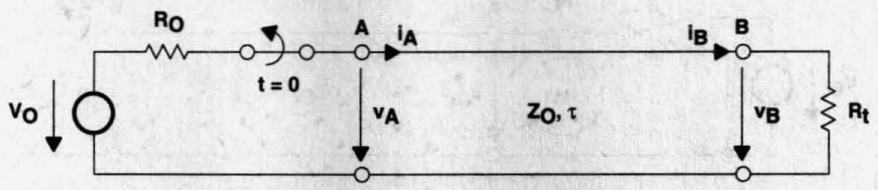


Figure 21. Turning Off a Line

The starting point for the Bergeron method is determined by the state at the point in time $t < 0$ as follows:

$$v_{B(-\tau)} = \frac{R_t}{R_O + R_t} \times V_O \tag{21}$$

$$i_{B(-\tau)} = \frac{V_O}{R_O + R_t} \tag{22}$$

Boundary condition (t = 0)

A:

$$i_A = 0 \tag{23}$$

B:

$$v_B = i_B \times R_t \tag{24}$$

Figure 22 shows the corresponding Bergeron diagram and the resulting potential gradient.

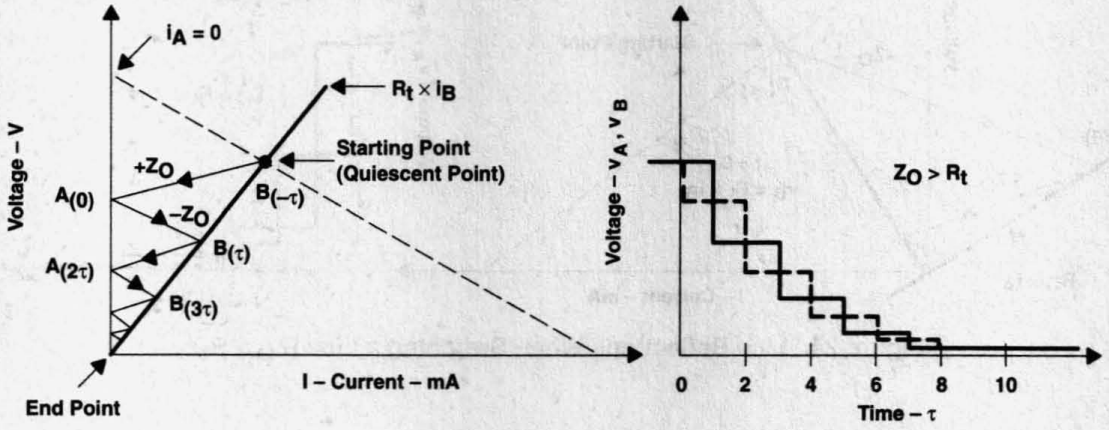


Figure 22. Line Reflections When Turning Off a Line

If the line is terminated at the end with an impedance $R_t = Z_O$, the voltage immediately swings to zero.

4.3 Switching a Line

The outputs of digital circuits are generally push-pull outputs. This means that when an output is switched, either a high voltage or a low voltage is connected to the line across the source impedance of the output stage (see Figure 23).

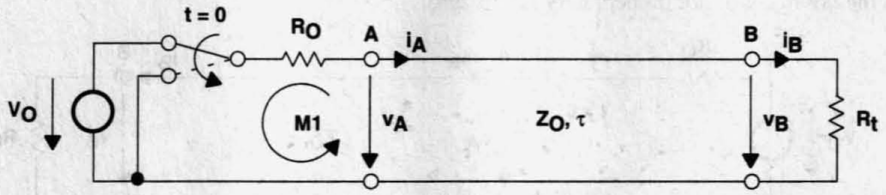


Figure 23. Switching a Line

At the point in time t = 0, the line is short-circuited on the input side across the source impedance of the generator. Before the switching, the same dc values apply as in the previous example.

Boundary condition

A:

$$v_A = -R_O \times i_A \text{ (loop M1)} \tag{25}$$

B:

$$v_B = R_t \times i_B \tag{26}$$

At the beginning of the line and at the end there are finite impedances, so the wave energy and, thus, the voltages V_A and V_B can break down faster than in the previous example.

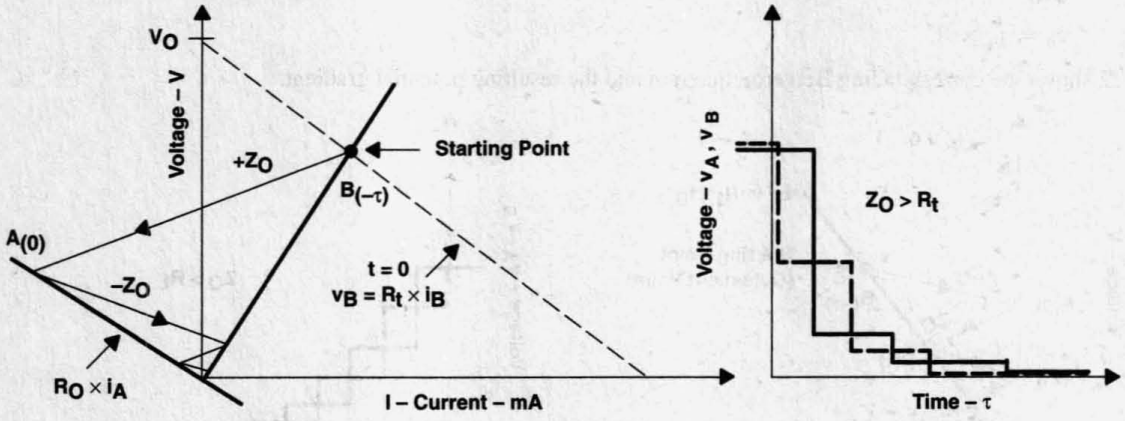


Figure 24. Line Reflections When Switching a Line ($Z_O > R_t$)

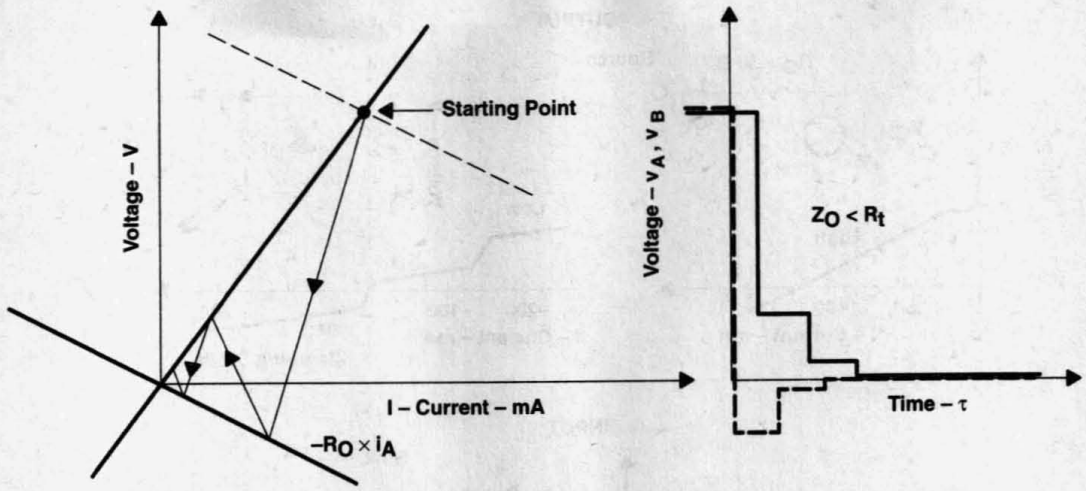


Figure 25. Line Reflections When Switching a Line ($Z_O < R_t$)

5 Bergeron Method With Nonlinear Line Terminations

As mentioned previously, the method can easily be applied for nonlinear characteristics exhibited by the inputs and outputs of TTL circuits. The senses shown in Figure 26 apply to currents and voltages.

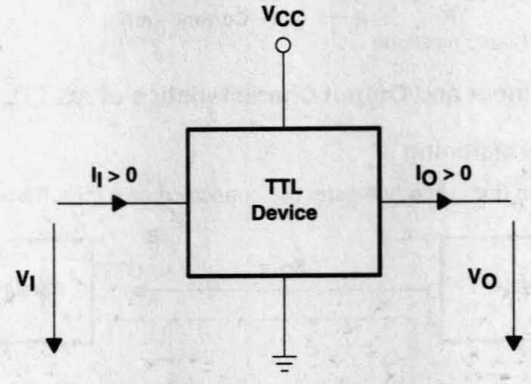


Figure 26. Definition of Current and Voltage Senses

Figure 27 shows the typical input and output characteristics of an AS/TTL circuit. A high output responds like a voltage source with an open-circuit voltage of about $V_{OH} = 3.5$ V and a source impedance of $R_O \approx 30\ \Omega$. In the low condition with positive voltages, the very low collector series resistance ($\approx 3\ \Omega$) is primarily effective, while negative voltages are limited by a Schottky diode at the output. The input characteristic is determined in the positive region by the high input impedance of the circuit (several kΩ). Again, negative voltages are limited by a Schottky diode (clamping diode).

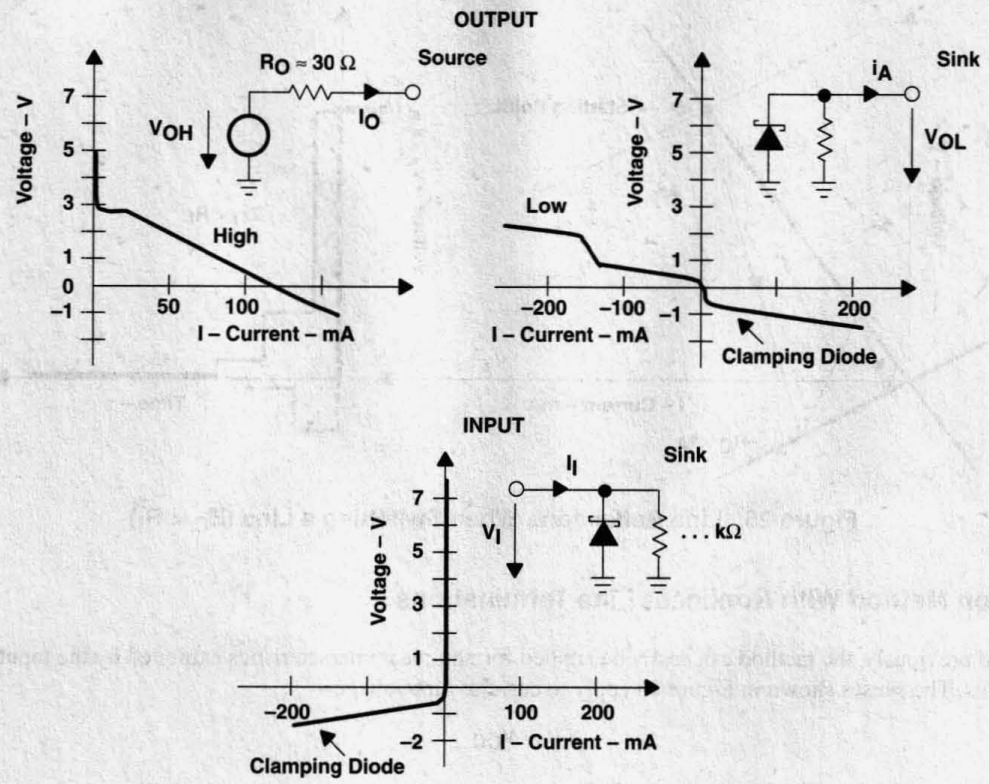


Figure 27. Input and Output Characteristics of AS/TTL Circuits

5.1 Gate Configuration Without Matching

Figure 28 shows a typical transmission line when two gates are connected on a circuit board.

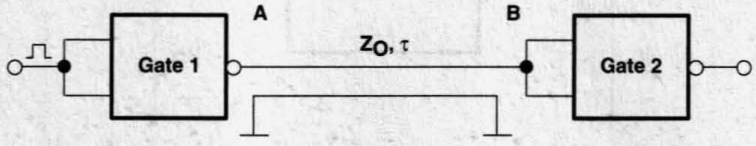


Figure 28. Transmission Line Without Matching

For the above configuration, all the necessary characteristics are entered into the V/I diagram (see Figure 29). The intersections of the input characteristic with the output characteristics are the steady-state conditions for high or low, and thus, the starting and finishing points of the Bergeron straight lines.

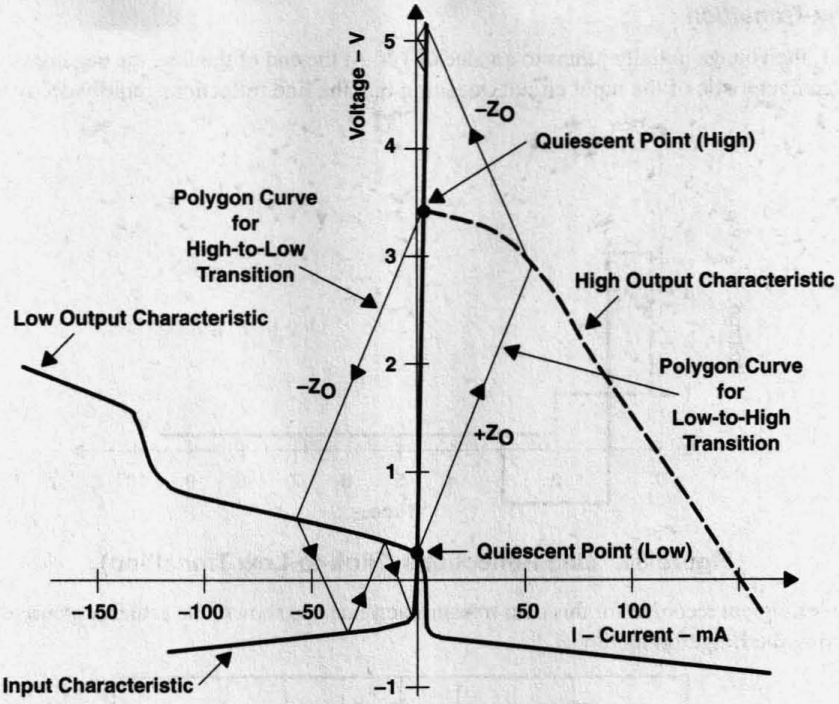


Figure 29. Bergeron Diagram for Transmission Line Between SN74AS000 TTL Circuits

5.1.1 Low-to-High Transition

Because of the low loading of the output by the line ($R_O < Z_O$), the voltage at the beginning of the line immediately rises to a value of about 2.5 V. The end of the line is terminated by the high input impedance of gate 2, thus, there is virtually a doubling of voltage. In this voltage region, the output impedance of gate 1 is also very large, so the voltage is slow in building up to its final value (see Figure 30).

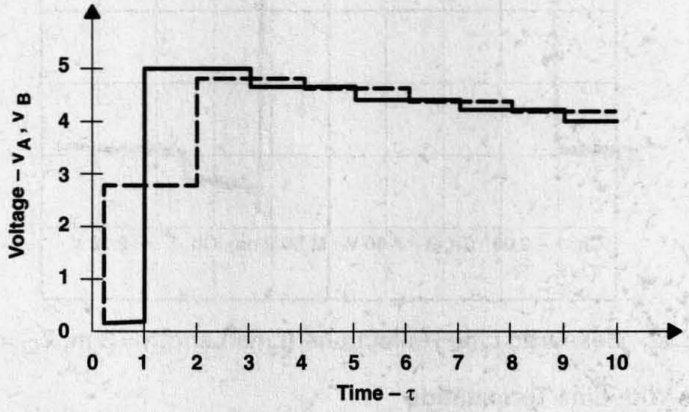


Figure 30. Line Reflections (Low-to-High Transition)

5.1.2 High-to-Low Transition

At the output of gate 1, the voltage initially jumps to a value of 1 V. At the end of the line, the negative overshoot is very much limited by the diode characteristic of the input circuit, meaning that the line reflections rapidly decay (see Figure 31).

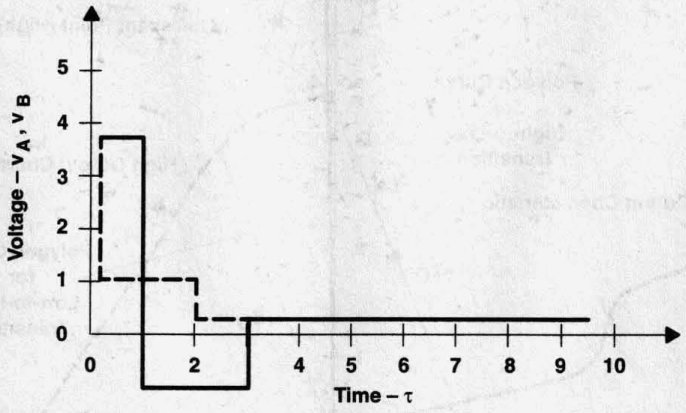


Figure 31. Line Reflections (High-to-Low Transition)

Figure 32 shows the oscillogram recorded for this data-transmission line. As shown, the actual response of the circuit coincides with that predicted using the Bergeron method.

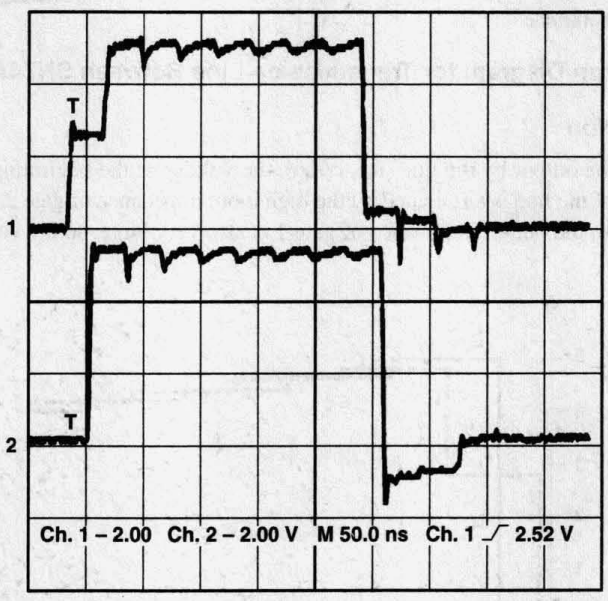


Figure 32. Measured Line Reflections (Line Length = 3 m, Z_O = 50 Ω)

5.2 Transmission Lines With Line Termination

Generally, lines in a TTL system do not have to be terminated. As shown previously, the reflections are usually adequately damped by the output impedance of the circuits (matching to the beginning of the line) or by clamping diodes (short-circuiting of the reflected energy). However, in certain applications, e.g., large bus systems, it may be necessary to provide for further damping of reflections by an additional termination of the line. The first possibility is that of terminating the end of the line with a resistance (see Figure 33).

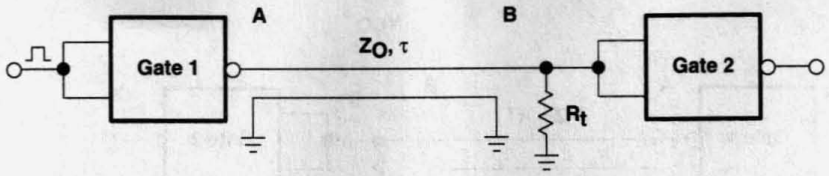


Figure 33. Termination of Line With a Resistor

Figure 34 shows the new characteristic of the line termination composed of the input characteristic of gate 2 and the parallel resistance R_t.

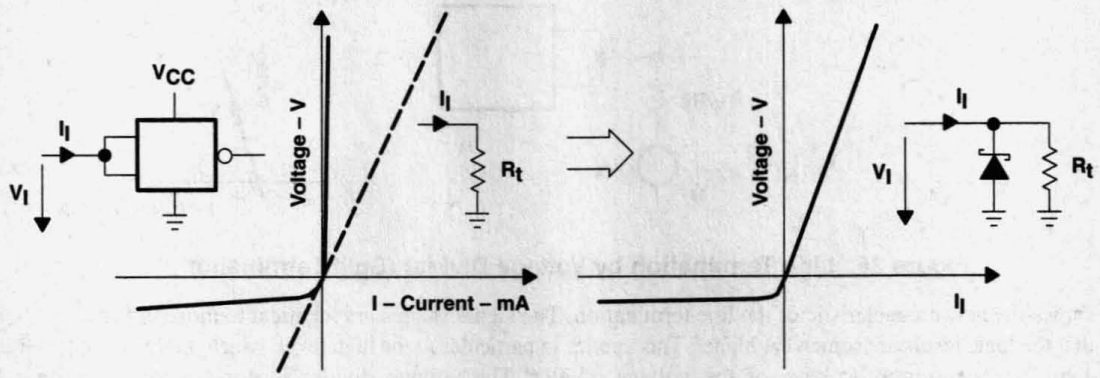


Figure 34. Characteristic of Line Termination

Figure 35 shows the signal shapes resulting on the line with matching ($R_t = Z_O$). As expected, reflections are completely avoided in this circuit. However, a drawback in this circuit is the high current that flows across the resistor, and the associated power consumption.

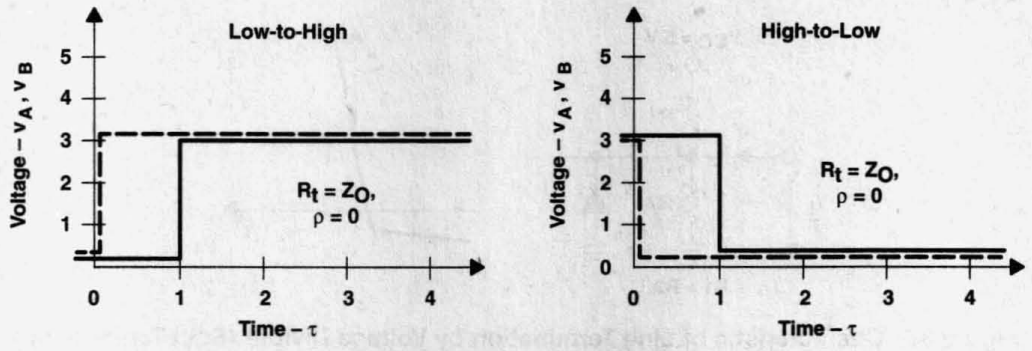


Figure 35. Signal Response for Matched Line

5.3 Split Termination

To reduce the dissipation in the terminating impedance, the line termination shown in Figure 36 is often used in TTL systems. In this case, the termination is split into two series-connected resistors (R1 and R2), thus, a split termination.

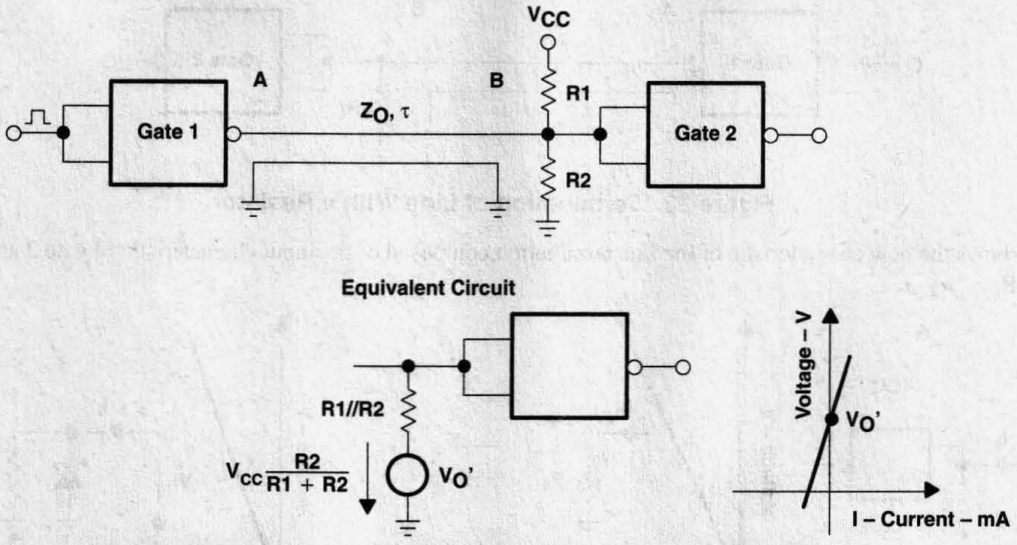


Figure 36. Line Termination by Voltage Divider (Split Termination)

Figure 37 shows the new characteristic of the line termination. The signal shapes are identical to those in Figure 34, with the exception that the logic levels are somewhat higher. This applies in particular to the high level, which, in this circuit, is primarily determined by the open-circuit voltage of the voltage divider. The voltage divider is dimensioned according to the following equations:

$$\frac{R1 \times R2}{R1 + R2} = Z_O \tag{27}$$

$$\frac{R2}{R1 + R2} \times V_{CC}\text{min} > 2.4\ V \tag{28}$$

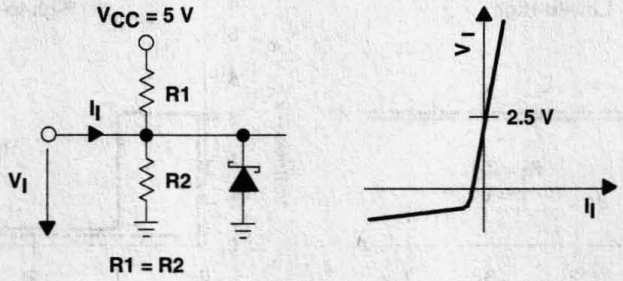


Figure 37. Characteristic of Line Termination by Voltage Divider (Split Termination) and Clamping Diode

5.4 Nonideal Matching

The good noise margin of TTL circuits allows a certain amount of line reflection. Ideal matching is, consequently, superfluous. Thus, termination can be a much higher impedance ($R_t > Z_O$) and power consumption can be reduced appreciably. TTL circuits provide a typical noise margin (N) as follows:

$$N = \frac{V_{TH} - V_{OL}}{V_{OH} - V_{OL}} = \frac{1.4\ V - 0.4\ V}{3.5\ V - 0.4\ V} \approx 0.35 \tag{29}$$

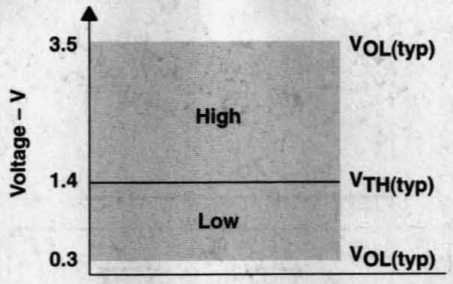


Figure 38. Typical Noise Margin of TTL Circuits

Spending 50% of the noise margin for line reflections, the acceptable reflection factor will be:

$$\rho = \frac{N}{2} \approx 0.2 \text{ (safety factor)} \tag{30}$$

With a reflection coefficient of $\rho = 0.2$, interference-free data transmission is ensured. From the equation for the reflection coefficient, there follows:

$$\rho = \frac{R_t - Z_O}{R_t + Z_O} = 0.2 \tag{31}$$

$$R_t = \frac{1.2}{0.8} \times Z_O = 1.5 \times Z_O \tag{32}$$

Equation 27 alters as follows:

$$\frac{R1 \times R2}{R1 + R2} = 1.5 \times Z_O \tag{33}$$

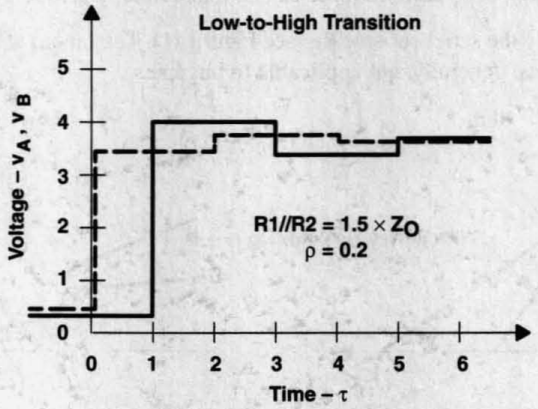


Figure 39. Line Reflections for Mismatch of 50% ($\rho = 0.2$)

CAUTION:

The supply voltage should be blocked on the terminating network by a ceramic capacitor (C = 0.1 μF) to ensure that the resistors (R1 and R2) cross ac voltage in parallel.

Lines on which there is data transfer in both directions (e.g., bus lines) must be terminated at both ends (see Figure 40). The resistors are dimensioned according to equations 28 and 33. This also ensures that defined high level appears on the bus when all drivers are inactive (3-state).

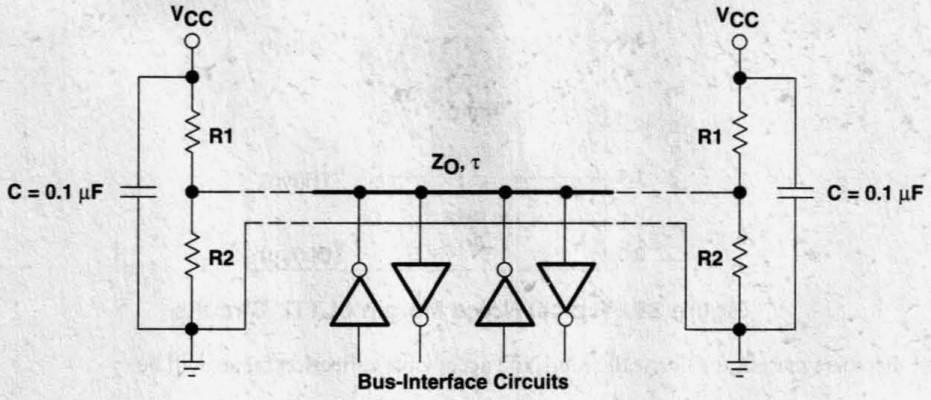


Figure 40. Termination of Bidirectional Bus Lines

5.5 Matching by Series Resistor

As shown in Figure 19, it is also possible to terminate the line at the beginning by appropriate matching of the generator source impedance, which avoids line reflections. In this case, the resistor R_S is connected in series with the output. This is selected so that, together with the source impedance R_O of the gate, it produces the required terminating impedance (see equation 34). The advantage of this circuitry variant is that the power consumption of the system is not increased by the termination.

$$R_O + R_S = Z_O \tag{34}$$

It should be noted that the output impedances of TTL circuits are different for high level (about 30 Ω) and low level (< 10 Ω). Therefore, ideal matching is only possible for one of the two logic levels. Since, as previously mentioned, a certain amount of reflection is admissible, in this case, also, compromises can be made in dimensioning.

The output characteristic is altered by the series resistor R_S (see Figure 41). The fanout of the driver is reduced. In this context note that this kind of line matching is, generally, not applicable to bus lines.

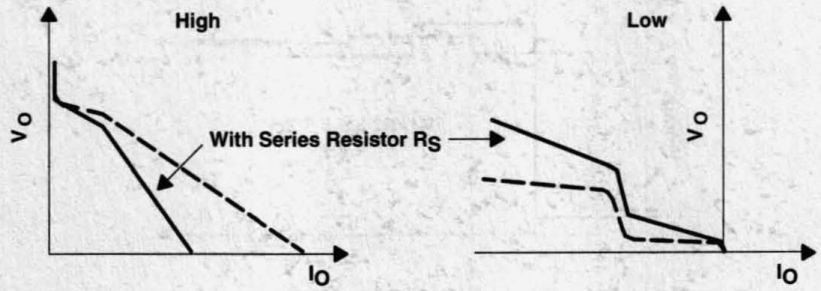


Figure 41. Driver Characteristics for Matching by Series Resistor

Acknowledgment

The author of this document is Karlheinz Fleder.

Appendix

Bergeron Diagrams

This appendix shows the Bergeron diagrams for different kinds of line matching. The output characteristics of the driver and the input characteristics of the receiver correspond to those of the SN74AS00. The following kinds of line termination are discussed:

No Line Termination (Figures 42, 43)

This is the arrangement of most connecting lines on a printed circuit. The positive edge produces a large positive overshoot that is slowly broken down because of the high impedances of the TTL circuits at these voltages. The negative overshoot resulting from the negative edge is largely damped by the clamping diodes at the input of the TTL circuits, meaning that here, also, no negative effects are expected.

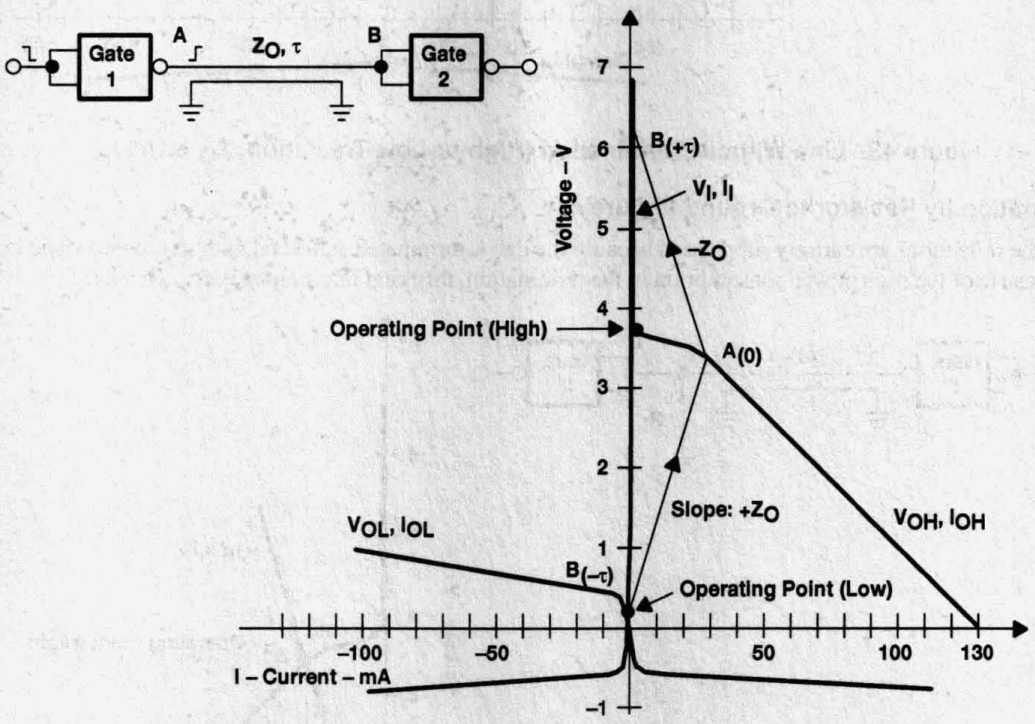


Figure 42. Line Without Termination (Low-to-High Transition, Z_O = 100 Ω)

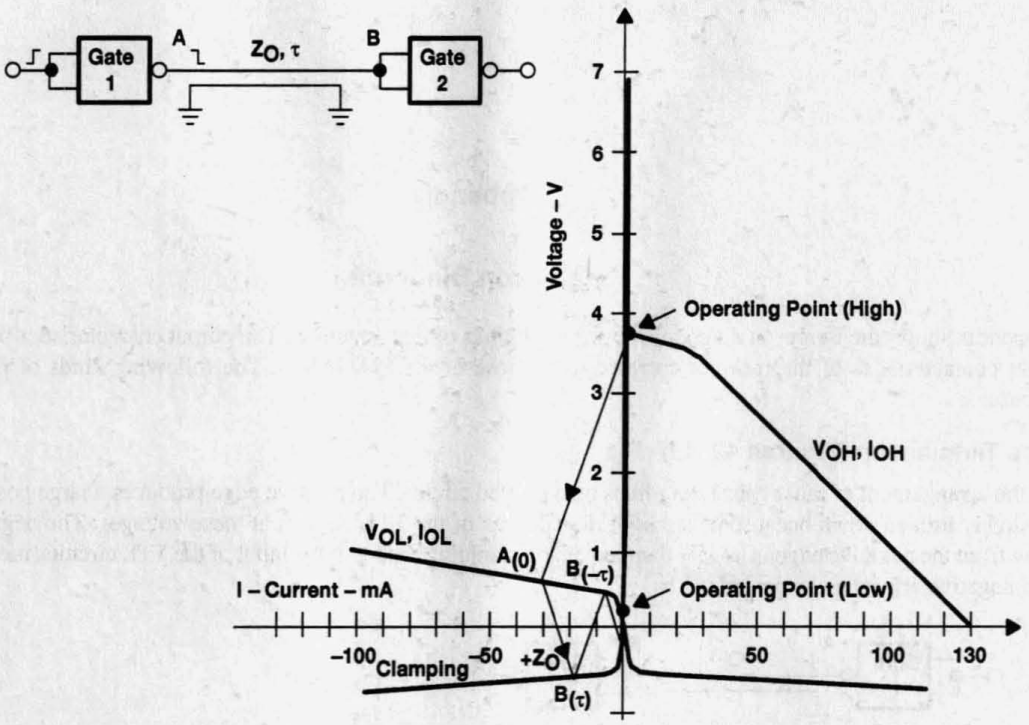


Figure 43. Line Without Termination (High-to-Low Transition, Z_O = 100 Ω)

Line Termination by Resistor to Ground (Figure 44)

In this case, the reflections are entirely suppressed because the line is terminated at the end with its characteristic impedance. However, because of the high power consumption in the termination, this kind of circuitry is not often used.

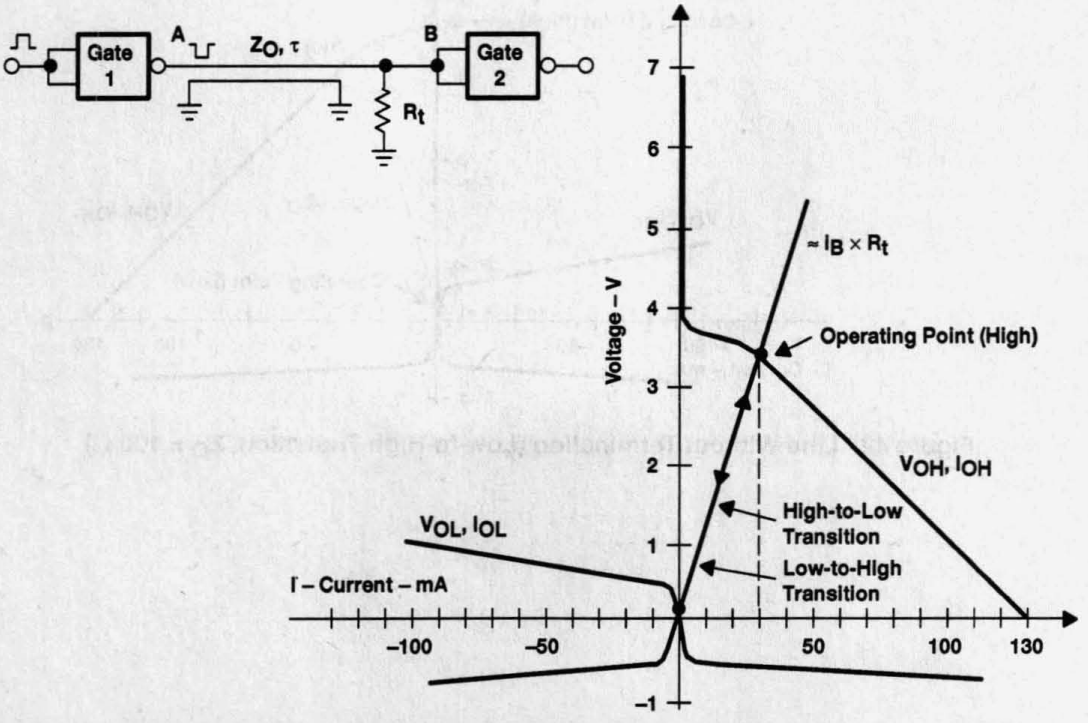


Figure 44. Line Termination by Resistor to Ground, Ideal Matching ($R_t = Z_O$ = 100 Ω)

Line Termination by Series Resistor in the Driver Output (Figure 45)

This kind of line termination requires the least amount of power. However, a disadvantage here is that the voltage at the beginning of the line, after switching, only reaches half amplitude for double the signal-delay time. Consequently, this kind of termination is not suitable for applications where there are several receivers arranged along the line (i.e., bus applications).

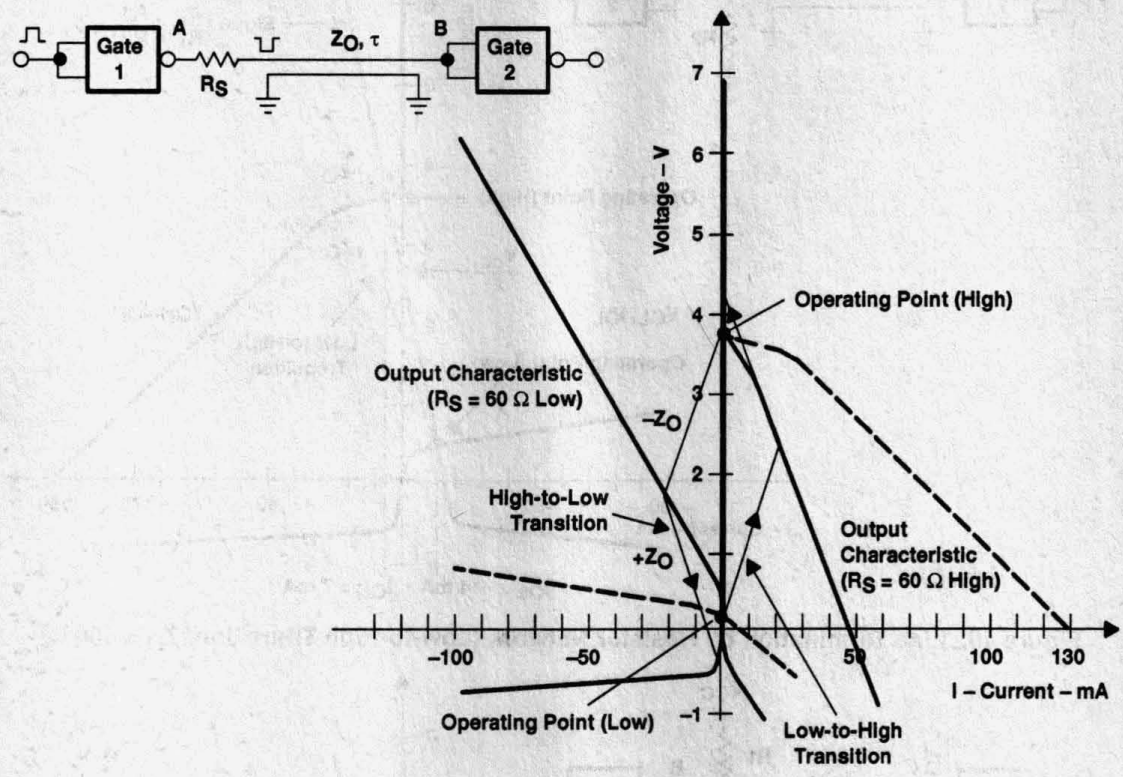


Figure 45. Line Termination by Series Resistor at the Generator Output (Z_O = 100 Ω)

Line Termination by Resistor Network (Split Termination) (Figures 46 and 47)

This is the most common kind of termination for lines that must be terminated. To reduce the power requirements in the terminating network, a certain mismatch will generally be tolerated. As shown in the figures, this does not lead to large signal distortions.

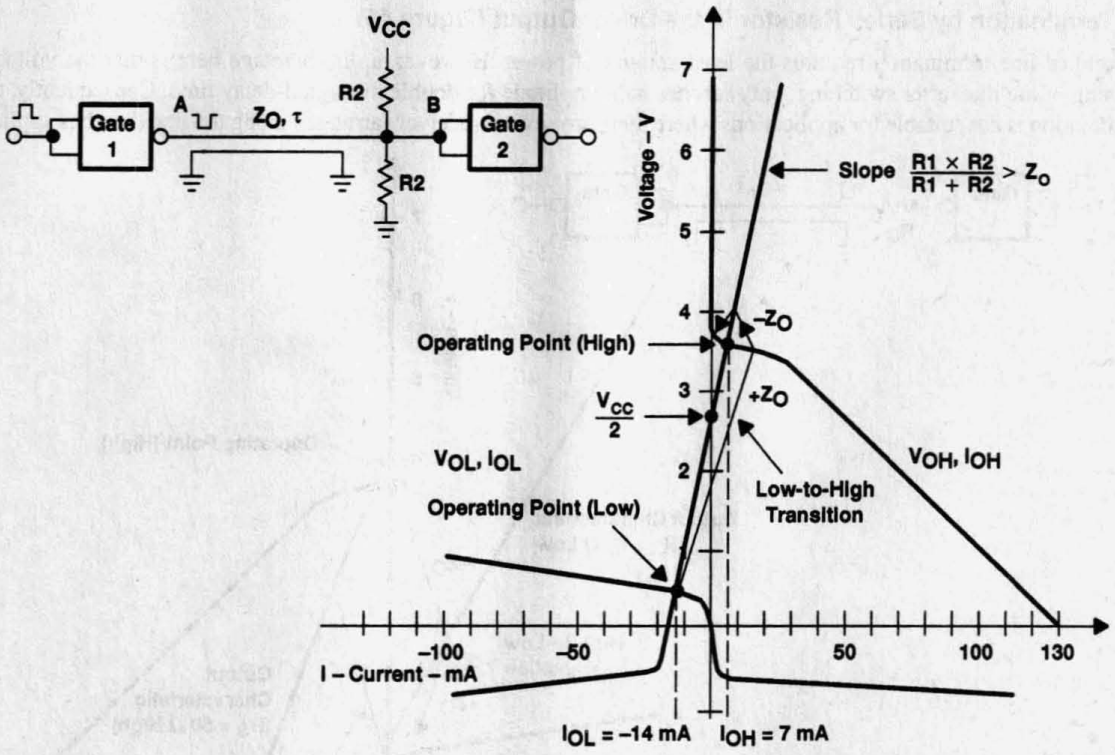


Figure 46. Line Termination by Resistor Network (Low-to-High Transition, Z_O = 100 Ω)

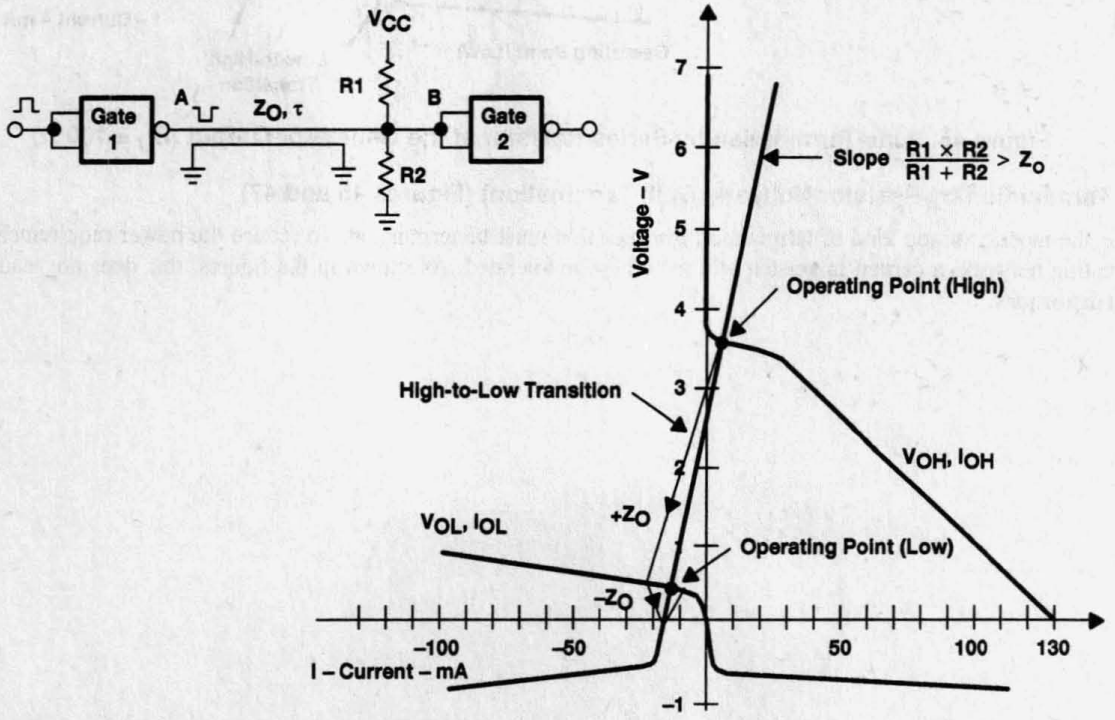


Figure 47. Line Termination by Resistor Network (High-to-Low Transition, Z_O = 100 Ω)

Live Insertion

SDYA012
October 1996

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	Page
Abstract	**2–63**
1 Introduction	**2–63**
2 Internal Construction of Integrated Circuits	**2–64**
3 Operating Conditions When Changing Modules With the Supply Voltage On	**2–66**
3.1 GND and the signal line (SL) make contact first; the output of circuit N1 is low	2–66
3.2 V_{CC} and the signal line (SL) make contact first; the output of circuit N1 is low	2–66
3.3 GND and the signal line (SL) make contact first; the output of circuit N1 is high	2–66
3.4 V_{CC} and the signal line (SL) make contact first; the output of circuit N1 is high	2–67
3.5 V_{CC} and GND make contact first	2–67
4 Simple Circuit Modifications	**2–67**
5 Avoidance of Bus Conflicts	**2–68**
6 Avoidance of Disturbances on the System Bus	**2–69**
7 Special Bus-Interface Circuits	**2–73**
8 Avoidance of Disturbances to the Supply Voltage	**2–75**
9 Summary	**2–79**
Acknowledgment	**2–79**

List of Illustrations

Figure	Title	Page
1	Diodes in the Inputs and Outputs of Integrated Circuits	2–64
2	Voltage-Monitoring Circuit in BiCMOS ICs	2–66
3	Simplified Circuit to Show Current Paths When Connecting a Module to a System	2–66
4	Improved Circuit Using Bipolar or BiCMOS Circuits	2–67
5	Curve for Calculating the Short-Circuit Currents That Occur With Bus Conflicts	2–68
6	Monitoring Bus-Interface Circuits	2–69
7	Connecting a Capacitor to a Line	2–70
8	Voltage Peaks When Making Contacts to Signal Lines (Without Voltage Bias)	2–70
9	Connection of a Capacitor to a Line (With Voltage Bias)	2–71
10	Voltage Peaks When Making Contacts to Signal Lines (With Voltage Bias)	2–71
11	Generation of the Voltage Bias and Control of the Interface	2–72
12	Generation of the Voltage Bias and Control in the SN74ABTE16245	2–73
13	Bus-Interface Control in ETL Circuits	2–74
14	Bus-Interface Control With BTL Circuits	2–75

Widebus is a trademark of Texas Instruments Incorporated.

List of Illustrations (continued)

Figure	*Title*	*Page*
15	Equivalent Circuit of the Current Supply to a Module	2–76
16	Transient Behavior of the Supply Voltage at Switch On, With Various Degrees of Damping	2–77
17	Switch-On Delay Circuit Using a MOS Transistor	2–77
18	Decentralized Power Supply With Limiting of Switch-On Current	2–78

Abstract

In many current applications, there is a requirement to exchange modules in electronic systems while the supply voltage remains on. This procedure is commonly known as live insertion. To understand this requirement, consider the case of an electronic telephone exchange in which replacing modules for maintenance or repair must be possible at any time without interrupting the operation of the system. To avoid damage to components, and any interruption of operation when changing modules in this way, additional circuitry modifications are necessary.

This report describes the phenomena that occur during live insertion, then presents circuit proposals to solve the potential problems that might otherwise arise.

1 Introduction

For many years, diverse functions and processes have been monitored and controlled successfully by electronic systems. The advantages of electronic controls in such cases (compared with manual or mechanical controls) are lower operating costs and the improved reliability that electronics now provide. However, faults also can arise in such electronic systems, which then require repair. By using modular construction for the equipment, it is possible to quickly exchange a defective module and clear the fault.

With most equipment, it is necessary to switch off the supply voltage during the exchange of the modules to avoid incorrect operation or destruction of components. In many cases–an obvious example is the computer in an office–the exchange of modules while the equipment is turned off is permissible.

In many electronic systems, switching off the equipment to exchange a defective module is unacceptable. Examples include an electronic telephone exchange, the switching control center of an electric utility, or the computer that processes data in the air-traffic control center of an airport. In all of these cases, when a fault is found in a module, exchanging this module in a running system without disturbing or otherwise compromising the rest of the system functions must be possible.

The engineer planning and developing electronic systems for such applications must consider the operating states that can arise and meet these requirements by choosing appropriate components and circuitry layout.

A distinction must be made at this point between two different cases. In the first, it is necessary only to ensure that a module or a part of the installation can be exchanged during operation without switching off the system and without damaging it. In such cases, it can be acceptable (for reasons described later) that the operation of the equipment is disturbed. An example is the installation or exchange of a printer for an operating office computer. The primary requirement is the simple and safe operation of the entire system; in this case, the requirements can be fulfilled by choosing appropriate components for the interfaces.

In the second case, the additional requirement must be met that, during exchange of the modules, the components involved should neither be damaged, nor should the operation be disturbed. To ensure this, beside choosing the appropriate components, the development engineer also must incorporate additional circuit modifications to allow continuous and reliable operation of the system.

This applications report provides the development engineer with suggestions for fulfilling these requirements. The report begins with the choice of the most appropriate components for the application, and continues with a description of circuit modifications that are necessary under the operating conditions described.

2 Internal Construction of Integrated Circuits

Some knowledge of the internal construction of integrated circuits is necessary to develop a system in which successful live insertion during operation is possible. It is less important to have a detailed knowledge of the internal circuit construction of the device than to know what information, in addition to that contained in data sheets, must be considered. In this case, protection circuits at the inputs and outputs are particularly important (for example, those for protection against destruction as a result of electrostatic discharge), together with the parasitic diodes in these parts of the circuit. The latter are determined by the internal construction of the circuits and by the characteristics that result from the production process.

In general, the structure of integrated circuits can be represented as shown in Figure 1. This simplified representation shows basic features of integrated circuits. An understanding of these features is necessary for proper understanding of the problems discussed in this report.

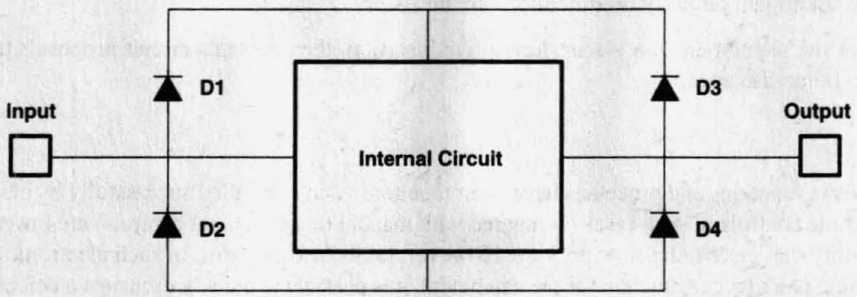


Figure 1. Diodes in the Inputs and Outputs of Integrated Circuits

The diodes shown in Figure 1 have the following functions:

- D1: This diode is integrated into most CMOS circuits for ESD protection. It is intended to limit positive voltages at the input of the circuit. This diode is not included in ABT, LVT, LVC, or AHC/AHCT devices.
- D2: This is a parasitic diode that is predetermined as a result of the internal construction of the semiconductor circuit. With digital circuits, an additional (lower-resistance) diode is intentionally integrated into the chip to limit undershoot of the input signals arising from line reflections. This diode also provides some protection from an electrostatic discharge.
- D3: This diode protects CMOS circuits against destruction as a result of electrostatic discharges. Most bipolar devices have a parasitic diode at this point as a result of the internal construction of the semiconductor. An exception is bipolar devices with an open-collector or 3-state output. With these devices, special modifications to the circuit ensure that this diode is not present and that this current path always remains at a high resistance.
- D4: This diode is present in all digital circuits. In most cases, it is the collector-substrate or drain-substrate diode of the lower-output transistor. With bipolar devices, an additional diode (a Schottky diode) is often integrated into the chip to limit undershoot arising from line reflections. With CMOS circuits, additional ESD-protection diodes are often incorporated.

Table 1. Internal Diodes and Withstanding Voltages of Logic Circuit Inputs and Outputs

	INPUT D1	TOTEM-POLE OUTPUT D3	OPEN-CIRCUIT COLLECTOR OUTPUT D3	3-STATE OUTPUT D3	POWER-UP 3-STATE CIRCUIT
SN7400	5.5 V	7 V	7 V	V_{CC} + 0.5 V	No
SN74LS	7 V	V_{CC} + 0.5 V	7 V	5.5 V	No
SN74S	5.5 V	V_{CC} + 0.5 V	7 V	5.5 V	No
SN74F	7 V	V_{CC} + 0.5 V	7 V	5.5 V	No
SN74ALS	7 V	V_{CC} + 0.5 V	7 V	5.5 V	No
SN74AS	7 V	V_{CC} + 0.5 V	7 V	5.5 V	No
SN74BCT	7 V	–	5.5 V	5.5 V	Yes
SN74ABT	7 V	–	–	5.5 V	Yes
SN74LVT	7 V		–	5.5 V	Yes
SN74HC	V_{CC} + 0.5 V	V_{CC} + 0.5 V	V_{CC} + 0.5 V	V_{CC} + 0.5 V	No
SN74AC	V_{CC} + 0.5 V	V_{CC} + 0.5 V	–	V_{CC} + 0.5 V	No
SN74LV	V_{CC} + 0.5 V	V_{CC} + 0.5 V	V_{CC} + 0.5 V	V_{CC} + 0.5 V	No
SN74LVC	7 V	V_{CC} + 0.5 V	–	5.5 V	No
SN74ALVC	4.6 V	–	–	V_{CC} + 0.5 V	No
SN74AHC	7 V	V_{CC} + 0.5 V	–	V_{CC} + 0.5 V	No
SN74AHCT	7 V	V_{CC} + 0.5 V	–	V_{CC} + 0.5 V	No

When changing modules with the supply voltage switched on, the voltages that are permissible to apply to the input and output components of the interfaces are of particular interest, as well as voltages at the interfaces with the supply voltage switched off. There are a large number of circuit variants and diverse logic functions. Table 1 provides development engineers with an overview of the voltages that can be applied to the terminals of various integrated circuits.

With devices that have diodes D1 and/or D3, a maximum voltage can be applied to the inputs and outputs that are 0.5 V more positive than the instantaneous V_{CC}. In Table 1, this is given as a maximum value of V_{CC} + 0.5 V. At higher voltages, these diodes become conducting. In this case, if there is no current limiting, the possibility of an overload or the destruction of the device must be accepted. If there are no diodes at this point, a voltage can be applied to the appropriate terminal, depending on the breakdown voltage of the transistors in the corresponding part of the circuit, independently of the instantaneous supply voltage. That is, when $V_{CC} = 0$. The permissible values of voltage are given in Table 1.

BiCMOS circuits also incorporate a power-up 3-state circuit. This circuit consists of a simple voltage-monitoring circuit (see Figure 2) in which V_{CC} is measured by diodes D1 and D2 and with the base-emitter voltage of transistor Q1. Below a certain supply voltage $V_{CC(off)}$ (ABT/BCT: $V_{CC(off)} \approx 2.5$ V; LVT: $V_{CC(off)} \approx 1.8$ V), the output of this circuit is at a high logic state. This signal switches all transistors in the output stage into a high-resistance blocked state (3-state), independently of signals applied to the control inputs of the circuits.

This property of BiCMOS bus-interface devices ensures that a defined behavior can be predicted, even at very low supply voltages where, usually, component behavior is not predictable. Because of power-up 3-state, BiCMOS devices have an advantage over CMOS devices in live-insertion applications.

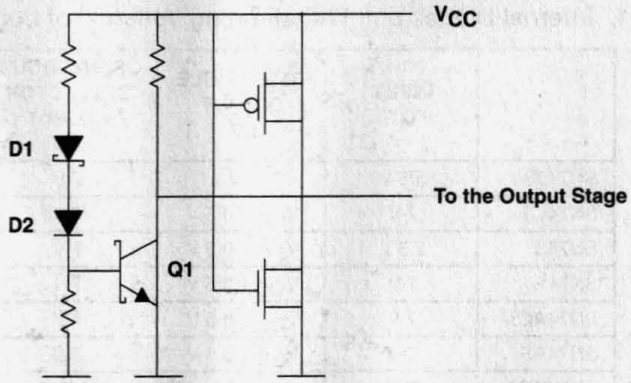


Figure 2. Voltage-Monitoring Circuit in BiCMOS ICs

3 Operating Conditions When Changing Modules With the Supply Voltage On

The previous section describes certain peculiarities of the inputs and outputs of integrated circuits. The operating conditions that can arise when inserting a module in a large system are now examined. The basis for this discussion is the circuit shown in Figure 3. Module 1 is assumed to be connected to the backplane wiring and supplied with voltage from source V1 via the backplane wiring.

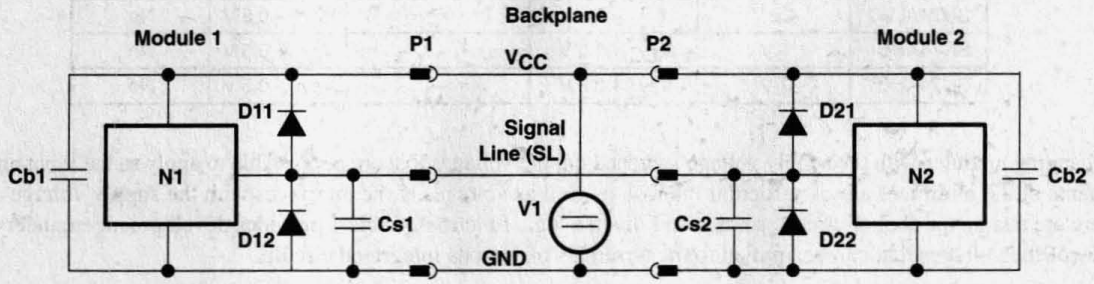


Figure 3. Simplified Circuit to Show Current Paths When Connecting a Module to a System

If Module 2 is inserted into a slot, the contacts of connector P2 make contact in random order as a result of the mechanical tolerances of the guide rails and of the connector. Thus, it is necessary to analyze the various logic states that result.

3.1 GND and the signal line (SL) make contact first; the output of circuit N1 is low

When the module is inserted, a switching capacitance (Cs2 ≈ 20 pF), consisting of the capacitance of the connector P2, the connection to the module, and the input and output capacitance of circuit N2, is charged to the instantaneous logic level (U_{SL} ≈ 0.4 V) of the signal line. Diodes D21 and D22 remain blocking. The signal line is not undesirably influenced. After the connection to V_{CC}, capacitor Cb2 (consisting of the blocking capacitors and the capacitance of the entire circuit) becomes charged, and the circuit on the module that has been inserted commences operation. The disturbances that arise during this switching-on phase, and which result from the initially undefined operation of circuit N2 and from disturbances on V_{CC}, are discussed later in more detail.

3.2 V_{CC} and the signal line (SL) make contact first; the output of circuit N1 is low

When the module is inserted, a connection between the signal line and GND is made via diode D22. The output of circuit N1 first supplies current via this route to the second module until GND also makes contact. This produces severe distortion of the signal on the signal line. As a result of the large equalizing currents that can be expected, an overload of both the output of circuit N1 and diode D22 is likely.

3.3 GND and the signal line (SL) make contact first; the output of circuit N1 is high

When the module is inserted, conditions arise similar to those described in the previous case. The output of circuit N1 supplies current via diode D21, causing an overload of both the output of circuit N1 and of diode D21. Under these circumstances, a defined signal on the signal line cannot be expected.

3.4 V_{CC} and the signal line (SL) make contact first; the output of circuit N1 is high

Assuming that capacitor Cs2 is discharged and that the high level at the output of circuit N1 < V_{CC} , diode D22 conducts and charges capacitor Cb2 to the difference between V_{CC} and the high level at the output of circuit N1. Under these circumstances, the current that flows is negligible as a result of the low level of current supplied by circuit N1. Signal distortion on the signal line is also very small, although the high level is somewhat elevated. This situation is not critical until, after a short time, the output of circuit N1 switches to low, when the state described in section 3.2 is reached.

3.5 V_{CC} and GND make contact first

Under these circumstances, V_{CC} goes to Module 2 before the signal line makes contact. Assuming that the supply voltage to Module 2 has reached an adequate level before the signal line makes contact, and that at the output of circuit N2 a defined (high-resistance) state already has been reached, any disturbance on the signal line can be largely avoided. However, it is possible that the output of circuit N1 is also at a high level, and the switching capacitance Cs2 also must be charged to this level. As shown later, under these circumstances a disturbance of the signal also must be expected.

4 Simple Circuit Modifications

The circuit shown in Figure 3 is so arbitrary that, under the conditions described above, it is impossible to attain definite operating states when inserting a module while the system is operating. The undefined order in which the V_{CC} and GND connections are made is unfavorable. Diodes D21 and D22 also are detrimental, because, in most cases, they open up undesirable current paths, which can then result in faulty operation, if not destruction of components.

The behavior of the circuit can be predicted if the following two requirements are met:

- The connector has one or more leading ground (GND) contacts that make contact before any other contacts are closed.
- For the interface, only integrated circuits without diodes (D11 and D21 in Figure 3) connected to the supply voltage rail, either at the inputs or at the outputs, are used. This requirement applies to all bipolar and BiCMOS circuits with 3-state or open-collector outputs.

The five possible operating states described previously have been reduced to those described in subsections 3.1 and 3.3. Figure 4 shows the changed circuit.

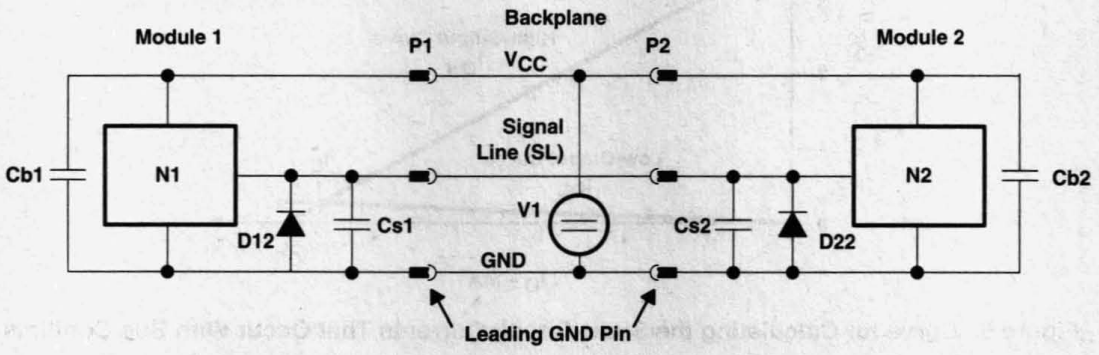


Figure 4. Improved Circuit Using Bipolar or BiCMOS Circuits

When inserting a module into a running system, the ground connection GND makes contact first. This ensures that definite potentials exist between the system and the new module. Diode D22, between the inputs and outputs of the integrated circuits and the ground line, is now operating only in a blocking state. Equalizing currents no longer occur along this path and, to this extent, destruction of the components is prevented.

If contact is made with the signal line before V_{CC}, outputs of the integrated circuits first remain in a high-resistance state. Only after the positive V_{CC} has been connected and the supply voltage to the module has slowly risen, can the outputs of the circuits N2 at the interfaces switch in a more-or-less undefined fashion. At the first instance (charging time of capacitor Cb2), with supply voltages that are still low, neither a definite operation of the enable logic in these bus-interface circuits can be expected, nor is it certain that valid signals will be provided by the controlling circuit to the module that has been inserted.

Using the simple precautions discussed previously can, to a large extent, ensure that a module inserted in an operating system is not damaged. More comprehensive (and costly) precautions are not necessary.

However, there are a number of effects caused by inserting a module that can result in faulty system operation or, in the worst case, can destroy the integrated circuits. For such possibilities, the following phenomena must be considered:

- When inserting a module and before making contact to the signal line, capacitor Cb2 in Figure 4 must be charged. The resulting currents inevitably cause distortion of the signals transmitted through the backplane wiring.
- As mentioned previously, when the supply voltage to the module that has just been inserted ramps up, the outputs of the interface circuits (N2 in Figure 4) can switch on in an uncontrolled fashion. In the simplest case, this can result in short circuiting of the signal, which interferes with the transmission of data in progress. If these bus conflicts continue long enough, thermal overloading of the circuits and destruction of the components can follow, involving not only the module that has just been inserted, but also circuits N1 and N2 in Figure 4.

5 Avoidance of Bus Conflicts

Bus conflicts arise when two or more interface circuits attempt to drive the bus simultaneously, one circuit delivering a high level and the other circuit a low level. Figure 5 shows the simplified typical output characteristics of bipolar bus-interface circuits. The currents that result when a bus conflict occurs are about I_k = 120 mA per output (see Figure 5), determined by the short-circuit current of the circuit that is attempting to supply the high level. The circuit that is trying to generate the low level takes precedence in such a situation. With this circuit, the overload is within acceptable limits. With a low output voltage, V_{OL} < 0.5 V, the total power dissipation P_{dl} of a circuit with n = 8 outputs (for example, the SN74ABT240) can be calculated as follows:

$$P_{dl} = n \times V_{OL} \times I_k = 8 \times 0.5\ V \times 120\ mA = 480\ mW \quad (1)$$

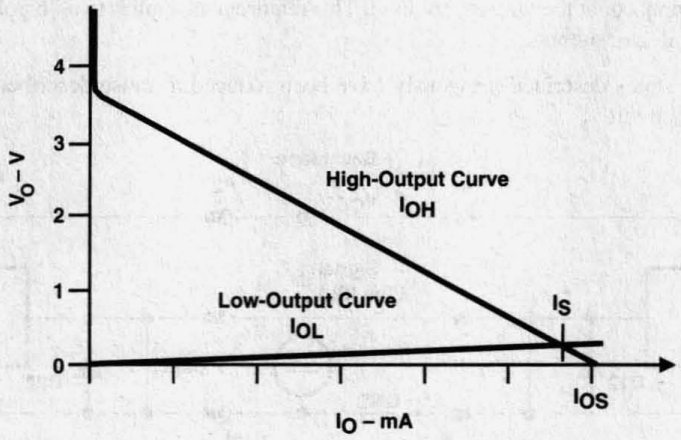


Figure 5. Curve for Calculating the Short-Circuit Currents That Occur With Bus Conflicts

Even with 16-bit Widebus™ circuits, reliability should not be detrimentally affected. The situation is different in the case of the circuit that should deliver the high level. As a result of the short circuit, the voltage drop across the output is about 5 V. With the currents assumed previously, the power dissipation increases to P_{dh} = 5 W (with Widebus circuits, to more than 10 W). Assuming a thermal resistance between the chip and ambient temperature of $R_{\theta JA} \approx 100$ K/W, and a thermal time constant for the silicon chip of $t_\vartheta \approx 1$ ms, in a very short time unacceptably high chip temperatures are reached, and destruction of the integrated circuit (or at least a significant deterioration of its reliability) is likely.

Additional circuit modifications are necessary to prevent an overload of the interface circuits. The simplest way to make the situation less critical consists of using only bus-interface circuits, which are provided with the power-up 3-state circuit, mentioned previously, at any questionable points in the circuit. Assuming that, in the system in question, the other digital circuits on the module that is to be exchanged have been implemented in CMOS technology (which at V_{CC} > 2 V are known to supply defined logic levels), bus conflicts should be avoided.

Unfortunately, in many cases it cannot be assumed that the logic circuits mentioned will also supply defined levels at higher supply voltages, keeping the bus-interface circuits in an inactive state. These logic circuits usually are controlled by VLSI circuits, e.g., by the microprocessor on this module. Last, control circuits do not necessarily supply valid output signals at very low supply voltages and during the initialization phase. The development engineer must use additional circuits that ensure, under all circumstances, that the circuits switch into 3-state.

A circuit proposal is shown in Figure 6. The heart of this circuit consists of the supply voltage supervision and initialization integrated circuit TLC7705. A component of this kind in the module is usually necessary to ensure correct initialization of the circuit (RESET) when switching on the supply voltage. Additionally, the outputs of this circuit are taken to the enable inputs of the bus-interface circuit in order, during the initialization phase, to keep the bus-interface circuits, under every condition, in an inactive high-resistance state. For this purpose, it is advantageous to use bus-interface devices having two enable inputs of equal priority, such as the SN74ABT541. With this device, one of the inputs is connected to the output of the monitor circuit, while the other input is connected to the part of the circuit that normally releases the outputs of the bus-interface circuits. If two independent enable inputs are not available, as with the SN74ABT245, the required function must be performed with an additional gate, for example, the SN74AC32. In some cases, the resulting increase in delay time is unacceptable. Faster bipolar circuits, such as the gate SN74F00, can remedy the delay-time problem. With these single-stage logic circuits, it is possible to ensure, even at very low supply voltages of 2 to 4.5 V, that a low level at an input will result in a high state at the output. However, under these circumstances, an adequate voltage level cannot be guaranteed. For this reason, as shown in Figure 6, a resistor should be provided at the output of this gate to pull the output up to a sufficiently high level.

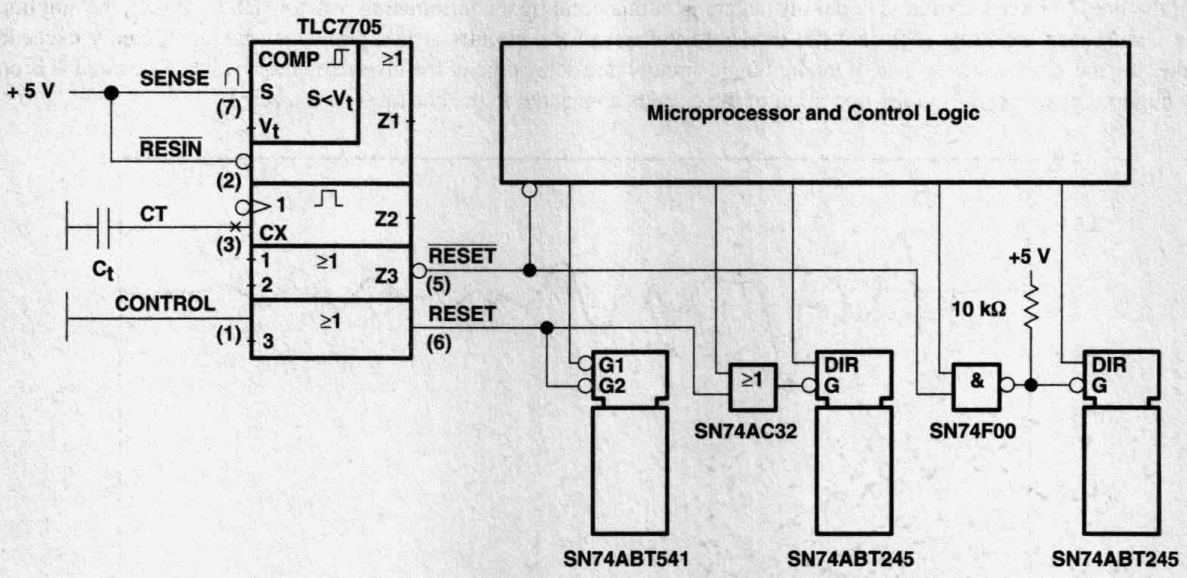


Figure 6. Monitoring Bus-Interface Circuits

6 Avoidance of Disturbances on the System Bus

When inserting a new module in an operating system, the switching capacitance (Cs2 in Figure 3) of the individual signal lines at the interface must be charged to the instantaneous voltage on the corresponding bus line. These additional currents distort the signal that is being transmitted at that instant. Figure 7 shows the equivalent circuit that describes this situation. This involves switching a capacitor (Cs2 = 20 pF) into the middle of a bus line. The inductance of the connector contact (L_c = 30 nH) is in series with this capacitor. The line has an impedance (Z_O = 30 Ω) with a signal propagation time (t_p = 10 ns). It is terminated at both ends with resistors (R_t = 100 Ω) such that, in the quiescent state, a high level (V_h = 3 V) results. The circuit arrangement shown here conforms to conditions typically found with backplane wiring systems that are driven by TTL levels.

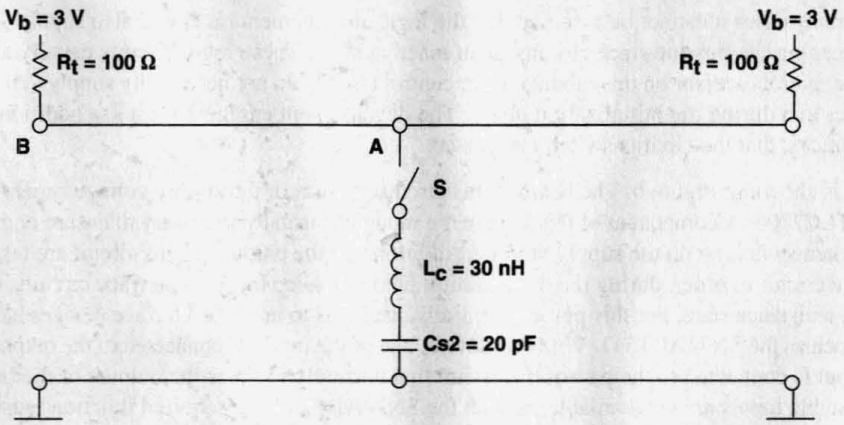


Figure 7. Connecting a Capacitor to a Line

Using the SPICE simulation program, the voltage waveform on the line was simulated at points A and B when closing switch S. Figure 8 shows the result. As expected, connecting capacitor Cs2 to the line at point A generates a voltage peak, which is already close to the threshold voltage (V_t = 1.5 V) of the receiver to which it is connected. The situation is even more critical at B (the end of the line). As a result of intentional mismatching at this point by the terminating resistors (R_t = 100 Ω), the amplitude of the disturbance increases such that the threshold voltage of the circuits at this point may be significantly exceeded. Considering the short response time of modern logic circuits (the delay time of the inverter in the bus-interface circuits is only a few hundred picoseconds), faulty operation of the circuits connected to the bus must be expected.

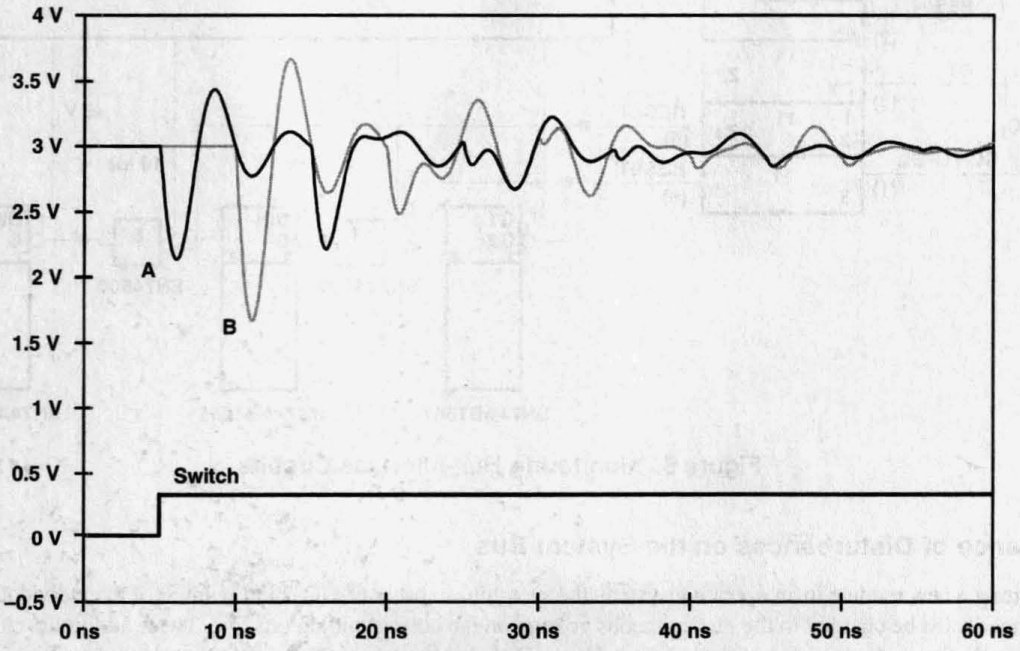


Figure 8. Voltage Peaks When Making Contacts to Signal Lines (Without Voltage Bias)

The amplitude of the interference voltage peaks can be reduced considerably if capacitor Cs2 is charged to the threshold voltage of the circuit via a high-value series resistor R_p (in the simulated circuit, R_p = 10 kΩ) before making contact. Cs2 is charged from an auxiliary voltage source (V_p) that corresponds approximately to the threshold voltage of the receiving circuits, i.e., typically V_p = 1.5 V. Figure 9 shows the corresponding circuit and Figure 10 shows that the interference voltage peaks have significantly reduced amplitude.

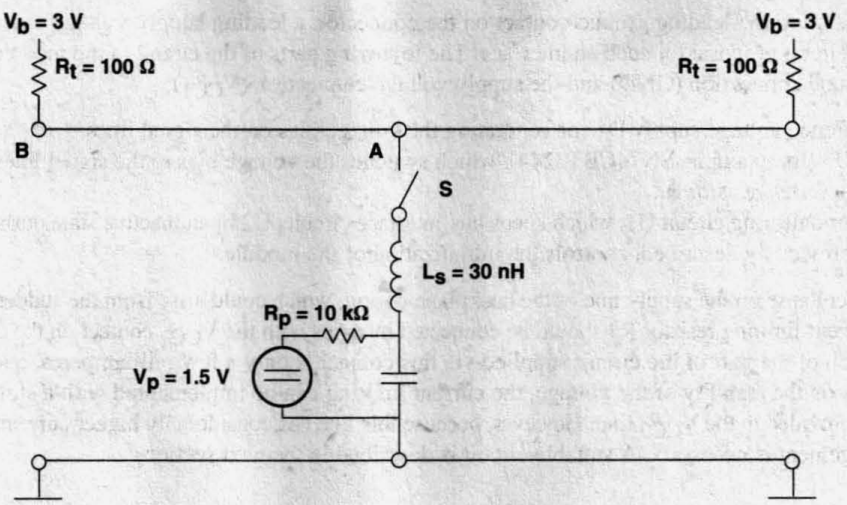


Figure 9. Connection of a Capacitor to a Line (With Voltage Bias)

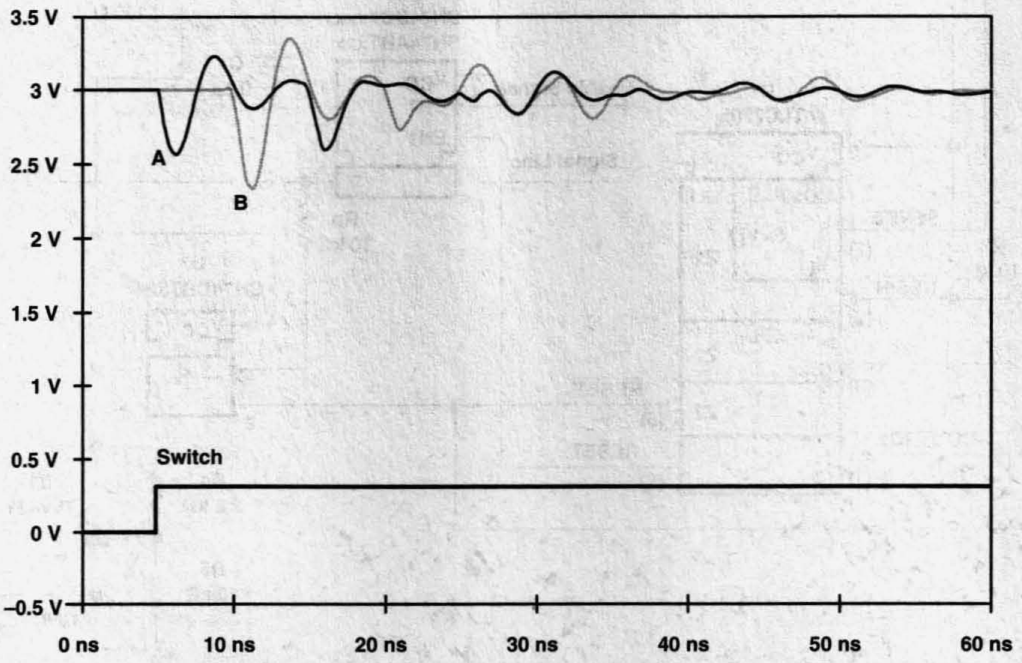


Figure 10. Voltage Peaks When Making Contacts to Signal Lines (With Voltage Bias)

Resistor R_p should have as high a value as possible to keep the loading of the bus during the module-insertion process as low as possible. However, the maximum value of the resistance is determined by the leakage current I_{off} of the circuit to be charged. This leakage current flowing through resistor R_p causes a voltage drop that must be added to the value of the voltage bias.

In practice, in addition to the leading ground contact on the connector, a leading supply-voltage contact must be provided. Figure 11 shows a circuit proposal for such an interface. The following parts of the circuit in the module are initially supplied via the leading ground connection (GND) and the supply voltage connection (V_{CC1}):

- The reference voltage supply D1 for generating the voltage bias on the signal lines
- Switch U3 (for example, SN74CBT3244), which switches the voltage bias to the signal lines during the switch-on phase via series resistor R_p
- Voltage-monitoring circuit U1, which keeps bus-interface circuits U2 in an inactive state during the switch-on phase and, as previously described, controls the initialization of the module.

To avoid a voltage collapse on the supply line of the backplane wiring, which could arise from the sudden charging of blocking capacitor C1, a current-limiting resistor R3 should be connected in series with the V_{CC1} contact on the connector. Because the current consumption of the part of the circuit supplied via this contact is only a few milliamperes, and because it places no excessive demands on the stability of the voltage, the current limiting can be implemented with a simple resistor. A similar filter must also be provided in the V_{CC2} line. However, because this line has considerably higher currents, a significantly more complicated arrangement is necessary. A suitable circuit is described in the next section.

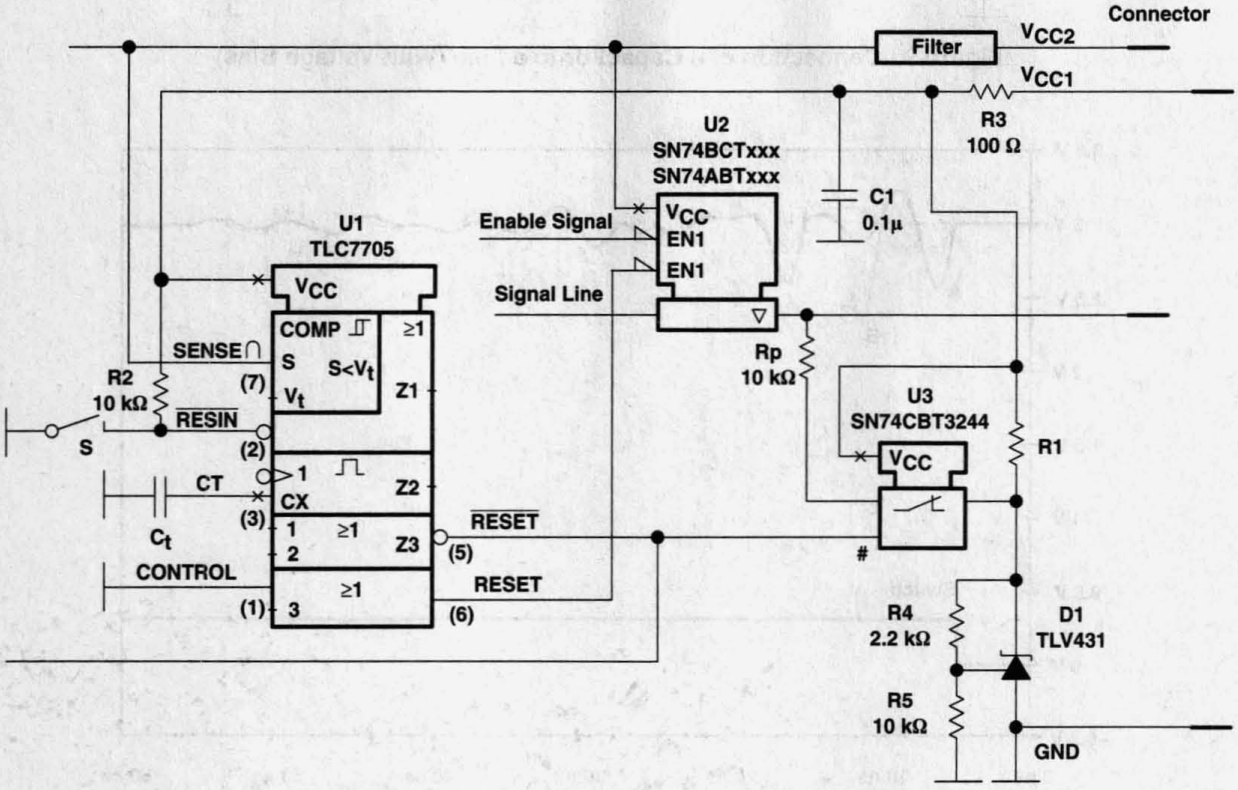


Figure 11. Generation of the Voltage Bias and Control of the Interface

Because supply voltage V_{CC2}, which must power the bus-interface circuits and all other circuits on the module, has not been applied at this instant, outputs of monitor circuit U1 are active, i.e., the voltage at its SENSE input is ≈ 0 V. The RESET output holds the bus-interface circuit U2 in an inactive state via enable input EN1. Simultaneously, the RESET signal closes the switch in circuit U3, so that the voltage bias supplied by the zener diode D1 via the decoupling resistor is applied to the signal lines. In addition, the RESET signal and, if necessary, the noninverting RESET signal, as well, are supplied to the other parts of the circuit on the module that need to be initialized when switching on. When the signal lines make contact as the module is inserted further, signal distortion on the system bus remains very low (see Figure 10). After V_{CC2} makes contact, the other parts of the circuit on the module are supplied with current. In the same way the potential at the SENSE input of circuit U1 rises to 5 V. After the elapsed time determined by timing capacitor C_t, the logic circuits on this module are in a defined initial state and can start operating. At this moment, switch U3 is again opened to avoid an additional loading of the signal lines by the resistors (R_s).

It is advantageous to make the signals delivered by voltage-monitoring circuit U1 independent of V_{CC1} and V_{CC2}. As a result of the contacts bouncing on the connector when inserting a module, undefined operating states can arise. For this reason, switch S at the inverting RESIN input of circuit U1 is provided, which is coupled with the mechanical interlock of the module. When a module is removed, unlatching this interlock automatically switches off logic circuits in the module. In this way, bus-interface circuits U2 also are immediately switched into an inactive state. Conversely, these circuits are held in an inactive state when inserting a new module until the interlock has been mechanically latched, and thus the correct mechanical insertion and defined contacting of the connector is ensured.

7 Special Bus-Interface Circuits

Integrating voltage bias, switches, and resistors into bus-interface circuits allows a significant reduction in the circuit complexity. This feature has been implemented in the enhanced transceiver logic (ETL), series SN74ABTE, and backplane transceiver logic (BTL), series SN74FB. The ETL circuits have been specified by the VITA working group, which has been concerned with the VME bus (ANSI/IEEE Standard 1014), while the BTL circuits are used in the FutureBus+ (IEEE Standard 896), among other applications.

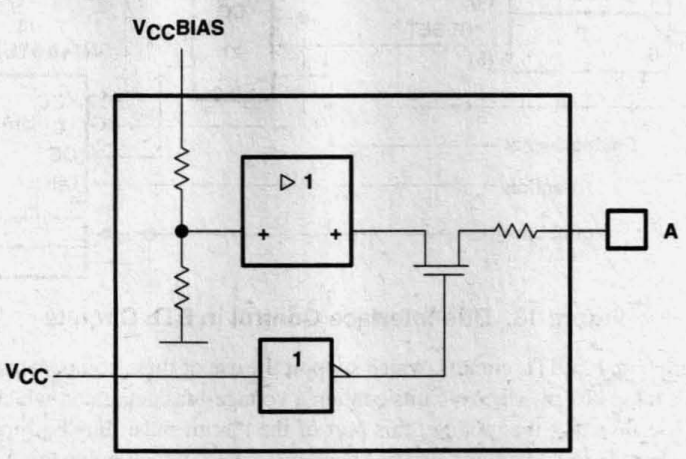


Figure 12. Generation of the Voltage Bias and Control in the SN74ABTE16245

The ETL circuits (for example, SN74ABTE16245) have an additional supply voltage connection (V_{CC}BIAS). This feeds the circuit, which generates the voltage bias mentioned above and, together with the V_{CC} connection, controls the switching on and off of the voltage bias. Figure 12 shows the simplified circuit diagram of this part of the circuit. It does not include the power-up 3-state circuit (see Figure 2), which also is contained in these bus-interface circuits, and which switches all outputs into the high-impedance state (3-state) at a supply voltage below about 2.5 V.

Figure 13 shows a bus interface with ETL circuits. At the moment the module is inserted, and after the connection of the V_{CC1}– and GND contacts, the generation of the voltage bias in the bus interface circuit U3 becomes effective. Voltage-monitoring circuit U1 is simultaneously switched on, which, via OR gate U2, switches the OE input of bus driver U3 to high; when the outputs of this circuit are inactive, this is the 3-state. Thus, the circuit remains in an inactive high-impedance state until initialization of the module has been completed. This also is the case after the V_{CC2} connector makes contact and this supply voltage has increased to the point that the power-up 3-state circuit in bus-interface circuit U3 is no longer effective. It also is advisable to control the end of the initialization phase by means of switch S, which should be coupled to the mechanical interlock of the module.

Before removing the module from a running system, this circuit must be brought to a definite inactive state. This also is performed with switch S, which closes when the module interlock is released. Thus, the outputs of bus-interface circuit U3 are automatically switched into the 3-state by circuits U1 and U2.

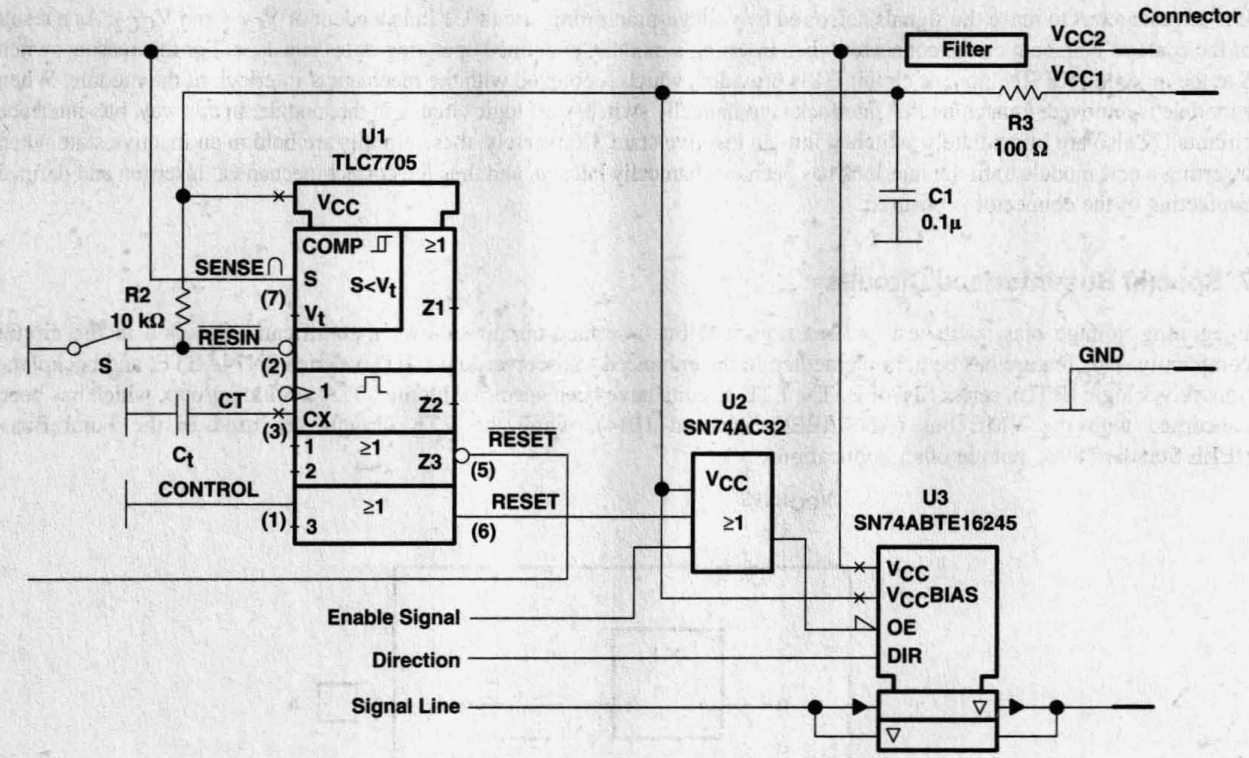


Figure 13. Bus-Interface Control in ETL Circuits

Additional circuit features are found in BTL circuits, which support the use of these components in the applications discussed here. As shown in Figure 12, these bus-interface circuits contain a voltage-bias generator, which is supplied with voltage via the BIASV_{CC} terminal. When inserting the module, this part of the circuit must thus be supplied with voltage (V_{CC1} in Figure 14). In addition, a power-up 3-state circuit also has been integrated, which holds the A and B outputs in an inactive high-impedance state (3-state), until the voltage at the V_{CC}– connections is < 2.5 V. The circuit design is simplified in that several of the BTL circuits for the control of the B outputs, which are taken to the backplane wiring, are provided with two enable inputs. One of the two inputs is monitored by the bus control, while the other input is controlled by the voltage-monitoring circuit. By eliminating an additional OR gate (U2 in Figure 13) the component complexity is reduced. It is more important that, because of the delay time of this gate, about 5 ns are saved.

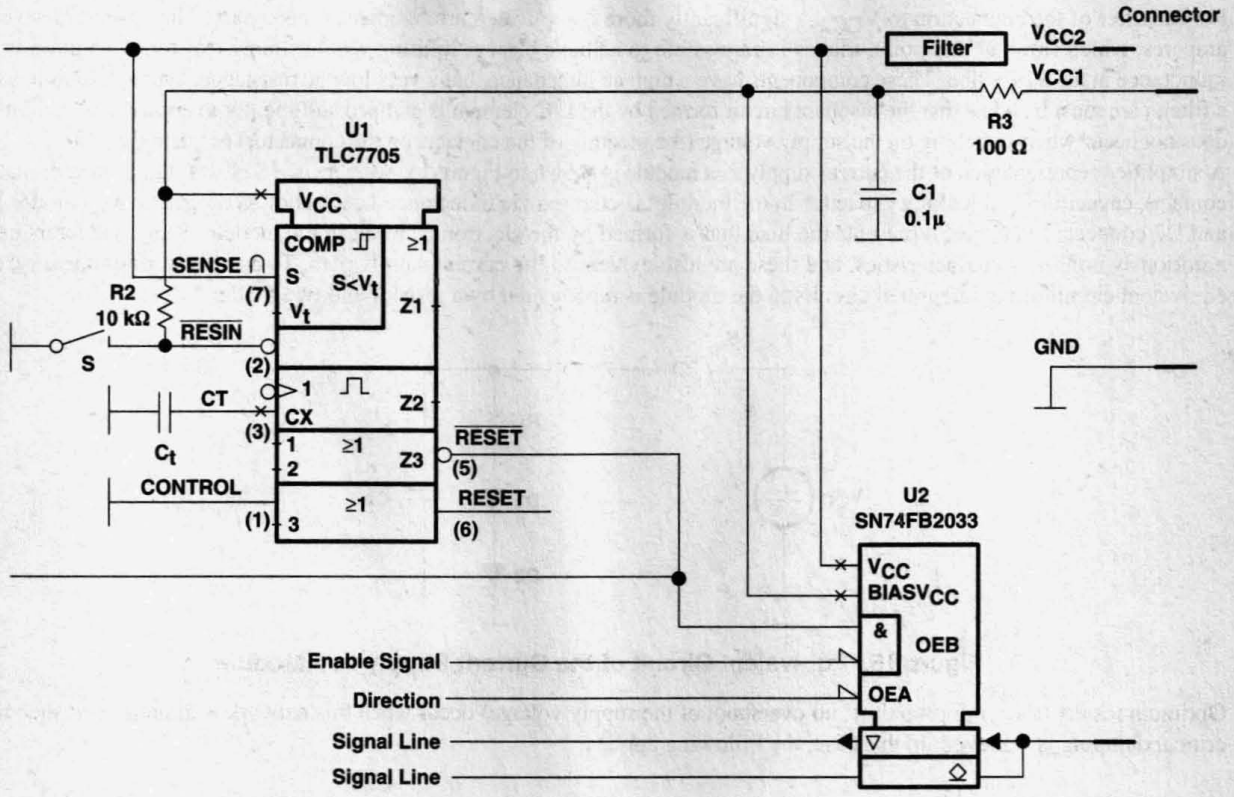


Figure 14. Bus-Interface Control With BTL Circuits

8 Avoidance of Disturbances to the Supply Voltage

Disturbances on the supply voltage lines of a system can occur as a result of charging the line capacitance in the same way as when switching the signal lines to the bus. When a module is inserted in a slot, the large capacitance of this circuit must first be charged. This capacitance is dictated primarily by the blocking capacitor on the circuit board where values of several tens to hundreds of µF are used. Another source of interference is the load on the module, which causes a considerable change of current, and hence voltage, when switching on the supply voltage. This problem is easily solved with the leading supply-voltage connector (V_{CC1} in Figures 13 and 14). Because the part of the circuit fed via this connector has a current consumption of only a few milliamperes, it is easy to implement current limiting at switch on with resistor R3 in Figures 13 and 14. Minor reductions of voltage are acceptable because the CMOS circuits in question can operate over a wide range of supply voltage.

The only question to be answered here is, what is the time constant ($t_d = R3 \times C1$)?, for example, see Figure 14. This time constant determines the rise time of V_{CC1}, and this voltage must have reached its nominal value before the lagging connections are made to V_{CC2}. The time that is available for the build up of V_{CC1} should be estimated. For this purpose, assume that the insertion distance of a module in a module carrier is $D_m = 15$ cm, that the leading contacts protrude by $D_c = 1.5$ mm, and that the time during which the module is being inserted is $t_i = 0.1$ s. Under these conditions, the leading contacts make contact about 1 ms before the subsequent ones. As shown by the applicable mechanical factors, these times are much longer than the time constant of the previously mentioned R/C network.

For the filter of the connection to V_{CC2}, a significantly more complicated arrangement is necessary. The current of several amperes, which flows at this point, makes it impossible to achieve current limiting with a simple resistor. A solution is an inductance in the V_{CC2} line. These components have a high ac impedance, but a very low dc resistance. When designing such a filter, care must be taken that the resonant circuit formed by the L/C element is damped sufficiently to ensure that oscillation does not occur when switching on the supply voltage (the meeting of the contacts on the connector) or when the load changes. A simplified representation of the current supply to a module is shown in Figure 15. After switch S closes (the connector makes contact), capacitor C_b (blocking capacitor in the module) is charged via inductance L. Resistor R_L, together with diodes D1 and D2 connected in series, represents the load that is formed by the electronic circuit in the module. Semiconductors have notoriously nonlinear characteristics, and these are also evident in the current supply path. To account for nonlinearity, the equivalent circuit of the integrated circuits in the module is represented by a resistor and two diodes.

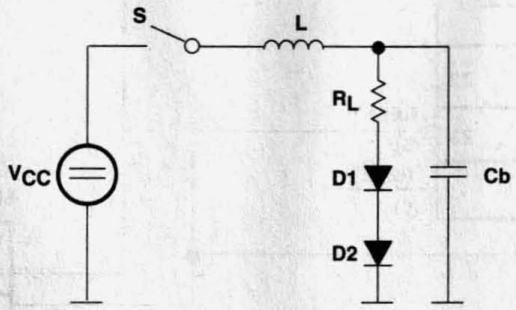


Figure 15. Equivalent Circuit of the Current Supply to a Module

Optimum results (short ramp-up time, no overshoot of the supply voltage) occur when this network is dimensioned such that critical damping is achieved. In this case, the following applies:

$$2 \times R_L = \sqrt{\frac{L}{C_b}} \quad (2)$$

The inductance can be calculated as follows:

$$L = 4 \times R_L^2 \times Cb \quad (3)$$

With a load resistor of $R_L = 1\ \Omega$ and a capacitor $C_b = 50$ mF, this expression applies:

$$L = 4 \times 1^2\Omega^2 \times 50\ \mu F = 200\ \mu H \quad (4)$$

Figure 16 shows the waveform of the supply voltage with various degrees of damping. It shows the following situations:

- Overshoot ($Q > 1$) : $L < 4 \times R_L^2 \times C_b$ ($R_L = 1\ \Omega$, $C_b = 50\ \mu F$, $L = 50\ \mu H$)
- Critical damping ($Q = 1$) : $L = 4 \times R_L^2 \times C_b$ ($R_L = 1\ \Omega$, $C_b = 50\ \mu F$, $L = 200\ \mu H$)
- Overdamping ($Q < 1$) : $L > 4 \times R_L^2 \times C_b$, ($R_L = 1\ \Omega$, $C_b = 50\ \mu F$, $L = 800\ \mu H$)

In the above calculations, the diodes in series with resistor R_L are ignored. This results in the curve (shown in Figure 16 as a case of critical damping) still showing a slight overshoot. In practice, this simplification of the calculations is permissible because the differential resistance of the diodes is usually small compared to resistor R_L. In addition, to avoid an overshoot of the supply voltage, inductance L is made sufficiently large to ensure that, in the worst case, overdamping occurs. In many applications, a problem is then presented by the mechanical dimensions of inductance L, which must be designed to carry high currents.

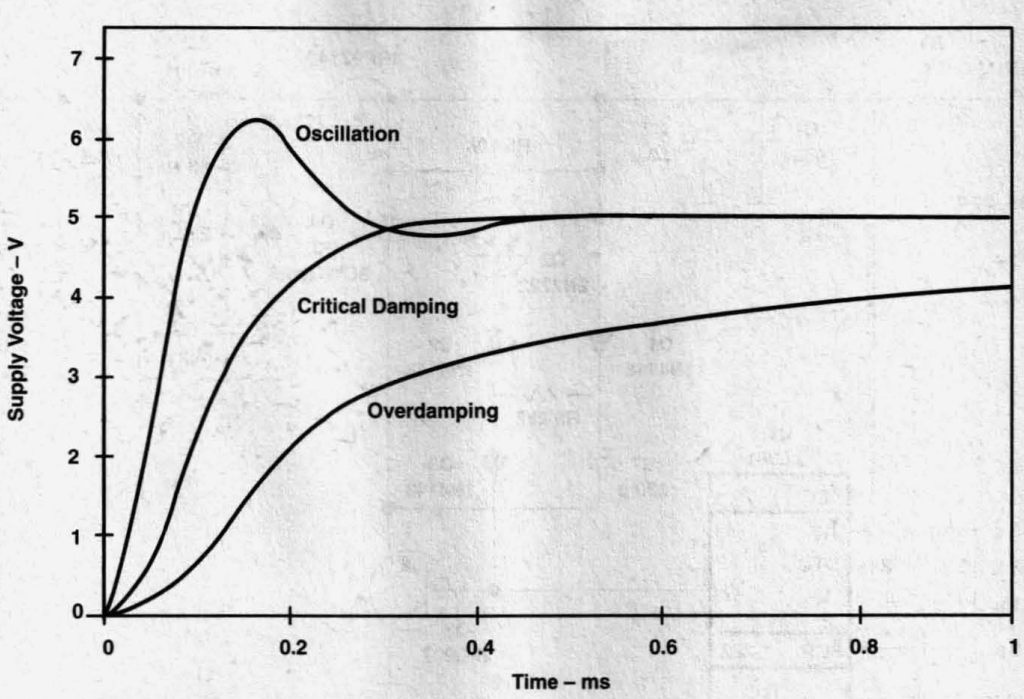


Figure 16. Transient Behavior of the Supply Voltage at Switch On, With Various Degrees of Damping

Another way to limit the switch-on current when inserting a module consists of inserting a semiconductor switch, which switches on slowly, in the supply line. Figure 17 shows such an arrangement. In this case, P-channel MOS transistor Q is used as a switch, an R/C network (R1, Cd) in the gate circuit of this transistor, ensuring that the latter switches on slowly. Diode D ensures that the capacitor discharges rapidly when the module is withdrawn.

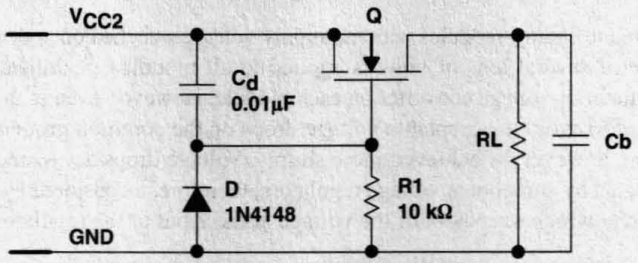


Figure 17. Switch-On Delay Circuit Using a MOS Transistor

When considering transistor Q, one with a low on-resistance (R_{DSon}) should be chosen to avoid an excessive voltage drop across this component. It may be necessary to use several transistors in parallel. Because the power dissipation is exceptionally low when in operation (as a result of the low voltage drop), transistors in the SO package, such as the TPS1101PW, also are suitable at this point in the circuit.

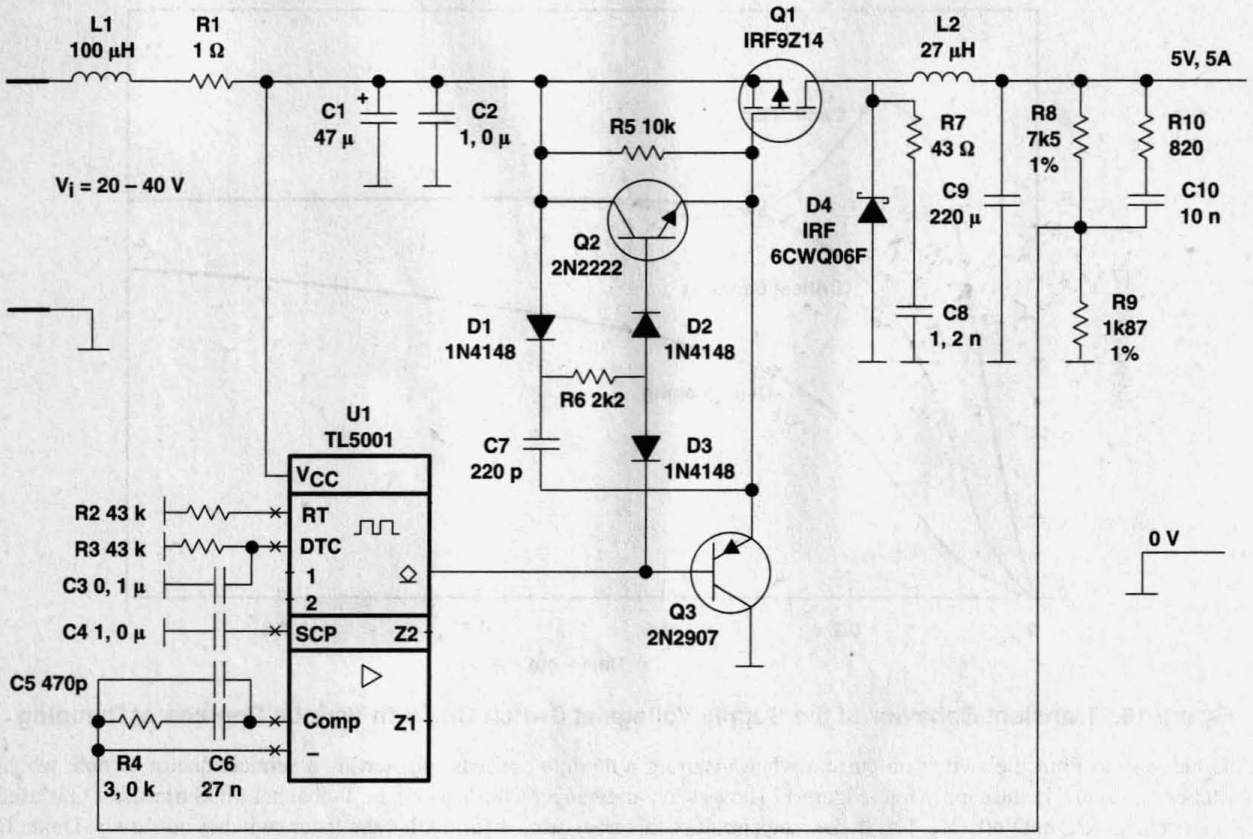


Figure 18. Decentralized Power Supply With Limiting of Switch-On Current

In equipment where it is required to change modules with the supply voltage switched on, a decentralized power supply is often used. An unstabilized voltage of several tens of volts is applied to all modules. Stabilization of the operating voltage is performed by a switching regulator or voltage converter on each module. However, even in this case, limiting of the switch-on current also should be provided to avoid unacceptable voltage drops on the common ground line (GND). The requirements of these parts of the circuit can, however, be achieved more simply. Voltage drops across inductances are not so significant, because these can be compensated by subsequent voltage regulators; therefore, a considerably smaller inductance can be used. Operating the filter in a region in which overshoot of the voltage at the input to the regulator occurs is acceptable.

Figure 18 shows a proposed circuit for a decentralized current supply of this kind. The switch-on current limiting is again performed with the help of the inductance L1 at the input. Damping of the switch-on process is implemented with resistor R1 in series with the inductor. Integrated circuit TL5001 is used as the switching regulator. More detailed information regarding the use of this component can be found in the corresponding data sheets and application reports.

9 Summary

When exchanging modules in electronic equipment whose supply voltage must remain switched on, the development engineer must make circuit modifications to avoid damage to the circuit and to prevent disturbances in the operation of the equipment.

The first requirement (avoiding damage) can be met comparatively easily. In this case, it is necessary only to ensure that, when a module is inserted, no undefined currents flow into the integrated circuits at the interfaces. In addition, the destruction of the interface circuits as a result of undefined states when the circuits are switched on (bus conflicts) must be prevented and can be achieved with the following precautions:

- Leading ground contacts (GND) on the connector
- Use of interface circuits that remain at a high resistance when the supply voltage is switched off. All circuits in the bipolar and BiCMOS logic families meet this requirement (see Table 1).
- Appropriate circuit modifications must be made to prevent undefined states at the outputs of the interface circuits (bus conflicts) when the supply voltage is switched on. Bus-interface circuits from the series ABT, BCT, and LVT are provided with a power-up 3-state circuit, which, in many cases, provides adequate protection. It is safer to switch the interface circuits during the start-up phase so that they are forced into an inactive state (see Figure 6), by means of an additional voltage-monitoring circuit on the module being inserted. Experience has shown that it is advisable to take this precaution, not only when modules must be inserted while the supply voltage is switched on, but because bus conflicts also arise when the system is switched on under normal conditions.

If there is the additional requirement that an operating system not be disturbed when a module is removed or inserted (live insertion), circuit design is much more complicated and the following requirements must be met:

- Leading supply voltage contacts (GND and V_{CC}) on the connector
- Exclusive use of interface circuits that are provided with a power-up 3-state circuit [series ABT, BCT, and LVT (see Table 1)]. These circuits ensure that, even with supply voltages < 2 V, the bus-interface circuits remain in an inactive high-resistance state.
- With suitable circuit modifications, undefined states of the outputs of the interface circuits (bus conflicts) must be avoided when the supply voltage is further increased. A supply-voltage monitoring circuit on the module being inserted is essential to maintain the interface circuits in an inactive high-impedance state during the switch-on phase.
- Control both the enabling and the deactivation of the circuit on the module (including the bus-interface circuits) with a switch that is coupled to the mechanical interlocking of the module.
- Ensure by suitable circuit modifications that, before making contact, the signal lines of the module being inserted are charged to a voltage (pre-charge) that lies approximately halfway between the high and low logic levels on the backplane wiring. This avoids disturbances on the system bus. Bus-interface circuits from the series BTL and ETL are provided with such integrated pre-charge circuits.
- Ensure a slow rise of the supply current when a module is inserted to prevent the rapid charging (giving the effect of a short-circuit) of the capacitors in a module when the module is inserted. This precaution ensures that no unacceptable interference voltages (ground bounce) arise on the ground line (GND) of the backplane wiring and a collapse of the voltage on the power-supply line of the system also is avoided.

If modules must be exchanged while the supply voltage remains on (live insertion), the engineer developing the system must account for a number of operating states, particularly during insertion. If suitable precautions are taken and the correct components are chosen, it is possible to not only prevent damage to parts of the circuit, but, more significantly, operation of the system is not adversely affected by removing or inserting modules.

The precautions that isolate a module from the system logic when the module is removed and reinserted in the system have not been covered in this report. Results of these tasks must be controlled by the operating system of the computer, a discussion that is far beyond the scope of this application report.

Acknowledgment

Eilhard Haseloff is the author of this application report.

General Design Considerations 1
Backplane Design 2
Device-Specific Design Aspects 3
5-V Logic Design 4
3.3-V Logic Design 5
Clock-Distribution Circuits (CDC) 6
Boundary-Scan IEEE Std 1149.1 (JTAG) Logic 7
Packaging 8
Index 9

Contents

	Page
Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices	3–3
Implications of Slow or Floating CMOS Inputs	3–17
Input and Output Characteristics of Digital Integrated Circuits	3–33
Metastable Response in 5-V Logic Circuits	3–71
Timing Measurements With Fast Logic Circuits	3–87
Designing With the SN54/74LS123	3–127
Digital Phase-Locked Loop Design Using SN54/74LS297	3–147

Family of Curves Demonstrating Output Skews for Advanced BiCMOS Devices

SCBA006A
December 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**3–7**
Skews	**3–7**
Source of Data	**3–7**
Sources of Error in Data	**3–8**
Summary	**3–8**

List of Illustrations

Figure	*Title*	*Page*
1	Skew = $\lvert t_{PLH14} - t_{PLH3} \rvert$	3–8
2	'ABT16240 – Single Switching	3–9
3	'ABT16240 – Simultaneous Switching	3–10
4	'ABT16245 – Single Switching	3–11
5	'ABT16952 – Single Switching	3–12
6	'ABT16500A – Single Switching	3–13
7	'ABT16500A – Simultaneous Switching	3–14
8	'ABT244 – Single Switching	3–15
9	'ABT244 – Multiple-Output Switching	3–16

Introduction

The data in this application report demonstrates the skew between the outputs of a sample of Texas Instruments Advanced BiCMOS (ABT) devices. This report explains which output skew is being examined, where the data comes from, and how the data is analyzed. Some of the errors that may be present in the data are discussed.

Skews

Skew is a term that defines the difference in time between two signal edges. Several different types of skew being used are defined in JEDEC 99 clause 2.3.5.

Output Skew [$t_{sk(o)}$] – The difference between two concurrent propagation delay times that originate at either a single input or two inputs switching simultaneously and terminating at different outputs.

Input Skew [$t_{sk(i)}$] – The difference between two propagation delay times that originate at different inputs and terminate at a single output.

Pulse Skew [$t_{sk(p)}$] – The difference between the propagation delay times t_{PLH} and t_{PHL} when a single switching input causes one or more outputs to switch.

Process Skew [$t_{sk(pr)}$] – The difference between identically specified propagation delay times on any two samples of an IC at identical operating conditions.

Limit Skew [$t_{sk(l)}$] – The difference between: 1) The greater of the maximum specified values of t_{PLH} and t_{PHL} and 2) The lesser of the minimum specified values of t_{PLH} and t_{PHL}.

The skew discussed here is the skew of propagation delays across the outputs of a device. More specifically, it is the difference between the largest value obtained for a propagation delay and the smallest value across all of the outputs. For example, if output 3 has the largest propagation delay t_{PLH} and output 14 has the smallest, the output skew for this device would be the difference between the propagation delays for output 3 and output 14 (see Figure 1).

The majority of the curves presented in this paper consist of data taken on devices that have one output switching at a time. This produces a skew that should not be confused with the defined data-sheet skew $t_{sk(o)}$. The data-sheet value for $t_{sk(o)}$ is found by switching all of the outputs simultaneously. Two of the devices examined in this paper ('ABT16240 and 'ABT16500A) include curves that present $t_{sk(o)}$ data.

Source of Data

The data used to produce the curves presented in this paper was extracted from the characterization data bases used to prepare the data sheets for the devices presented. The sample size of the data base is approximately 30 devices for each characterization lot (wafer) used.

The data was sorted so that the maximum skew for each device at a particular V_{CC} and temperature combination could be determined. Next, the maximum skew values were averaged to produce a data point for each transition. Further statistical analysis of this data was performed to calculate a standard deviation of the maximum skew across the devices. This value was then used to produce a three-standard-deviation data point for each V_{CC} and temperature combination. The data is presented as a family of curves across V_{CC}, with each member of the family being an output skew versus temperature curve. The curves for each device are broken out by output transition (i.e., t_{PLH}, t_{PHL}). Each transition is further separated into a set of curves depicting the average skew across the devices and a set representing the average skew, plus three standard deviations.

For those devices ('ABT16952 and 'ABT16500A) that have registers, the data path chosen for each device was the path that put the device in a transparent mode. Also, for the bidirectional devices ('ABT16245, 'ABT16952, and 'ABT16500A), the A-to-B direction was used.

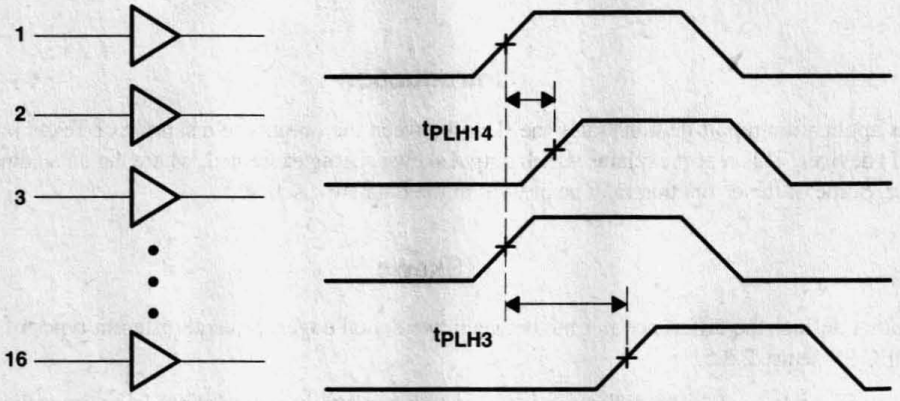


Figure 1. Skew = $|t_{PLH14} - t_{PLH3}|$

Sources of Error in Data

The data in this report was taken on an IMPACT tester, which is automatic test equipment used to characterize integrated circuits. The tester is offset using a golden unit that has had data taken on a laboratory bench setup. The offsetting process is the main source of error in the data.

Briefly, the tester is offset in the following manner. The golden unit has its propagation delay measurements taken at 25°C and 85°C using a pulse generator as the source and an oscilloscope as the measurement device. The golden unit is then placed on the IMPACT and the data is again taken. The difference between the two values is the offset. The 25°C offsets are used for the data taken at –55°C, –40°C, and 25°C, while the 85°C offsets are used at 85°C and 125°C.

Great care is taken during this process to ensure that the induced error is kept to a minimum. For example, the boards are checked before use to ensure the output loads are correct, the oscilloscope is calibrated each day, and the input signals are closely monitored to ensure that the intended signal is delivered to the golden unit.

This reduction in error is quite important in this application because the average skews for the devices are about 200 ps. A 20-ps error in offsets translates into an approximate error of 10% in the output skew data. However, it can be seen in the curves presented here that the error has been kept to a minimum and that the curves are fairly well behaved.

Summary

The family of curves presented in Figures 2 through 9 demonstrates that the Texas Instruments Advanced BiCMOS family of devices can be expected to produce an average skew between outputs that remain below 400 ps for devices with single switching outputs. Also, when a device's outputs switch simultaneously, the average skew across the outputs can be expected to remain below 700 ps.

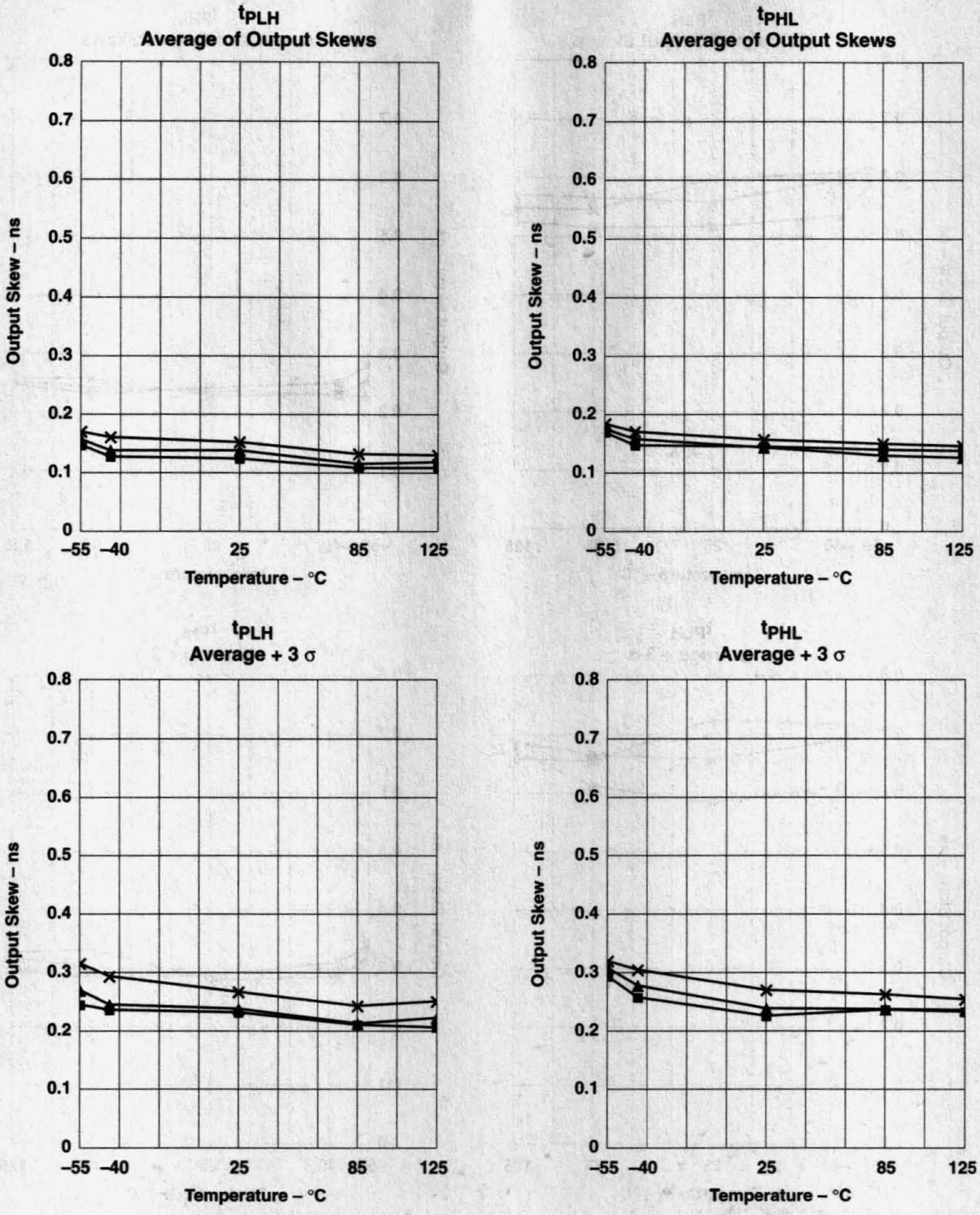


Figure 2. 'ABT16240 – Single Switching

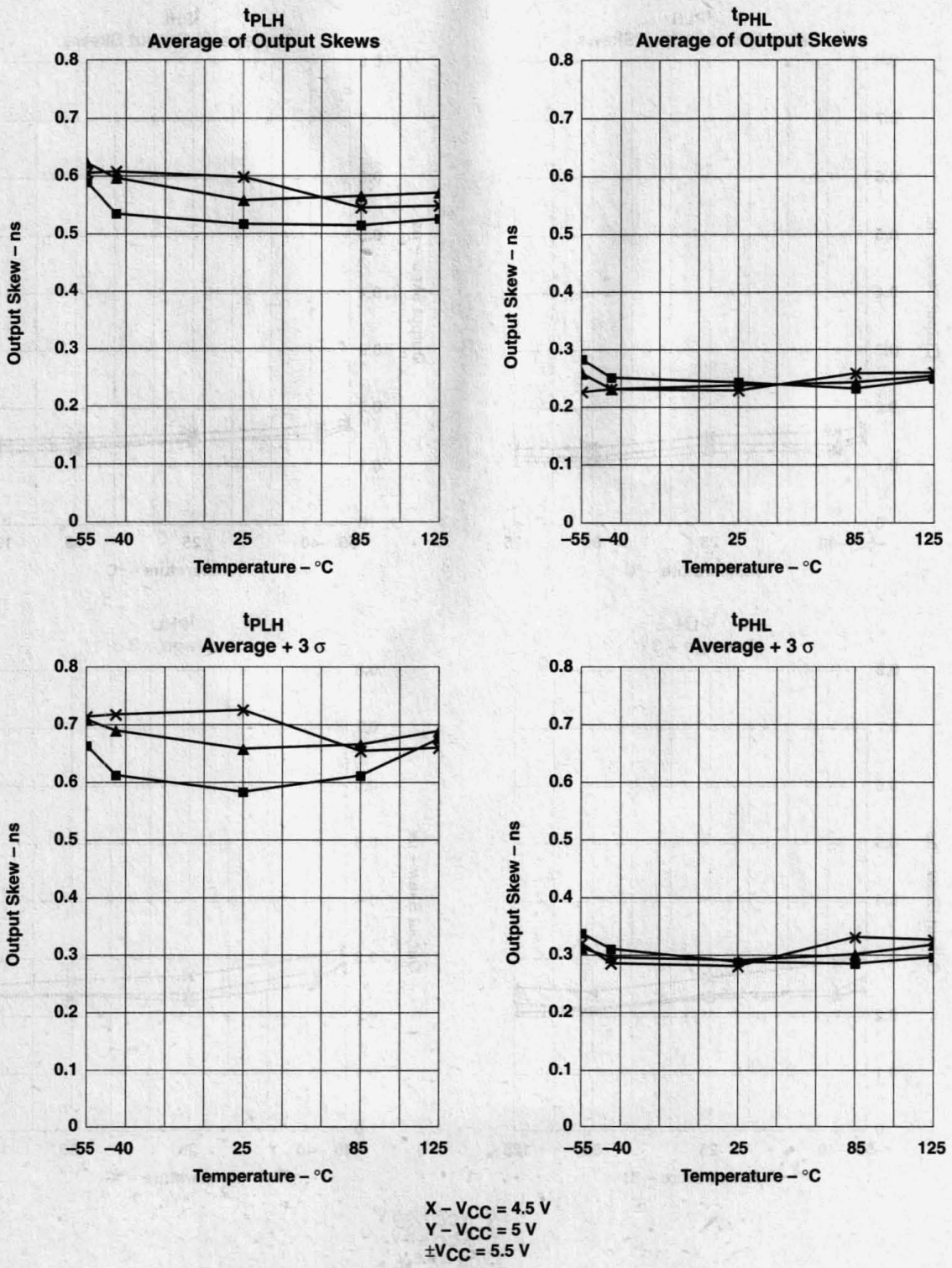


Figure 3. 'ABT16240 – Simultaneous Switching

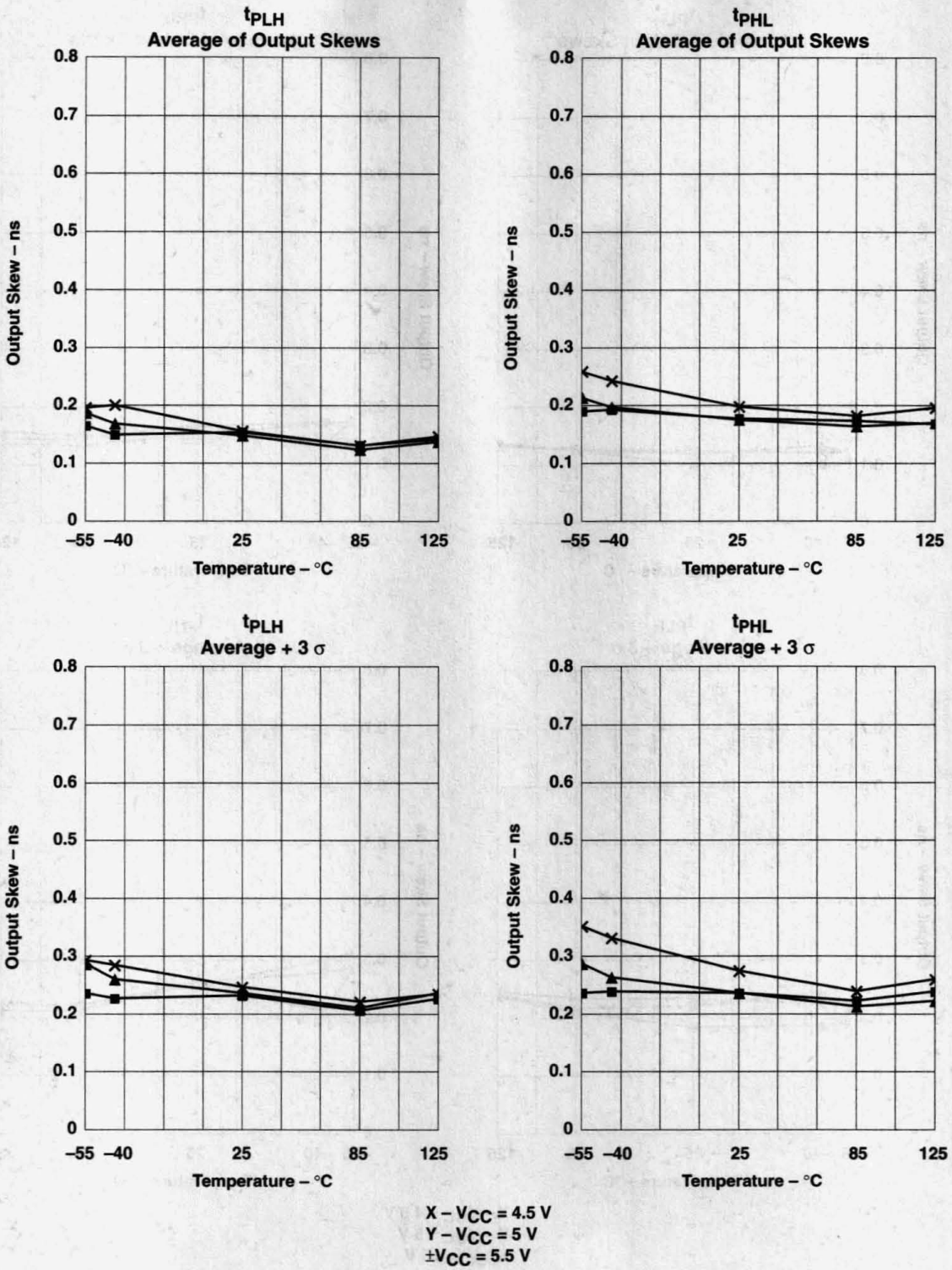


Figure 4. 'ABT16245 – Single Switching

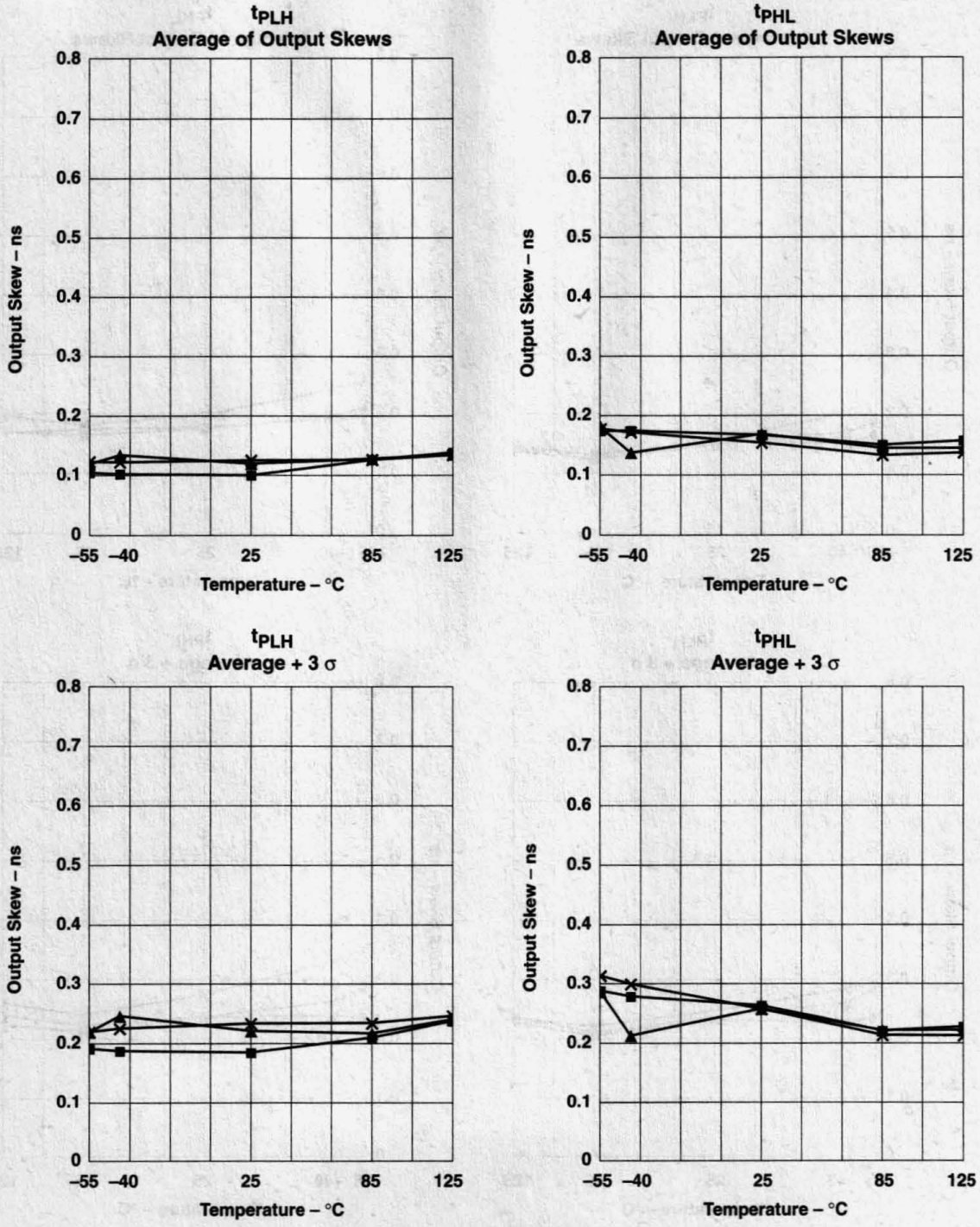


Figure 5. 'ABT16952 – Single Switching

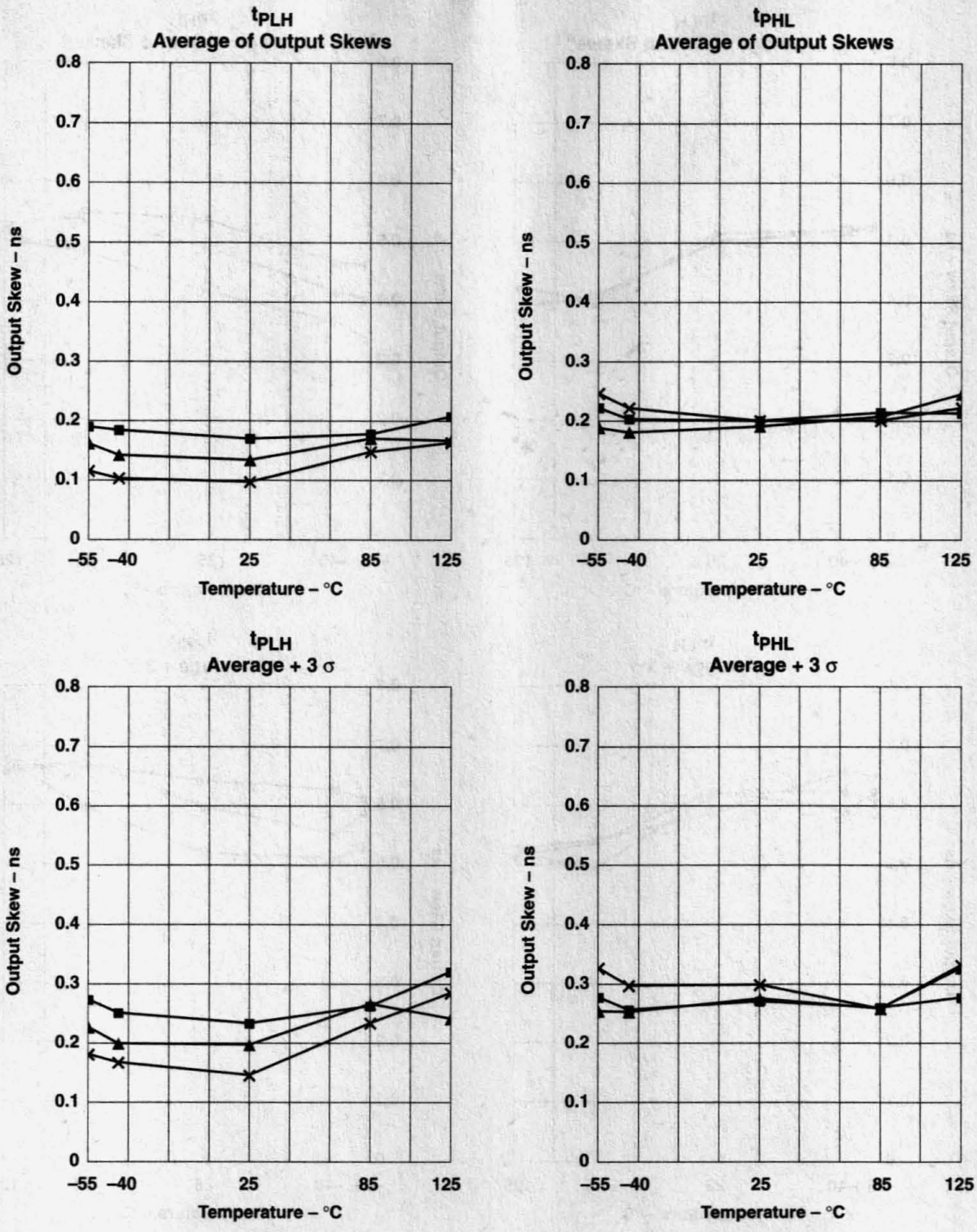


Figure 6. 'ABT16500A – Single Switching

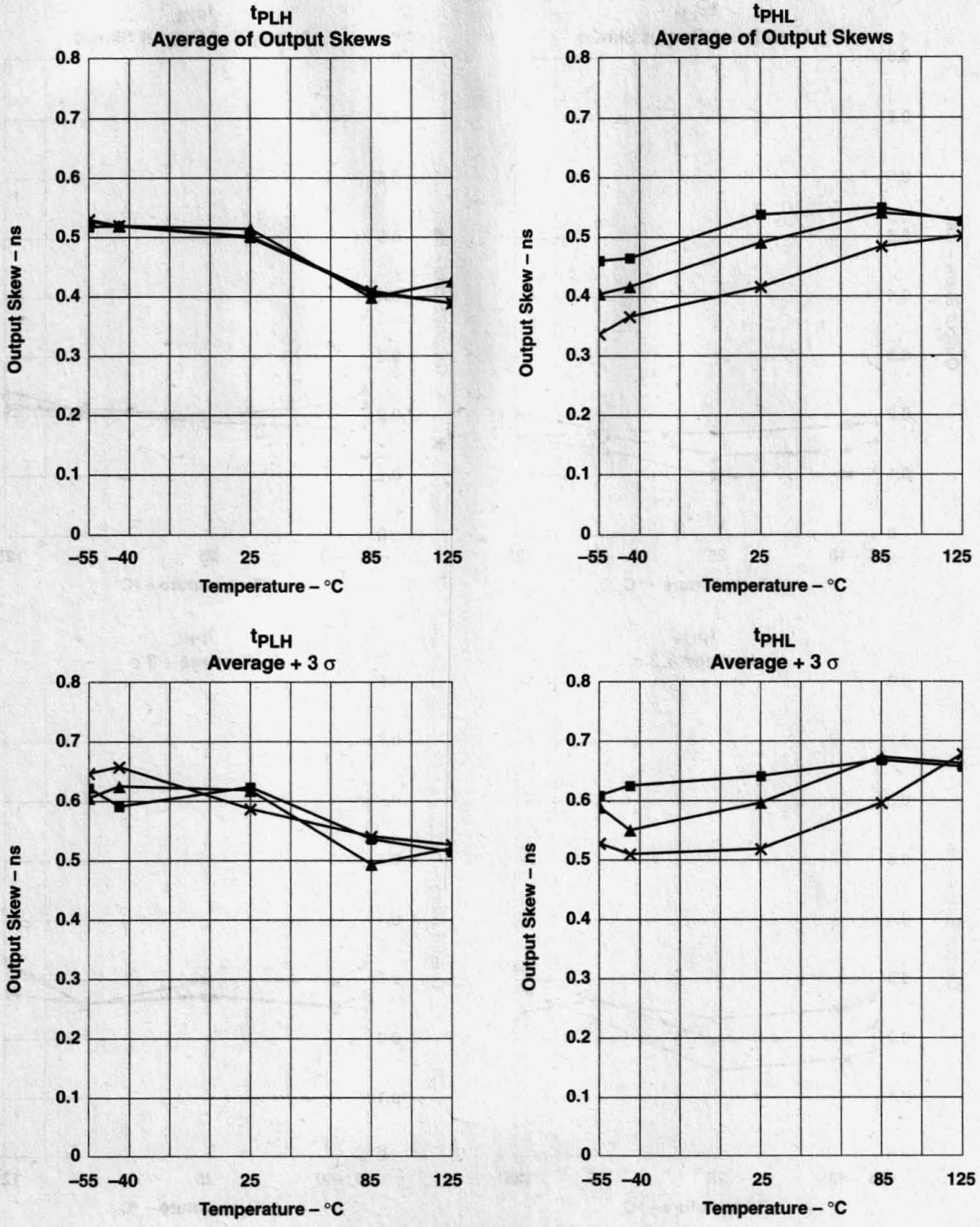


Figure 7. 'ABT16500A – Simultaneous Switching

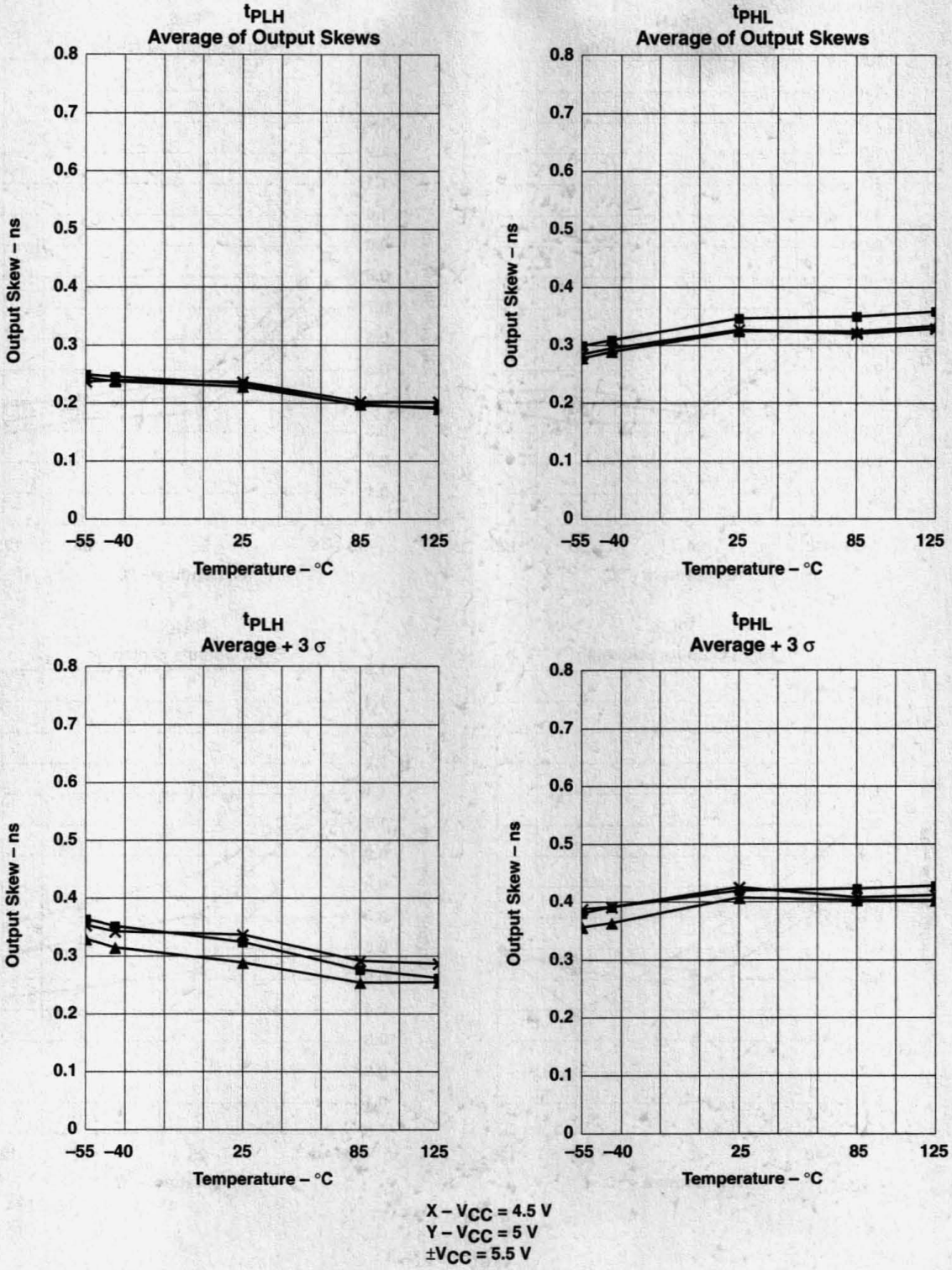
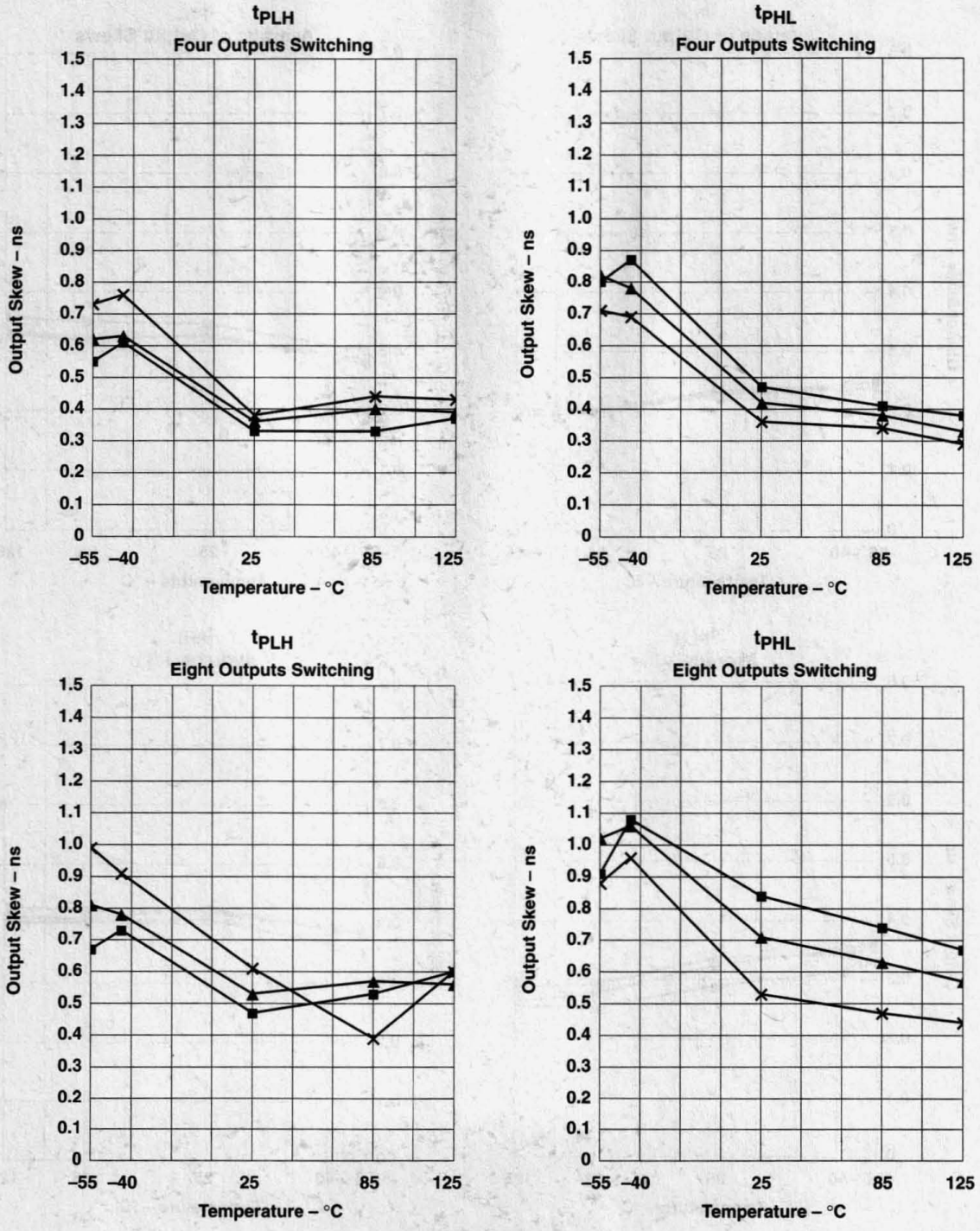


Figure 8. 'ABT244 – Single Switching



X – V_{CC} = 4.5 V
Y – V_{CC} = 5 V
±V_{CC} = 5.5 V

Figure 9. 'ABT244 – Multiple-Output Switching

Implications of Slow or Floating CMOS Inputs

SCBA004A
March 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**3–21**
Characteristics of Slow or Floating CMOS Inputs	**3–21**
Slow Input Edge Rate	**3–22**
Floating Inputs	**3–23**
Recommendations for Designing More Reliable Systems	**3–24**
Bus Control	3–24
Pullup or Pulldown Resistors	3–25
Bus-Hold Circuits	3–26
Summary	**3–32**

List of Illustrations

Figure	*Title*	*Page*
1	Input Structures of ABT and LVT/LVC Devices	3–21
2	Supply Current Versus Input Voltage (One Input)	3–22
3	Input Transition Rise or Fall Rate as Specified in Data Sheets	3–22
4	Input/Output Model	3–23
5	Supply-Current Change of the Input at TTL Level as Specified in Data Sheets	3–23
6	Supply Current Versus Input Voltage (36 Inputs)	3–24
7	Typical Bidirectional Bus	3–24
8	Inactive-Bus Model With a Defined Level	3–25
9	Typical Bus-Hold Cell	3–26
10	Stand-Alone Bus-Hold Cell (SN74ACT107x)	3–26
11	Diode Characteristics (SN74ACT107x)	3–27
12	Input Structure of ABT/LVT and ALVC/LVC Families With Bus Hold	3–28
13	Bus-Hold Input Characteristics	3–29
14	Driver and Receiver System	3–30
15	Output Waveforms of Driver With and Without Receiver Bus Hold	3–30
16	Bus-Hold Supply Current	3–30
17	Input Power With or Without Bus Hold at Different Frequencies	3–31
18	Data-Sheet Minimum Specification for Bus Hold	3–32

Widebus and Widebus+ are trademarks of Texas Instruments Incorporated.

Introduction

In recent years, CMOS (AC, ACT, LVC) and BiCMOS (ABT, LVT) logic families have further strengthened their position in the semiconductor market. New designs have adopted both technologies in almost every system that exists, whether it is a PC, a workstation, or a digital switch. The reason is very obvious: power consumption is becoming a major issue in today's market. However, when designing systems using CMOS and BiCMOS devices, one must understand the characteristics of these families and the way inputs and outputs behave in systems. It is very important for the designer to follow all rules and restrictions that the manufacturer requires, as well as to design within the data-sheet specifications. Because data sheets do not cover the input behavior of a device in detail, this application note explains the input characteristics of CMOS and BiCMOS families in general. It also explains ways to deal with problem issues when designing with such families where floating inputs are a concern. Understanding the behavior of these inputs results in more robust designs and better reliability.

Characteristics of Slow or Floating CMOS Inputs

Both advanced CMOS and BiCMOS (ABT/LVT) families have a CMOS input structure. This structure is an inverter consisting of a p-channel to V_{CC} and an n-channel to GND as shown in Figure 1. With low-level input, the p-channel transistor is on and the n-channel is off, causing current to flow from V_{CC} and pulling the node to a high state. With high-level input, the n-channel transistor is on and the p-channel is off and the current flows to GND, pulling the node low. In both cases, no current flows from V_{CC} to GND. However, when switching from one state to another, the input crosses the threshold region, causing the n-channel and the p-channel to turn on simultaneously, generating a current path between V_{CC} and GND. This current surge can be damaging, depending on the length of time that the input is in the threshold region (0.8 to 2 V). The supply current (I_{CC}) can rise to several milliamperes per input, peaking at approximately 1.5 V V_I (see Figure 2). This is not a problem when switching states at the data-sheet-specified input transition time (see Figure 3).

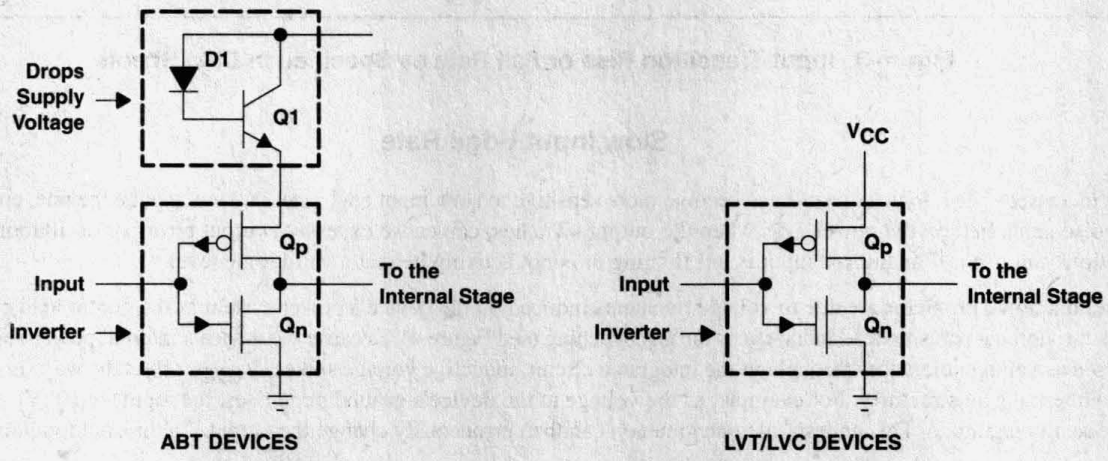


Figure 1. Input Structures of ABT and LVT/LVC Devices

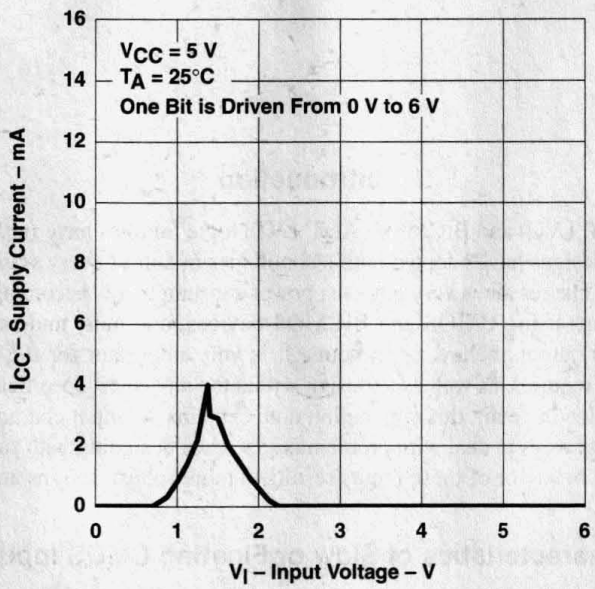


Figure 2. Supply Current Versus Input Voltage (One Input)

recommended operating conditions

			MIN	MAX	UNIT
$\Delta t/\Delta v$	Input transition rise or fall rate	ABT octals		5	ns/V
		ABT Widebus™ and Widebus+™		10	
		LVT, LVC, ALVC		10	
		LV		100	

Figure 3. Input Transition Rise or Fall Rate as Specified in Data Sheets

Slow Input Edge Rate

With increased speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output errors or oscillations. Similar situations can occur if an unused input is left floating or is not actively held at a valid logic level.

These functional problems are due to voltage transients induced on the device's power system as the output load current (I_O) flows through the parasitic lead inductances during switching (see Figure 4). Because the device's internal power-supply nodes are used as voltage references throughout the integrated circuit, inductive voltage spikes, V_{GND}, affect the way signals appear to the internal gate structures. For example, as the voltage at the device's ground node rises, the input signal, V_I', appears to decrease in magnitude. This undesirable phenomenon can then erroneously change the output if a threshold violation occurs.

In the case of a slowly rising input edge, if the change in voltage at GND is large enough, the apparent signal, V_I', at the device will appear to be driven back through the threshold and the output will start to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents), the slow input edge will be repeatedly driven back through the threshold, causing the output to oscillate. Therefore, the maximum input transition time of the device should not be violated, so no damage to the circuit or the package can occur (refer to Figure 3 for the maximum transition rate for each family).

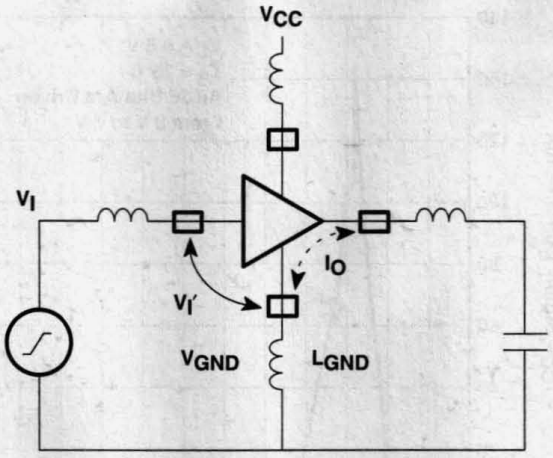


Figure 4. Input/Output Model

Floating Inputs

If a voltage between 0.8 V and 2 V is applied to the input for a prolonged period of time, this situation becomes critical and should not be ignored, especially with higher bit count and more dense packages (SSOP, TSSOP). For example, if an 18-bit transceiver had 36 I/O pins floating at the threshold, the current from V_{CC} could be as high as 150 to 200 mA. This is approximately 1 W of power consumed by the device, which leads to a serious overheating problem. This continuous overheating of the device affects its reliability. Also, because the inputs are in the threshold region, the outputs tend to oscillate, resulting in damage to the internal circuit over a long period of time. The data sheet shows the increase in supply current (ΔI_{CC}) when the input is at a TTL level [for ABT V_I = 3.4 V, ΔI_{CC} = 1.5 mA (see Figure 5)]. This becomes more critical when the input is in the threshold region as shown in Figure 6.

These characteristics are typical for all CMOS input circuits, including microprocessors and memories.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
ΔI_{CC}†	ABT	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		1.5	mA
	LVT	V_{CC} = 3 V to 3.6 V,	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND		0.2	
	LVC, ALVC, LV					0.5	

† This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Figure 5. Supply-Current Change of the Input at TTL Level as Specified in Data Sheets

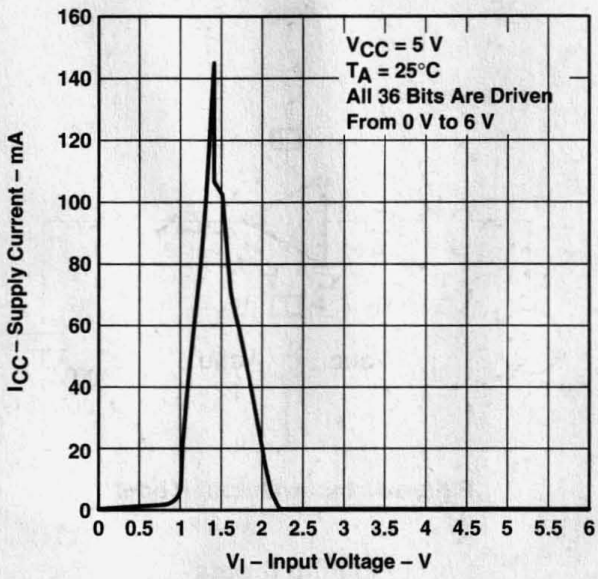


Figure 6. Supply Current Versus Input Voltage (36 Inputs)

As long as the driver is active in a transmission path or bus, the receiver's input is always in a valid state. No input specification is violated as long as the rise and fall times are within the data-sheet limits. However, when the driver is in a high-impedance state, the receiver input is no longer at a defined level and tends to float. This situation can worsen when several transceivers share the same bus. Figure 7 is an example of a typical bus system. When all transceivers are inactive, the bus-line levels are undefined. When a voltage that is determined by the leakage currents of each component on the bus is reached, the condition is known as a *floating state*. The result is a considerable increase in power consumption and a risk of damaging all components on the bus. Holding the inputs or I/O pins at a valid logic level when they are not being used or when the part driving them is in the high-impedance state is recommended.

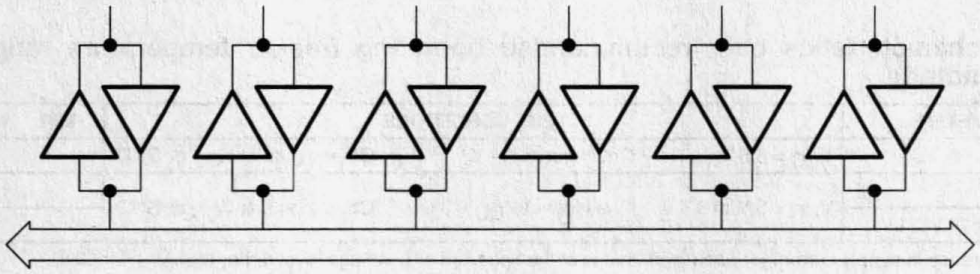


Figure 7. Typical Bidirectional Bus

Recommendations for Designing More Reliable Systems

Bus Control

The simplest way to avoid floating inputs in a bus system is to ensure that the bus is always either active or inactive for a limited time when the voltage buildup does not exceed the maximum V_{IL} specification (0.8 V for TTL-compatible input). At this voltage, the corresponding I_{CC} value is too low and the device operates without any problem or concern (see Figures 2 and 4).

To avoid damaging components, the designer must know the maximum time the bus can float. First, assuming that the maximum leakage current is I_{OZ} = 50 µA and the total capacitance (I/O and line capacitance) is C = 20 pF, the change in voltage with respect to time on an inactive line that exceeds the 0.8-V level can be calculated as in equation 1.

$$\Delta V/\Delta t = \frac{I_{OZ}}{C} = \frac{50\ \mu A}{20\ pF} = 2.5\ V/\mu s \quad (1)$$

The permissible floating time for the bus in this example should be reduced to 320 ns maximum, which ensures that the bus will not exceed the 0.8-V level specified above. The time constant does not change when multiple components are involved because their leakage currents and capacitances are summed.

The advantage of this method is that it requires no additional cost for adding special components. Unfortunately, this method does not always apply because buses are not always active.

Pullup or Pulldown Resistors

When buses are disabled for more than the maximum allowable time, other ways should be used to prevent components from being damaged or overheated. A pullup or a pulldown resistor to V_{CC} or GND, respectively, should be used to keep the bus in a defined state. The size of the resistor plays an important role and if its resistance is not chosen properly, a problem may occur. Usually, a 1-kΩ to 10-kΩ resistor is recommended. The maximum input transition time must not be violated when selecting pullup or pulldown resistors (see Figure 3). Otherwise, components can be destroyed.

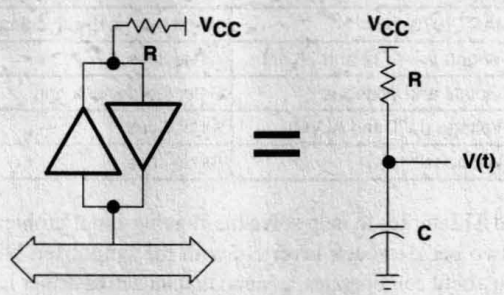


Figure 8. Inactive-Bus Model With a Defined Level

Assume that an active-low bus goes to the high-impedance state as modeled in Figure 8. C represents the device plus the bus-line capacitance and R is a pullup resistor to V_{CC}. The value of the required resistor can be calculated as in equation 2.

$$V(t) = V_{CC} - [e^{-t/RC} (V_{CC} - V_B)] \quad (2)$$

Where:

- $V(t)$ = voltage at time t
- V_B = 0.8 V, maximum allowable floating voltage
- V_{CC} = 5 V
- C = total capacitance
- R = pullup resistor
- t = maximum input rise time as specified in Figure 3 of the data sheet

Solving for R, the equation becomes:

$$R = \frac{t}{0.17 \times C} \quad (3)$$

For multiple transceivers on a bus:

$$R = \frac{t}{0.17 \times C \times N} \quad (4)$$

Where:

N = number of components connected to the bus

Assuming that there are ten components connected to the bus, each with a capacitance C = 20 pF requiring a maximum rise time of 10 ns/V and t = 50-ns total rise time for 5-V input, the maximum resistor size can be calculated:

$$R = \frac{50 \text{ ns}}{0.17 \times 20 \text{ pF} \times 10} = 1.5 \text{ k}\Omega \quad (5)$$

This pullup resistor method is recommended for ac-powered systems; however, it is not recommended for battery-operated equipment because power consumption is very critical. Instead, use the bus-hold feature that is discussed in the next section. The overall advantage of using pullup resistors is that they ensure defined levels when the bus is floating and help eliminate some of the line reflections because resistors can act as bus terminations as well.

Bus-Hold Circuits

The most effective method to provide defined levels for a floating bus is to use Texas Instruments (TI) built-in bus-hold feature on selected families or as an external component like the SN74ACT1071 and SN74ACT1073 (refer to Table 1).

Table 1. Devices With Bus Hold

DEVICE TYPE	BUS HOLD INCORPORATED
SN74ACT1071	10-bit bus hold with clamping diodes
SN74ACT1073	16-bit bus hold with clamping diodes
ABT Widebus+™ (32 and 36 bit)	All devices
ABT Octals and Widebus™	Selected devices only
Low Voltage (LVT and ALVC)	All devices
LVC Widebus™	All devices

Bus hold is a circuit used in selected TI families to help solve the floating-input problem and eliminate the need for pullup and pulldown resistors. It consists of two back-to-back inverters with the output fed back to the input through a resistor (see Figure 9). To understand how the bus-hold cell operates, assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit. Now, the driver goes to the high-impedance state and the bus-hold circuit holds the high level through the feedback resistor. The current requirement of the bus hold is determined only by the leakage current of the circuit. The same condition applies when the bus is in the low state and then goes inactive.

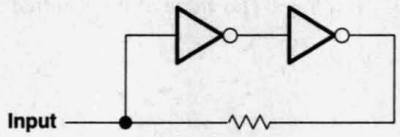


Figure 9. Typical Bus-Hold Cell

As mentioned previously in this section, TI offers the bus hold as stand-alone 10-bit and 16-bit devices (SN74ACT1071 and SN74ACT1073) with clamping diodes to V_{CC} and GND for added protection against line reflections caused by impedance mismatch on the bus. Because purely ohmic resistors cannot be implemented easily in CMOS circuits, a configuration known as a transmission gate is used as the feedback element (see Figure 10). An n-channel and a p-channel are arranged in parallel between the input and the output of the buffer stage. The gate of the n-channel transistor is connected to V_{CC} and the gate of the p-channel is connected to GND. When the output of the buffer is high, the p-channel is on, and when the output is low, the n-channel is on. Both channels are of relatively small surface area — the on resistance from drain to source, R_{dson}, is about 5 kΩ.

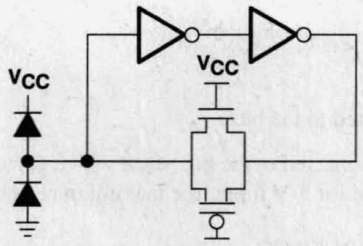


Figure 10. Stand-Alone Bus-Hold Cell (SN74ACT107x)

Now, assume that in a practical application the leakage current of a driver on a bus is I_{OZ} = 10 µA and the voltage drop across the 5 kΩ resistance is V_D = 0.8 V (this value is assumed to ensure a defined logic level). Then, the maximum number of components that a bus hold can handle is calculated as follows:

$$N = \frac{V_D}{I_{OZ} \times R} = \frac{0.8\ V}{10\ \mu A \times 5\ k\Omega} = 16\ \text{components} \quad (6)$$

The 74ACT1071 and 74ACT1073 also provide clamping diodes as an added feature to the bus hold. These diodes are useful for clamping any overshoot or undershoot generated by line reflections. Figure 11 shows the characteristics of the diodes when the input voltage is above V_{CC} or below GND. At V_I = –1V, the diode can source about 50 mA, which can help eliminate undershoots. This can be very useful when noisy buses are a concern.

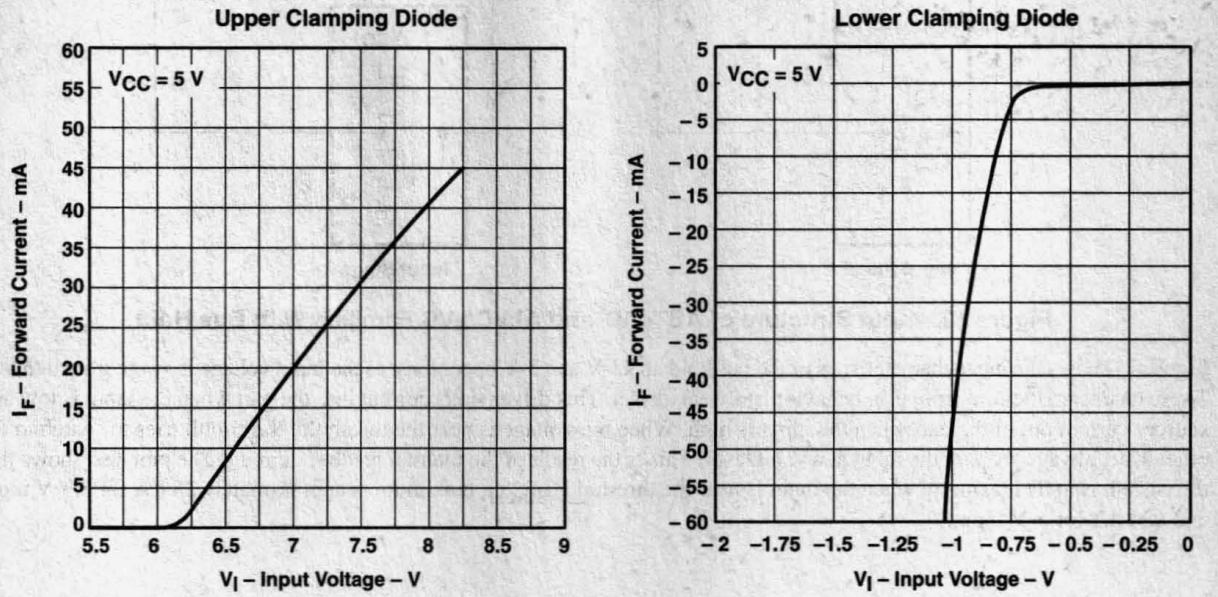


Figure 11. Diode Characteristics (SN74ACT107x)

TI also offers the bus-hold circuit as a feature added to some of the advanced-family drivers and receivers. This circuit is similar to the stand-alone circuit with a diode added to the drain of the second inverter (ABT and LVT only, see Figure 12). The diode blocks the overshoot current when the input voltage is higher than V_{CC} ($V_I > V_{CC}$), so only the leakage current is present. This circuit uses the device's input stage as its first inverter; a second inverter creates the feedback feature. The calculation of the maximum number of components that the bus hold can handle is similar to the previous example. However, the advantage of this circuit over the stand-alone bus hold is that it eliminates the need for external components or resistors that occupy more area on the board. This becomes very critical for some designs, especially when wide buses are used. Also, because cost and board-dimension restrictions are a major concern, designers prefer the easy fix: drop-in replaceable parts. TI offers this feature in most of the commonly used functions in several families (refer to Table 1 for more details).

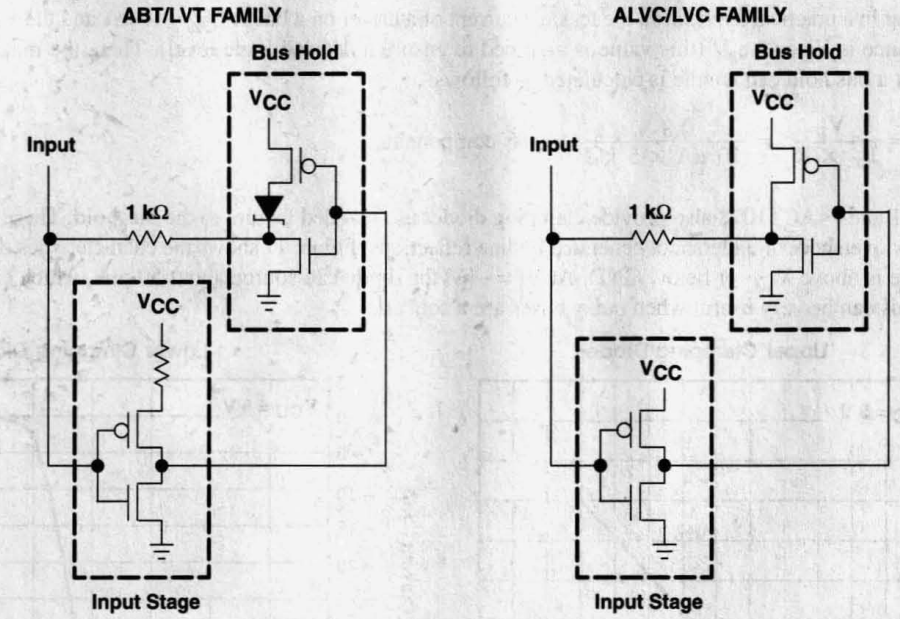


Figure 12. Input Structure of ABT/LVT and ALVC/LVC Families With Bus Hold

Figure 13 shows the input characteristics of the bus hold at 3.3-V and 5-V operations, as the input voltage is swept from 0 to 5 V. These characteristics are similar in behavior to a weak driver. This driver sinks current into the part when the input is low and sources current out of the part when the input is high. When the voltage is near the threshold, the circuit tries to switch to the other state, always keeping the input at a valid level. This is the result of the internal feedback circuit. The plot also shows that the current is at its maximum when the input is near the threshold. $I_{I(hold)}$ maximum is approximately 25 µA for 3.3-V input and 400 µA for 5-V input.

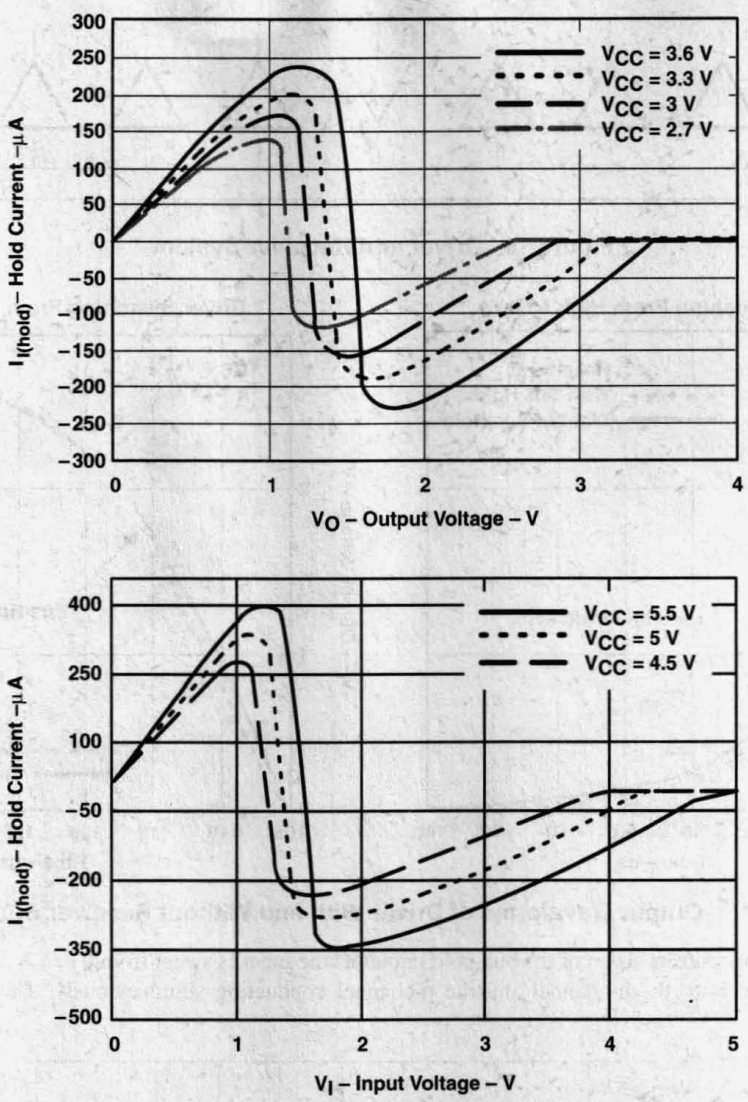


Figure 13. Bus-Hold Input Characteristics

When multiple devices with bus hold are driven by a single driver, one may be concerned about the ac switching capability of the driver becoming weaker. As small drivers, bus-hold cells require an ac current to switch them. This current is not significant when using TI CMOS and BiCMOS families. Figure 14 shows a 4-mA buffer driving six LVTH16244 devices. The trace is a 75-Ω transmission line. The receivers are separated by 1cm, with the driver located in the center of the trace. Figure 15 shows the bus-hold loading effect on the driver when connected to six receivers switching low or high. It also shows the same system with the bus hold disconnected from the receivers. Both plots show the effect of bus hold on the driver's rise and fall times. Initially, the bus hold tries to counteract the driver, causing the rise or fall time to increase. Then, the bus hold changes states (note the crossover point), which helps the driver switch faster, decreasing the rise or fall time.

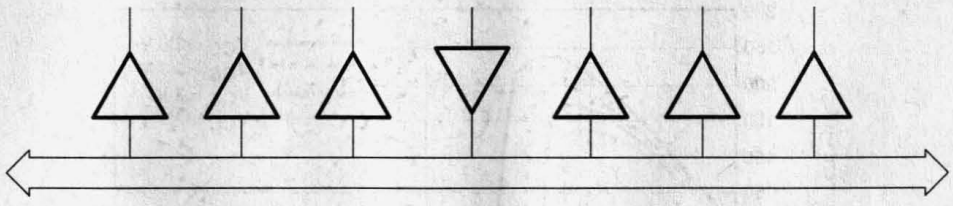


Figure 14. Driver and Receiver System

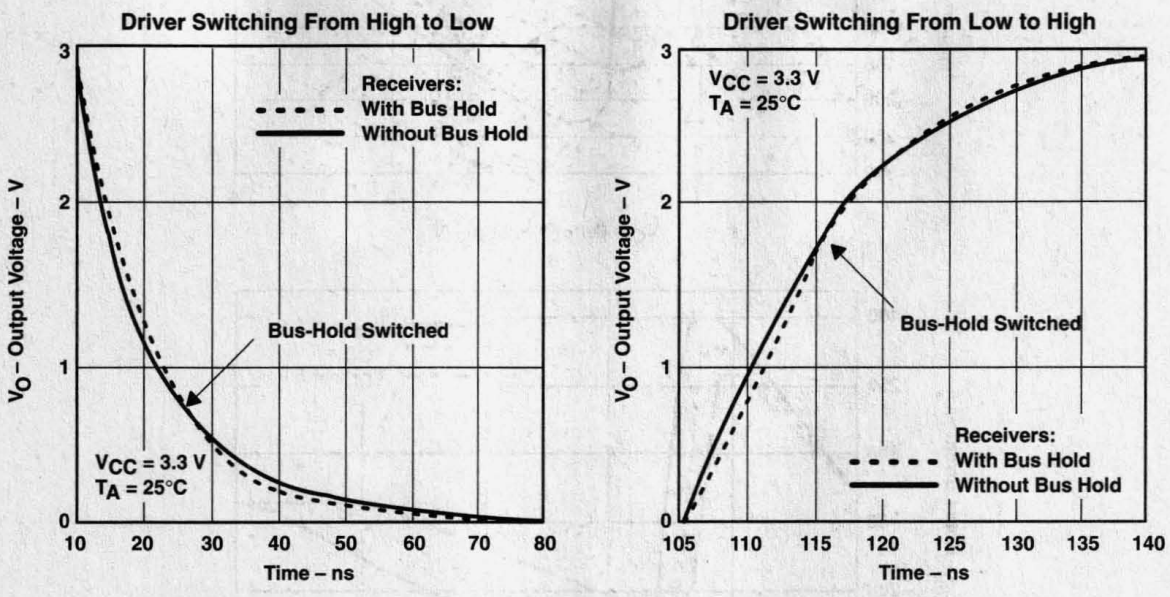


Figure 15. Output Waveforms of Driver With and Without Receiver Bus Hold

Figure 16 shows the supply current (I_{CC}) of the bus-hold circuit as the input is swept from 0 to 5 V. Again, the spike seen at about 1.5-V V_I is due to both the n-channel and the p-channel conducting simultaneously. This is one of the CMOS transistor characteristics.

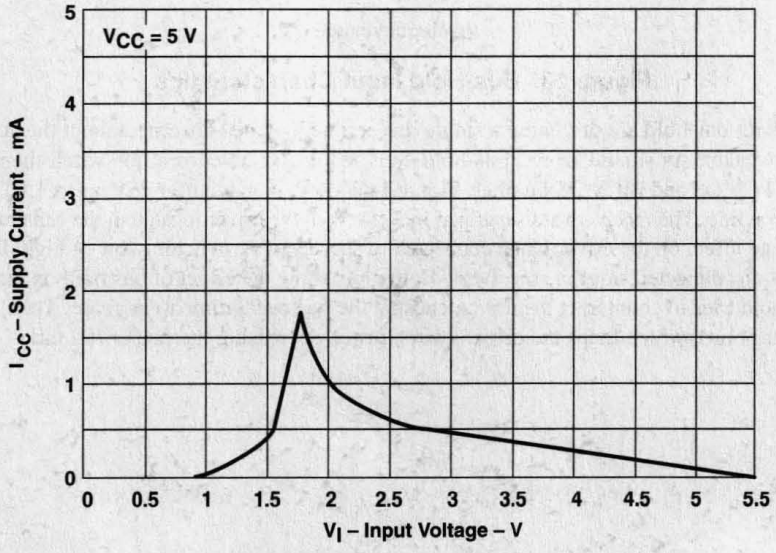


Figure 16. Bus-Hold Supply Current Versus Input Voltage

The power consumption of the bus hold is minimal when switching the input at higher frequencies. Figure 17 shows the power consumed by the input at different frequencies with or without bus hold. As shown, the increase in power consumption of the bus hold at higher frequencies is not significant enough to be considered in power calculations.

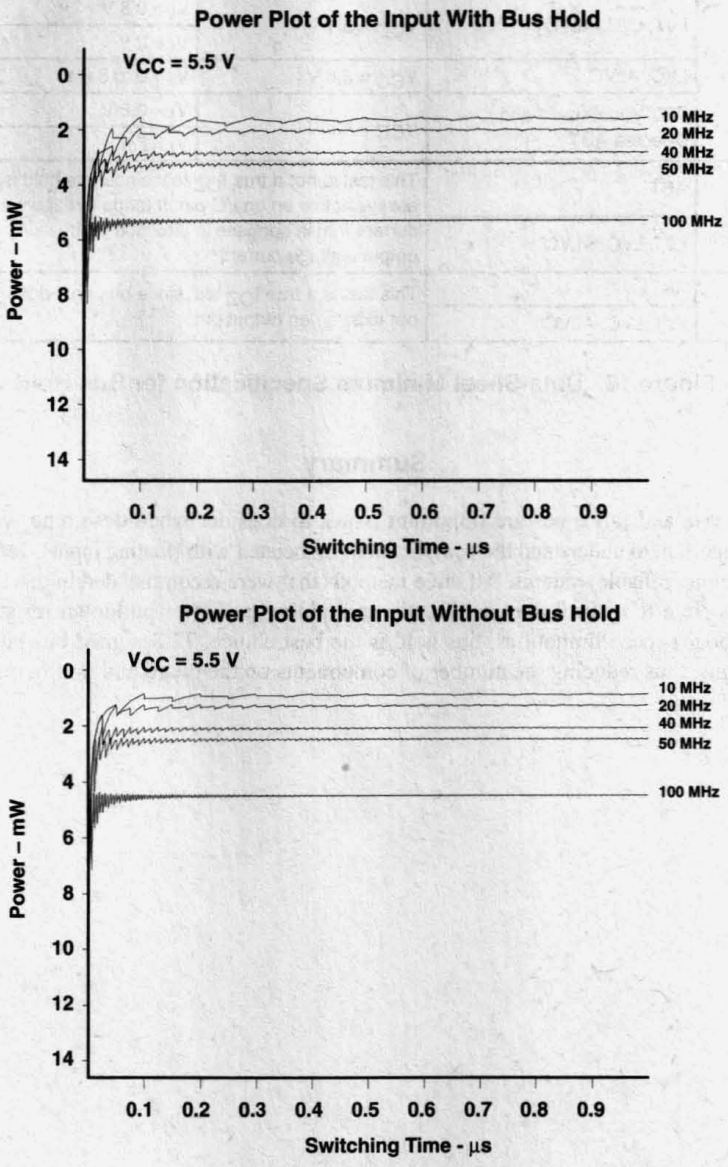


Figure 17. Input Power With or Without Bus Hold at Different Frequencies

Figure 18 shows the data sheet dc specifications for bus hold. The first test condition is the minimum current required to hold the bus at 0.8 V or 2 V. These voltages meet the specified low and high levels for TTL inputs. The second test condition is the maximum current that the bus hold sources or sinks at any input voltage between 0 V and 3.6 V (for low-voltage families) or between 0 V and 5.5 V (for ABT). The bus-hold current becomes minimal as the input voltage approaches the rail voltage. The output leakage currents, I_{OZH} and I_{OZL}, are insignificant for transceivers with bus hold because a true leakage test cannot be performed due to the existence of the bus-hold circuit. Because bus hold behaves as a small driver, it tends to source or sink a current that is opposite in direction to the leakage current. This situation is true for transceivers with bus hold only and does not apply to buffers. All LVT, ABT Widebus+™, and selected ABT octal and Widebus™ devices have the bus-hold feature (refer to Table 1 or contact the local TI sales office for more information).

electrical characteristics over recommended operating free-air temperature range (for families with bus-hold feature)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
$I_{I(hold)}$	Data inputs or I/Os	LVT, LVC, ALVC	V_{CC} = 3 V	V_I = 0.8 V	75		µA
				V_I = 2 V	–75		
		LVC, ALVC	V_{CC} = 3.6 V,	V_I = 0 to 3.6 V		±500	
		ABT Widebus+™ and selected ABT	V_{CC} = 4.5 V	V_I = 0.8 V	100		
				V_I = 2 V	–100		
I_{OZH}/I_{OZL}	Transceivers with bus hold	ABT	This test is not a true I_{OZ} test since bus hold is always active on an I/O pin. It tends to supply a current that is opposite in direction to the output leakage current.			±1	µA
		LVT, LVC, ALVC					
	Buffers with bus hold	ABT	This test is a true I_{OZ} test since bus hold does not exist on an output pin.			±10	
		LVT, LVC, ALVC				±5	

Figure 18. Data-Sheet Minimum Specification for Bus Hold

Summary

Floating inputs and slow rise and fall times are important issues to consider when designing with CMOS and advanced BiCMOS families. It is important to understand the complications associated with floating inputs. Terminating the bus properly plays a major role in achieving reliable systems. All three methods that were recommended in this application note should be considered. If it is not possible to control the bus directly and adding pullup or pulldown resistors is impractical due to power-consumption and board-space limitations, bus hold is the best choice. TI designed bus hold to reduce the need for resistors used in bus designs, thus reducing the number of components on the board and improving the overall reliability of the system.

Input and Output Characteristics of Digital Integrated Circuits

SDYA010
November 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	*Page*
Abstract	**3–39**
Introduction	**3–39**
Acknowledgment	**3–40**
Input Characteristics	**3–41**
Output Characteristics	**3–51**
Output Waveforms	**3–61**

List of Illustrations

Figure	*Title*	*Page*
1	Input Characteristics of the SN7400	3–41
2	Input Characteristics of the SN7440	3–41
3	Input Characteristics of the SN74LS00	3–41
4	Input Characteristics of the SN74LS40	3–42
5	Input Characteristics of the SN74LS240	3–42
6	Input Characteristics of the SN74S00	3–42
7	Input Characteristics of the SN74S40	3–43
8	Input Characteristics of the SN74S240	3–43
9	Input Characteristics of the SN74ALS00	3–43
10	Input Characteristics of the SN74ALS40	3–44
11	Input Characteristics of the SN74ALS240	3–44
12	Input Characteristics of the SN74ALS1004	3–44
13	Input Characteristics of the SN74AS00	3–45
14	Input Characteristics of the SN74AS240	3–45
15	Input Characteristics of the SN74AS1004	3–45
16	Input Characteristics of the SN74F00	3–46
17	Input Characteristics of the SN74F40	3–46
18	Input Characteristics of the SN74F240	3–46
19	Input Characteristics of the SN74HC00	3–47
20	Input Characteristics of the SN74HC240	3–47
21	Input Characteristics of the SN74AC11240	3–47
22	Input Characteristics of the SN74BCT240	3–48
23	Input Characteristics of the SN74BCT25240	3–48
24	Input Characteristics of the SN74ABT240	3–48
25	Input Characteristics of the SN74LV00	3–49

Widebus is a trademark of Texas Instruments Incorporated.

List of Illustrations (continued)

Figure	*Title*	*Page*
26	Input Characteristics of the SN74LV244	3–49
27	Input Characteristics of the SN74LVC244	3–49
28	Input Characteristics of the SN74ALVC16244	3–50
29	Input Characteristics of the SN74LVT244	3–50
30	Output Characteristics of the SN7400	3–51
31	Output Characteristics of the SN7440	3–51
32	Output Characteristics of the SN74LS00	3–51
33	Output Characteristics of the SN74LS40	3–52
34	Output Characteristics of the SN74LS240	3–52
35	Output Characteristics of the SN74S00	3–52
36	Output Characteristics of the SN74S40	3–53
37	Output Characteristics of the SN74S240	3–53
38	Output Characteristics of the SN74ALS00	3–53
39	Output Characteristics of the SN74ALS40	3–54
40	Output Characteristics of the SN74ALS240	3–54
41	Output Characteristics of the SN74ALS1004	3–54
42	Output Characteristics of the SN74AS00	3–55
43	Output Characteristics of the SN74AS240	3–55
44	Output Characteristics of the SN74AS1004	3–55
45	Output Characteristics of the SN74F00	3–56
46	Output Characteristics of the SN74F40	3–56
47	Output Characteristics of the SN74F240	3–56
48	Output Characteristics of the SN74HC00	3–57
49	Output Characteristics of the SN74HC240	3–57
50	Output Characteristics of the SN74AC11240	3–57
51	Output Characteristics of the SN74BCT240	3–58
52	Output Characteristics of the SN74BCT25240	3–58
53	Output Characteristics of the SN74ABT240	3–58
54	Output Characteristics of the SN74LV00	3–59
55	Output Characteristics of the SN74LV244	3–59
56	Output Characteristics of the SN74LVC244	3–59
57	Output Characteristics of the SN74ALVC16244	3–60
58	Output Characteristics of the SN74LVT244	3–60
59	Setup for Obtaining Output Waveforms	3–61
60	Waveforms of the SN7400	3–61
61	Waveforms of the SN7440	3–61
62	Waveforms of the SN74LS00	3–62
63	Waveforms of the SN74LS40	3–62
64	Waveforms of the SN74LS240	3–62

List of Illustrations (continued)

Figure	*Title*	*Page*
65	Waveforms of the SN74S00	3–63
66	Waveforms of the SN74S40	3–63
67	Waveforms of the SN74S240	3–63
68	Waveforms of the SN74ALS00	3–64
69	Waveforms of the SN74ALS40	3–64
70	Waveforms of the SN74ALS240	3–64
71	Waveforms of the SN74ALS1004	3–65
72	Waveforms of the SN74AS00	3–65
73	Waveforms of the SN74AS240	3–65
74	Waveforms of the SN74AS1004	3–66
75	Waveforms of the SN74F00	3–66
76	Waveforms of the SN74F40	3–66
77	Waveforms of the SN74F240	3–67
78	Waveforms of the SN74HC00	3–67
79	Waveforms of the SN74HC240	3–67
80	Waveforms of the SN74AC11240	3–68
81	Waveforms of the SN74BCT240	3–68
82	Waveforms of the SN74BCT25240	3–68
83	Waveforms of the SN74ABT240	3–69
84	Waveforms of the SN74LV00	3–69
85	Waveforms of the SN74LV244	3–69
86	Waveforms of the SN74LVC244	3–70
87	Waveforms of the SN74ALVC16244	3–70
88	Waveforms of the SN74LVT244	3–70

Abstract

This report contains a comprehensive collection of the input and output characteristic curves of typical integrated circuits from various logic families. These curves go beyond the information given in data sheets by providing additional details regarding the characteristics of the components. This knowledge is particularly useful when, for example, a decision must be made as to which circuit should be used in a bus system, or when the waveforms that can be expected in a transmission system need to be predicted by using a Bergeron chart. In addition, the waveforms at the outputs of these components are shown when loaded with a 50-Ω coaxial line, which is open circuited at the end of the line. These oscillograms are of great assistance when generating models for simulation programs that analyze the dynamic behavior of the integrated circuits in a particular environment.

Introduction

The parameters given in the data sheets of integrated circuits can give only a limited indication of their actual behavior in a system. Data sheets generally give only information regarding the behavior over an input and output voltage range of 0 to 5 volts. The output currents specified over this range provide an incomplete picture of the actual performance that can be expected from the device. Often the behavior outside the usually accepted operating conditions is of interest. This is, for example, the situation when the characteristic curves need to be used to predict the signal waveforms resulting from line reflections.

For requirements of this kind, the most important input and output characteristic curves of logic circuits are shown in the figures that follow. In view of the wide range of integrated circuits that are available, it has been necessary to limit this information to typical characteristics only. As a result, the input and output characteristics of the following circuits have been shown as being representative of other components which have similar circuit behavior:

'00: The characteristic curves of this NAND gate are representative of all logic circuits having normal drive capability, such as gates, flip-flops, counters, multiplexers, etc.

'40: For a range of applications, gates are available in several logic families that have increased drive capability. Such components can supply about three times the output current, when compared with the normal drive-capability logic circuits mentioned above.

'1004: A special group of driver circuits was introduced into the ALS and AS family for applications requiring a very large output current. These components play a significant role in clock distribution systems.

'240: The output characteristics of these bus interface circuits are of particular importance when a decision must be made as to which circuit family should be used for a specific system requirement. The available output current has a decisive influence on the distortion of signals on bus lines.

'25240: The incident-wave-switching (IWS) driver was developed to meet the requirements imposed by fast bus systems and applications with exceptionally low-resistance lines. Since these components play a significant role in applications of this kind, their input and output characteristics have been included.

Table 1 provides an overall view of the input and output characteristics curves shown on the following pages.

Table 1. Typical Output Types in the Various Logic Families

FAMILY	TYPE				
	'00	'40	'240	'1004	'25240
SN74	✓	✓			
SN74LS	✓	✓	✓		
SN74S	✓	✓	✓		
SN74ALS	✓	✓	✓	✓	
SN74AS	✓		✓	✓	
SN74F	✓	✓	✓		
SN74HC	✓		✓		
SN74AC			✓†		
SN74BCT			✓		✓
SN74ABT			✓		
SN74LV	✓		✓		
SN74LVC			✓		
SN74ALCV			✓‡		
SN74LVT			✓		

† With the AC family, the device type is SN74AC11240.
‡ With the ALVC family, only the Widebus™ function SN74ALVC16240 is available.

Waveforms at the outputs of the integrated circuits in the above table are shown in Figures 60 through 88. For these measurements, the devices under test were loaded with a 1.3-m coaxial cable having a characteristic impedance of 50 Ω; the end of the line was open circuit. These waveforms provide good insight into the dynamic behavior of the components. In particular, the oscillograms provide information regarding drive capability with a low-resistance load, together with an indication of the line reflections that can be expected.

Acknowledgment

The author of this document is Peter Forstner.

Input Characteristics

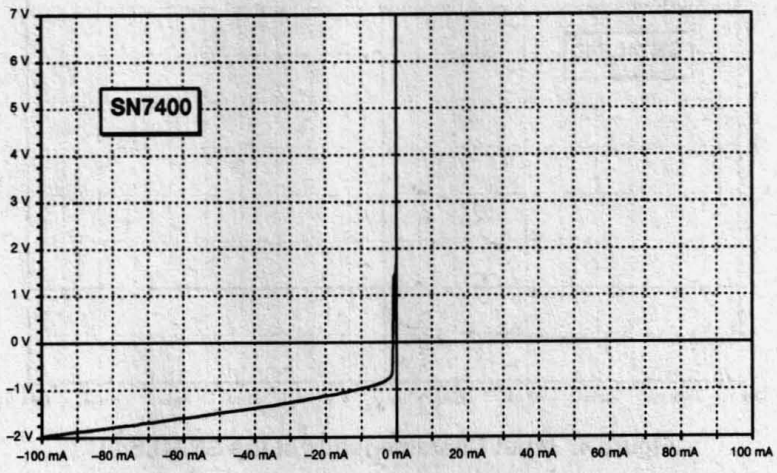


Figure 1. Input Characteristics of the SN7400

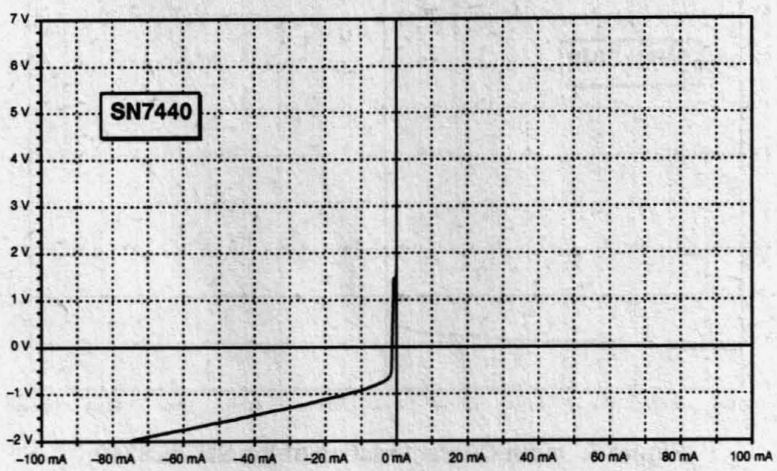


Figure 2. Input Characteristics of the SN7440

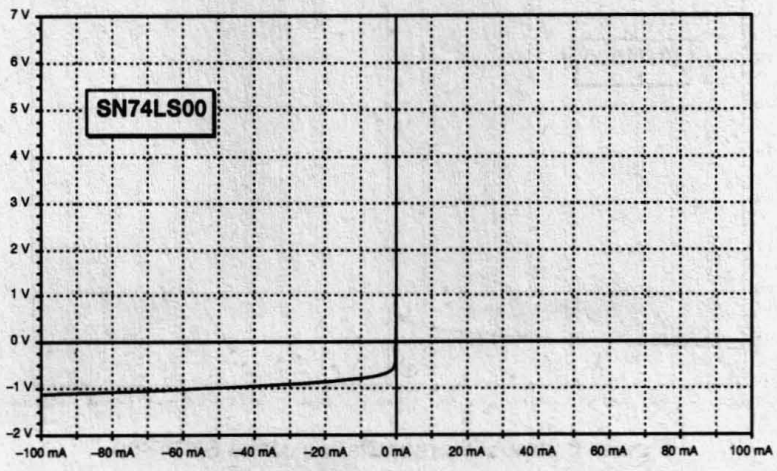


Figure 3. Input Characteristics of the SN74LS00

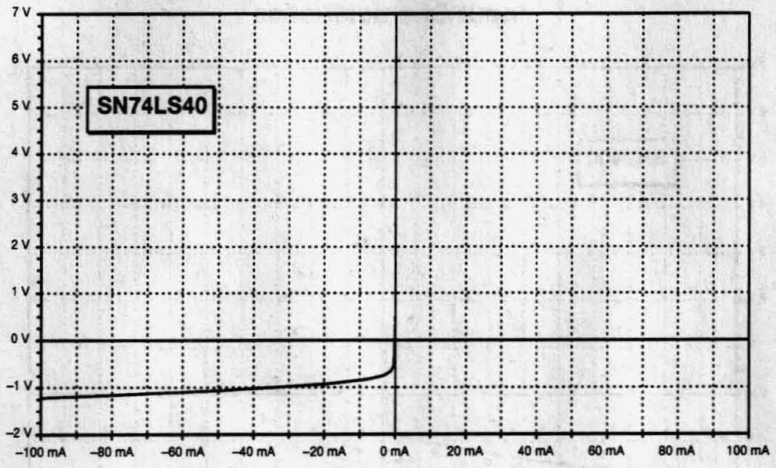


Figure 4. Input Characteristics of the SN74LS40

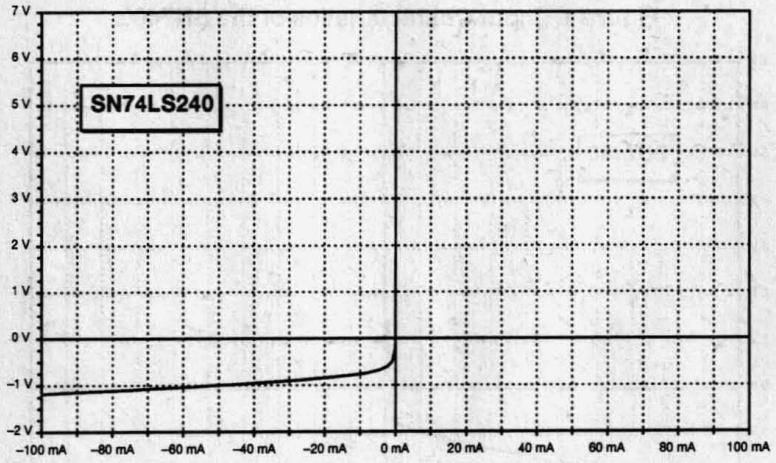


Figure 5. Input Characteristics of the SN74LS240

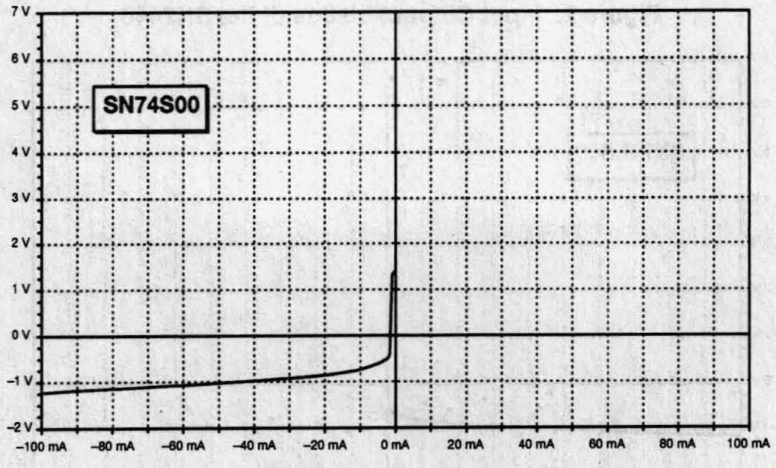


Figure 6. Input Characteristics of the SN74S00

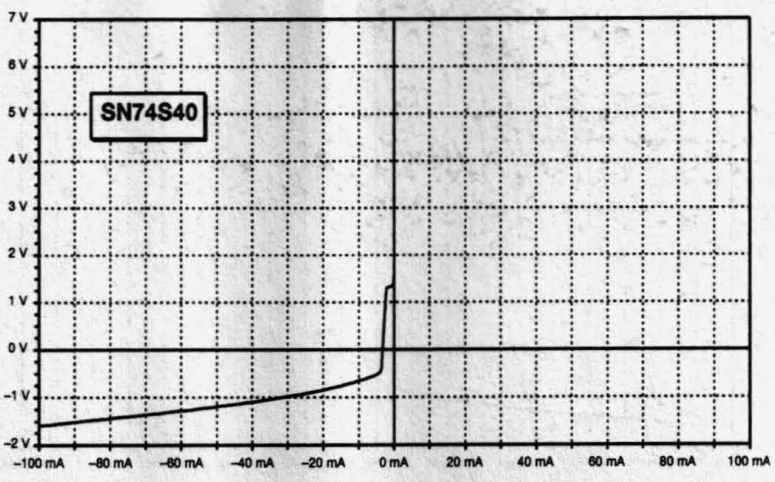


Figure 7. Input Characteristics of the SN74S40

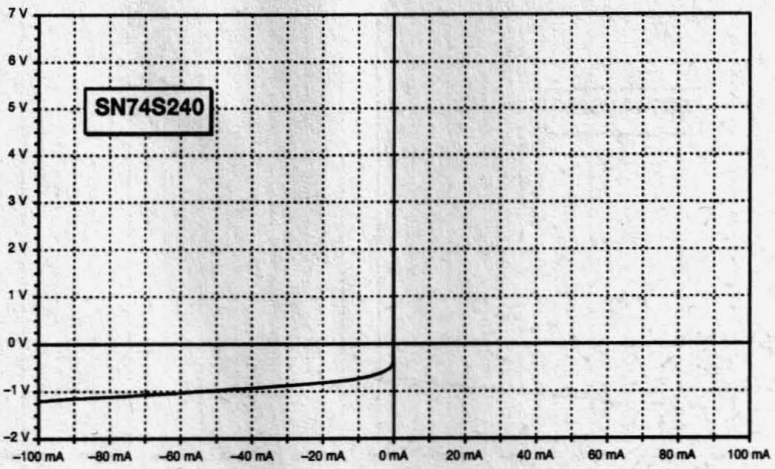


Figure 8. Input Characteristics of the SN74S240

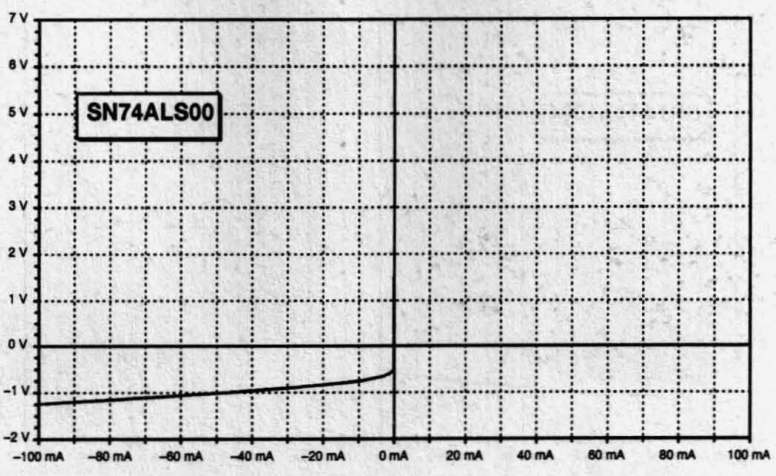


Figure 9. Input Characteristics of the SN74ALS00

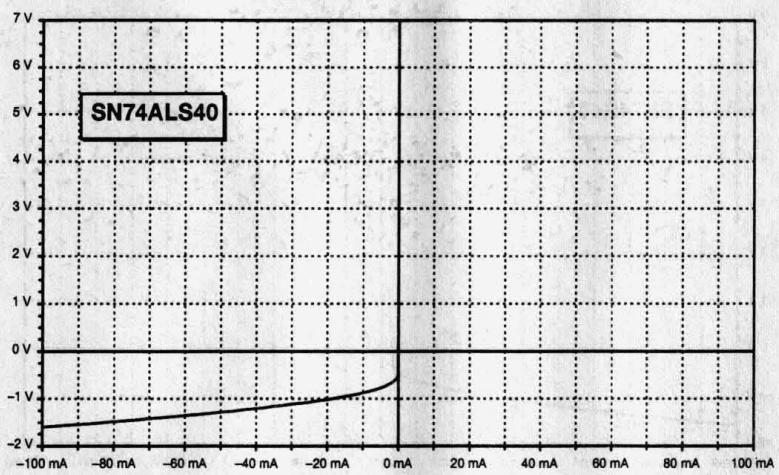


Figure 10. Input Characteristics of the SN74ALS40

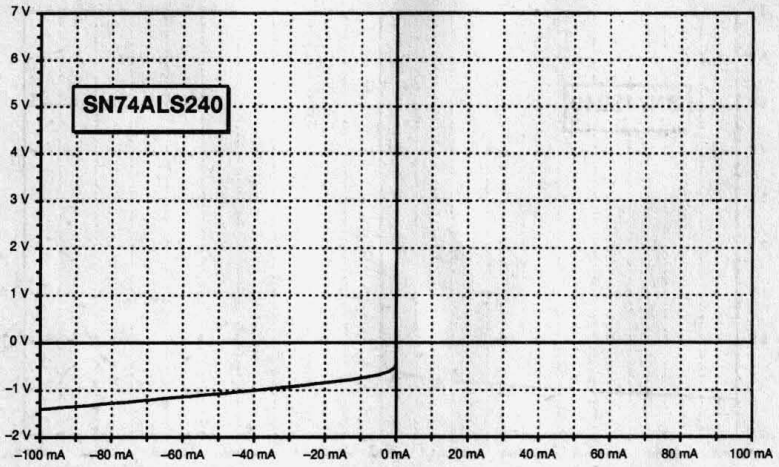


Figure 11. Input Characteristics of the SN74ALS240

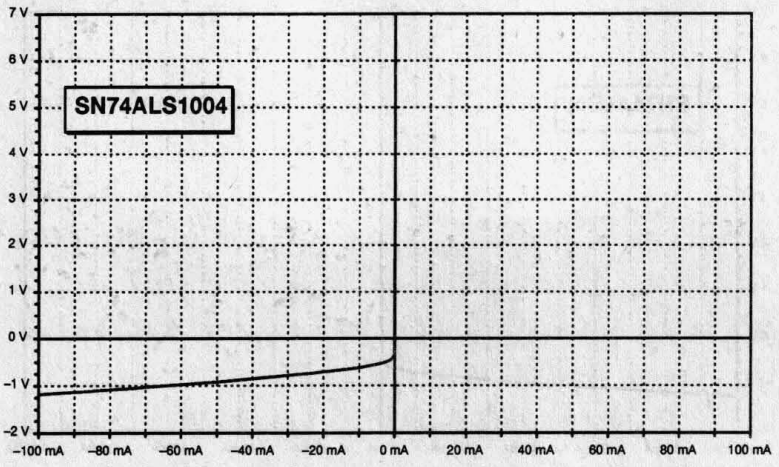


Figure 12. Input Characteristics of the SN74ALS1004

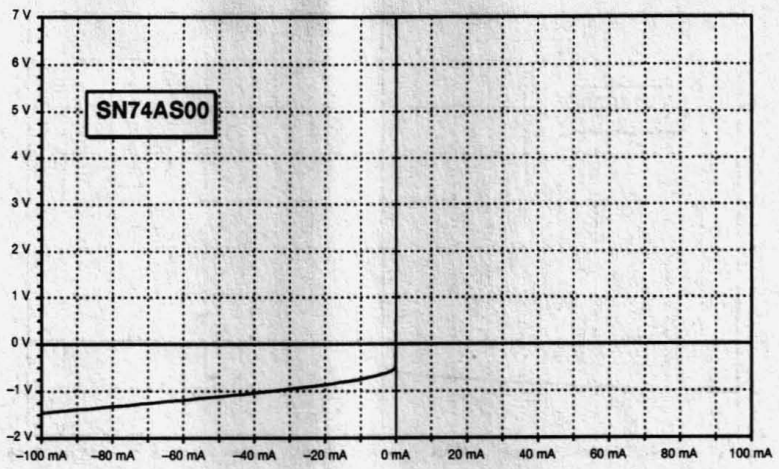


Figure 13. Input Characteristics of the SN74AS00

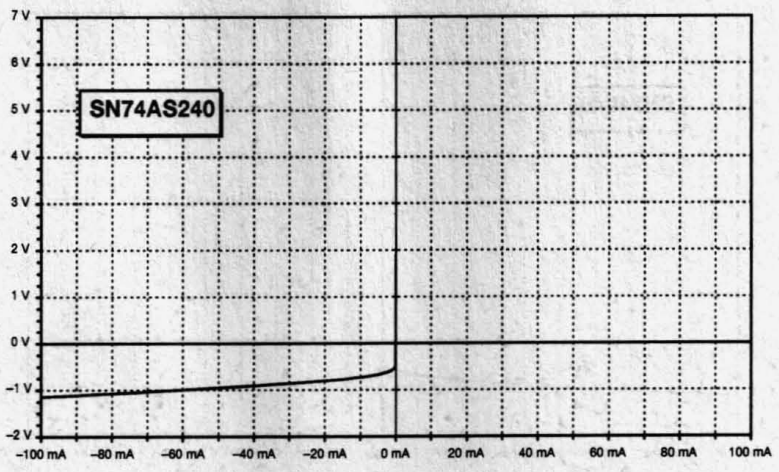


Figure 14. Input Characteristics of the SN74AS240

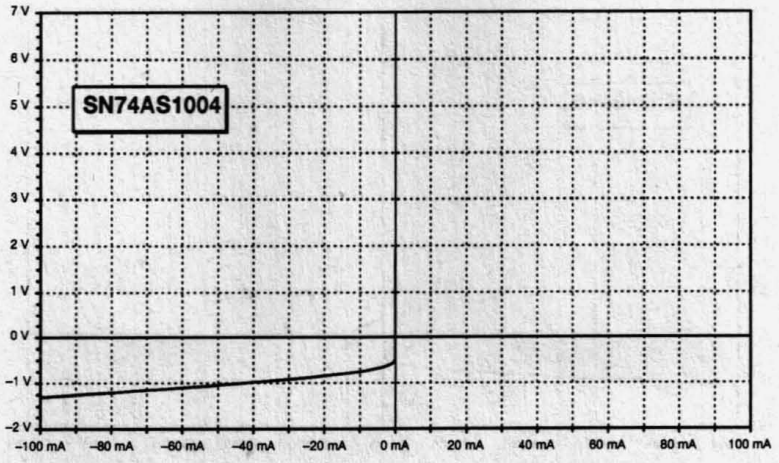


Figure 15. Input Characteristics of the SN74AS1004

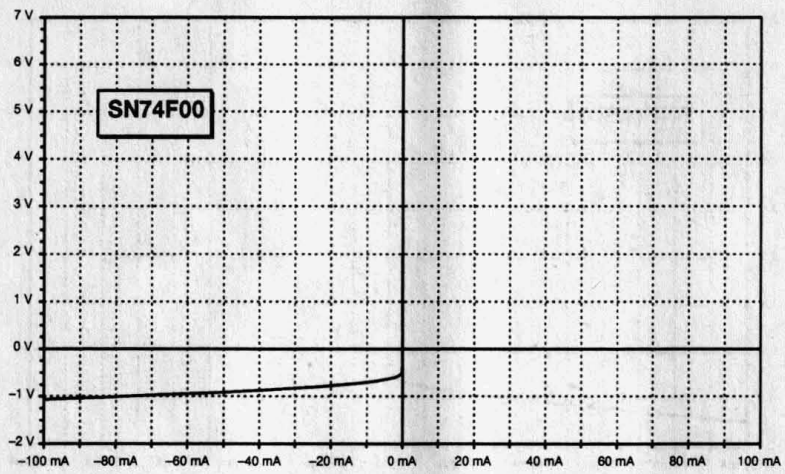


Figure 16. Input Characteristics of the SN74F00

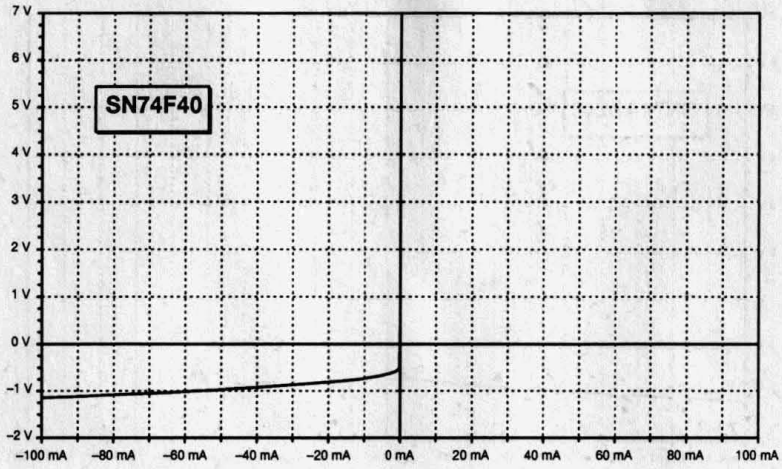


Figure 17. Input Characteristics of the SN74F40

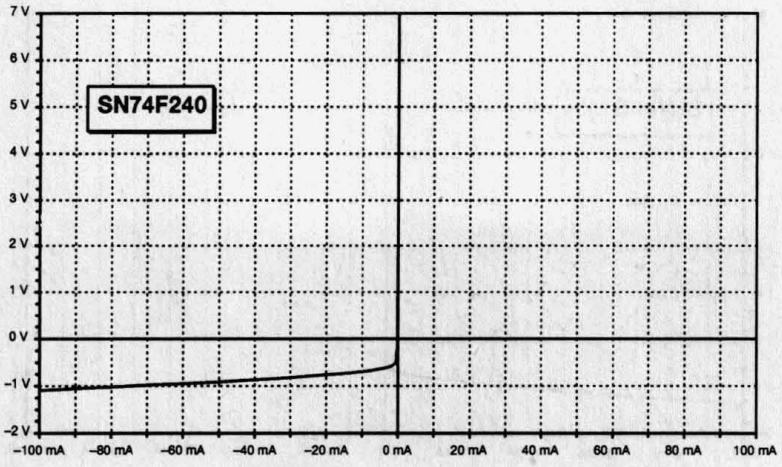


Figure 18. Input Characteristics of the SN74F240

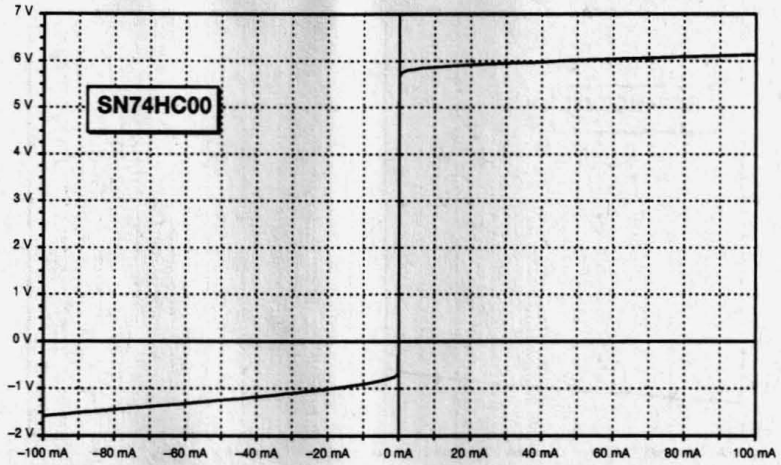


Figure 19. Input Characteristics of the SN74HC00

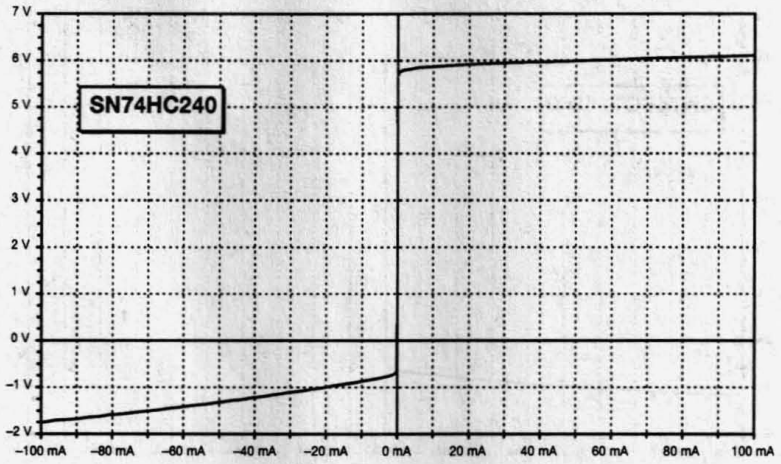


Figure 20. Input Characteristics of the SN74HC240

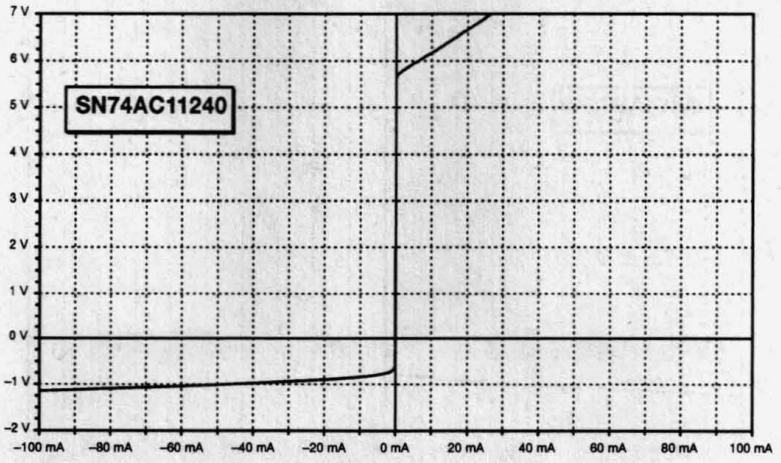


Figure 21. Input Characteristics of the SN74AC11240

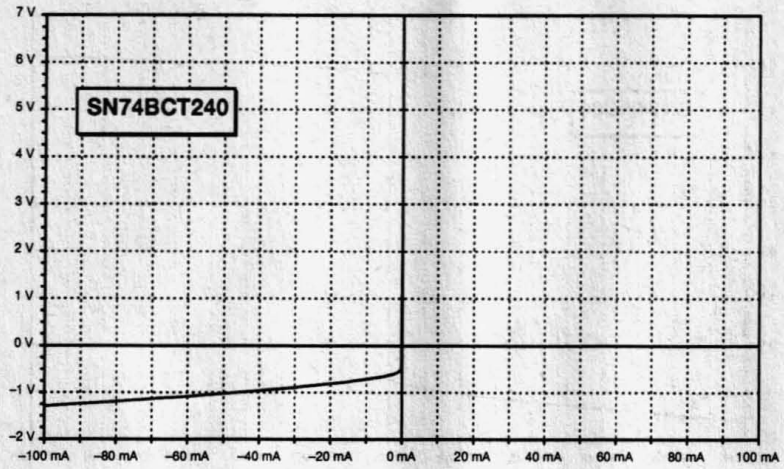


Figure 22. Input Characteristics of the SN74BCT240

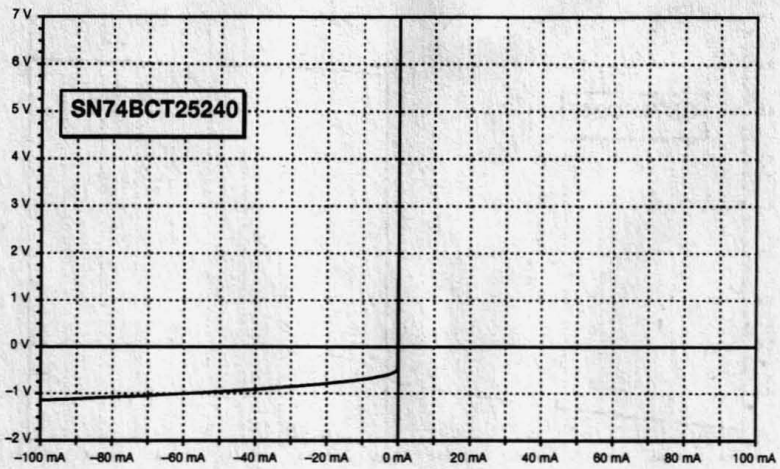


Figure 23. Input Characteristics of the SN74BCT25240

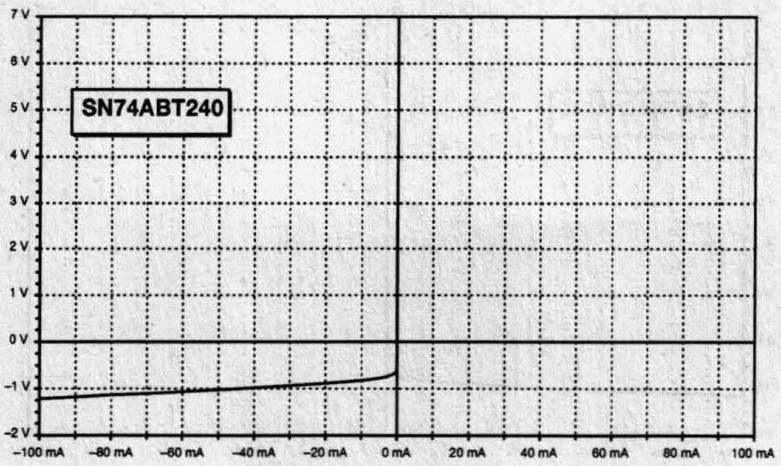


Figure 24. Input Characteristics of the SN74ABT240

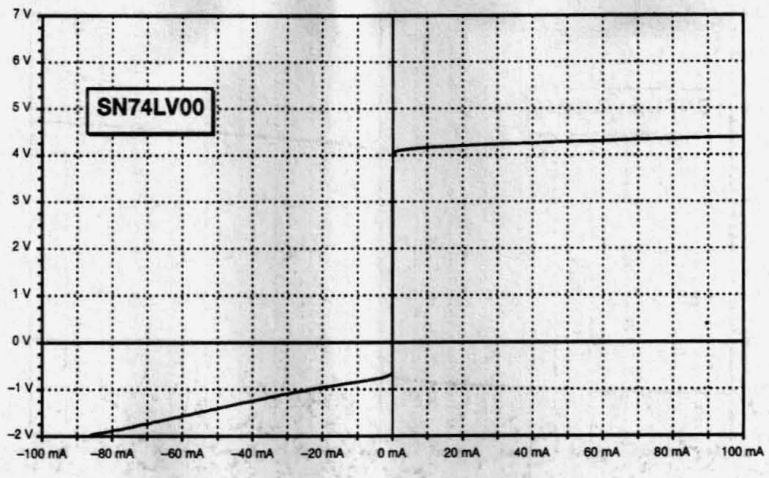


Figure 25. Input Characteristics of the SN74LV00

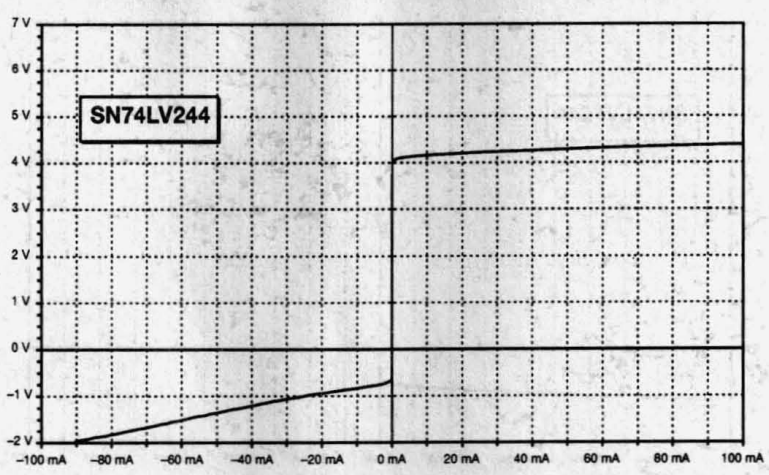


Figure 26. Input Characteristics of the SN74LV244

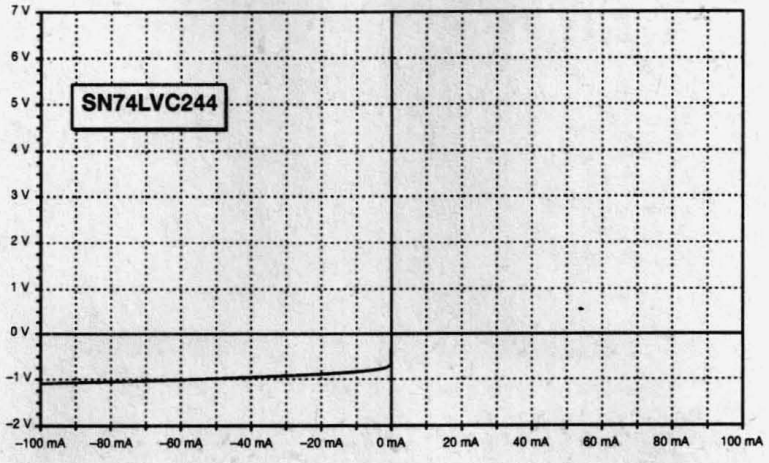


Figure 27. Input Characteristics of the SN74LVC244

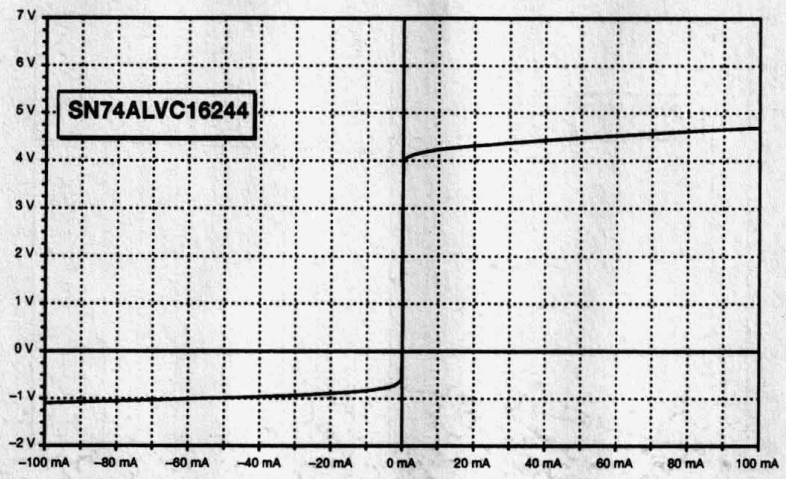


Figure 28. Input Characteristics of the SN74ALVC16244

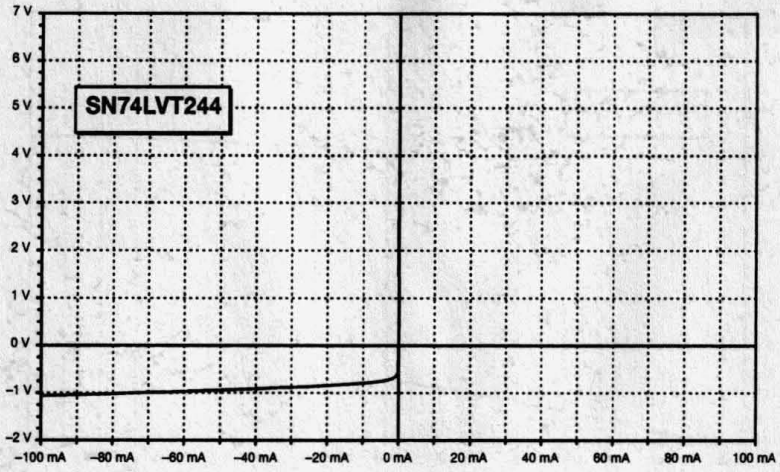


Figure 29. Input Characteristics of the SN74LVT244

Output Characteristics

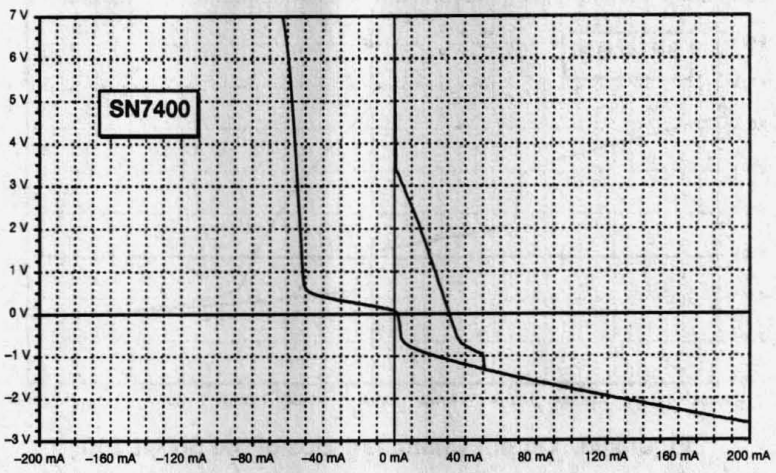


Figure 30. Output Characteristics of the SN7400

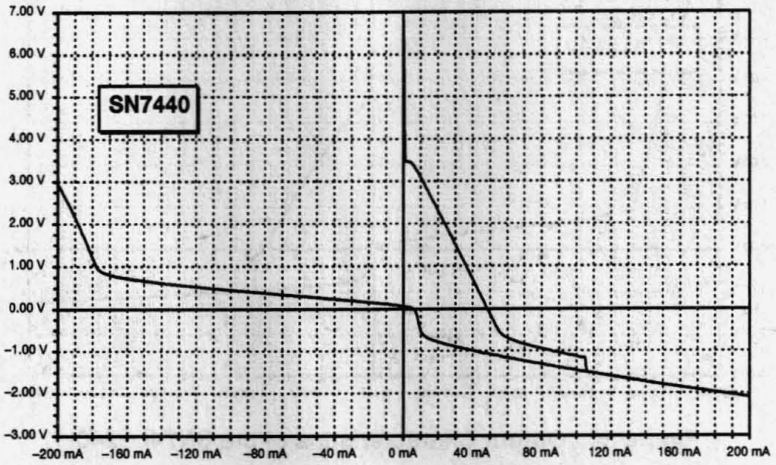


Figure 31. Output Characteristics of the SN7440

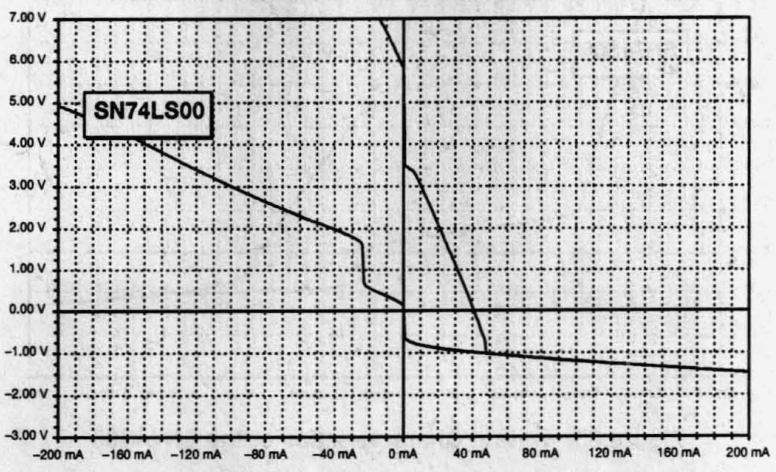


Figure 32. Output Characteristics of the SN74LS00

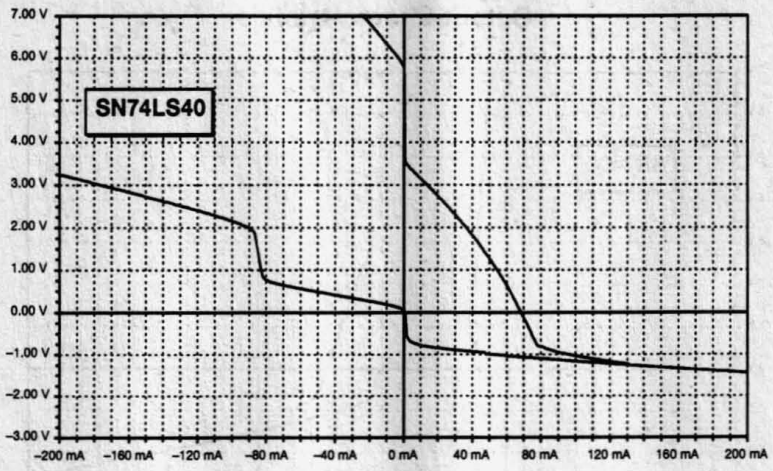


Figure 33. Output Characteristics of the SN74LS40

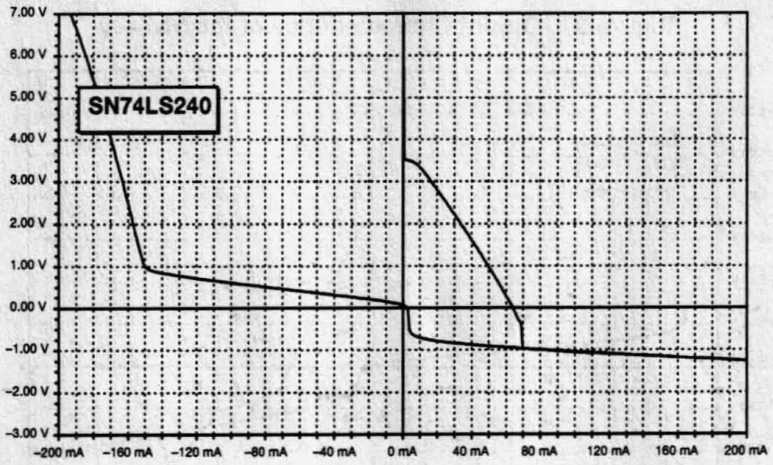


Figure 34. Output Characteristics of the SN74LS240

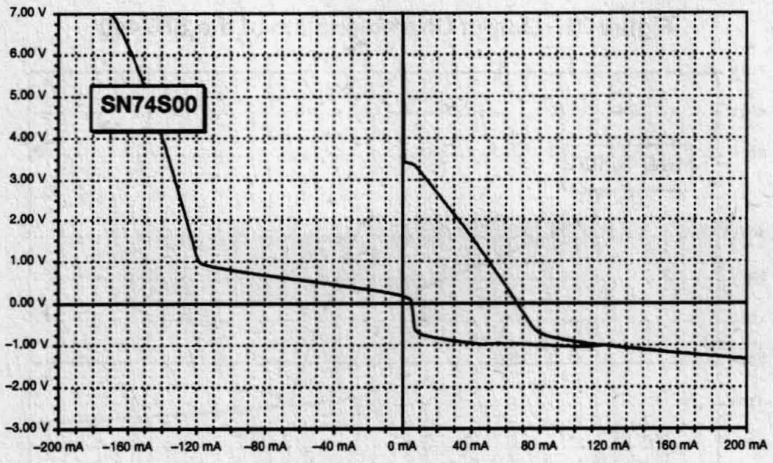


Figure 35. Output Characteristics of the SN74S00

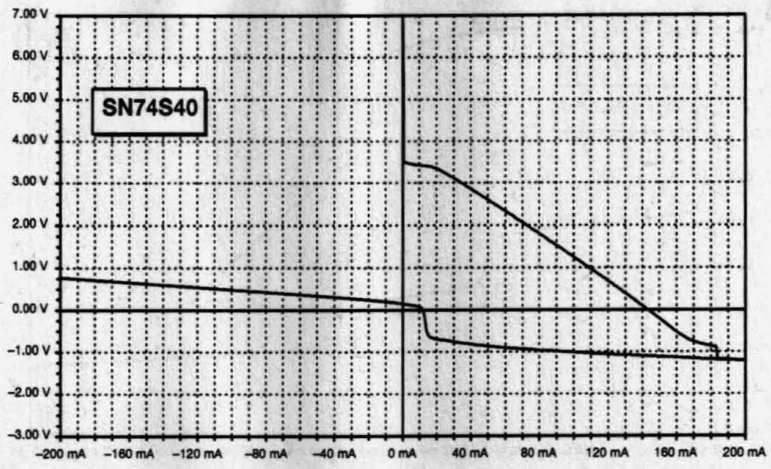


Figure 36. Output Characteristics of the SN74S40

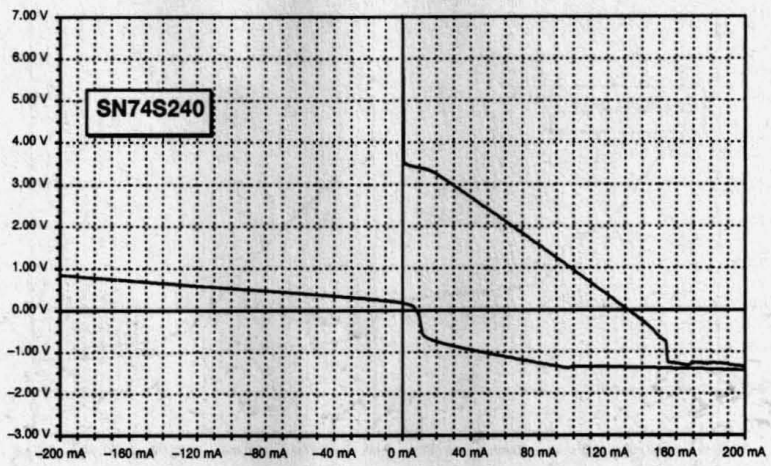


Figure 37. Output Characteristics of the SN74S240

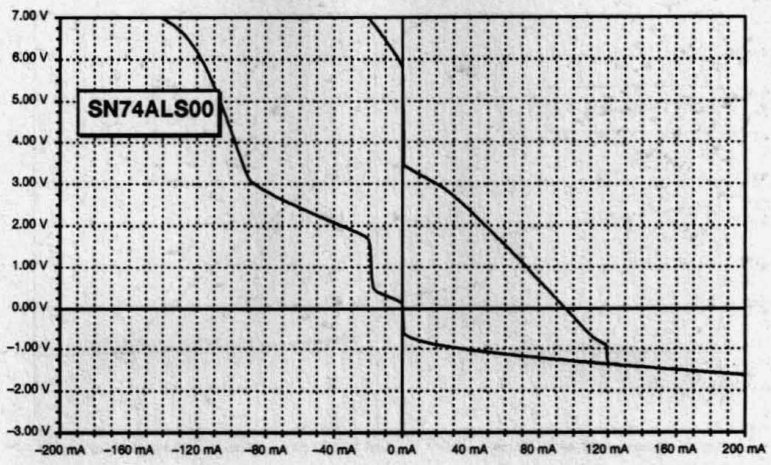


Figure 38. Output Characteristics of the SN74ALS00

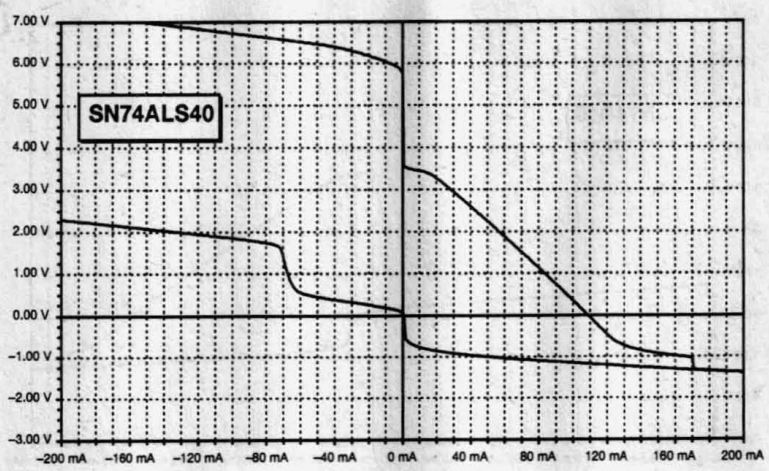


Figure 39. Output Characteristics of the SN74ALS40

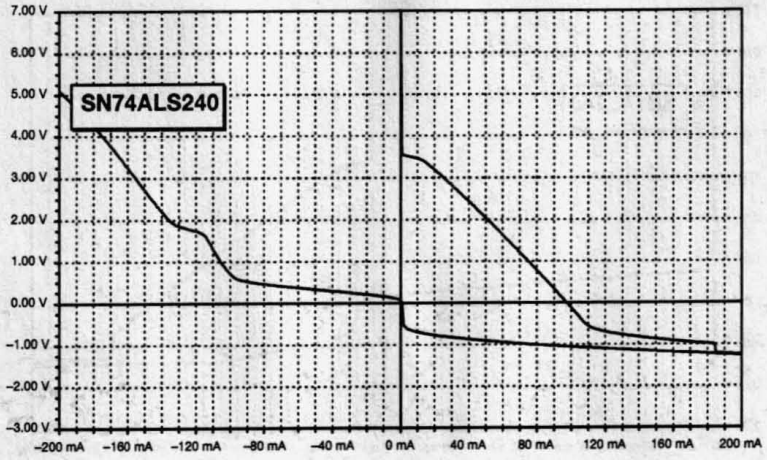


Figure 40. Output Characteristics of the SN74ALS240

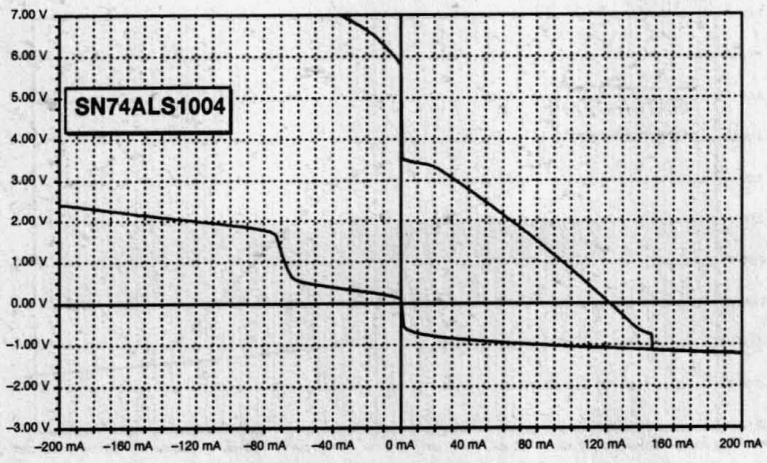


Figure 41. Output Characteristics of the SN74ALS1004

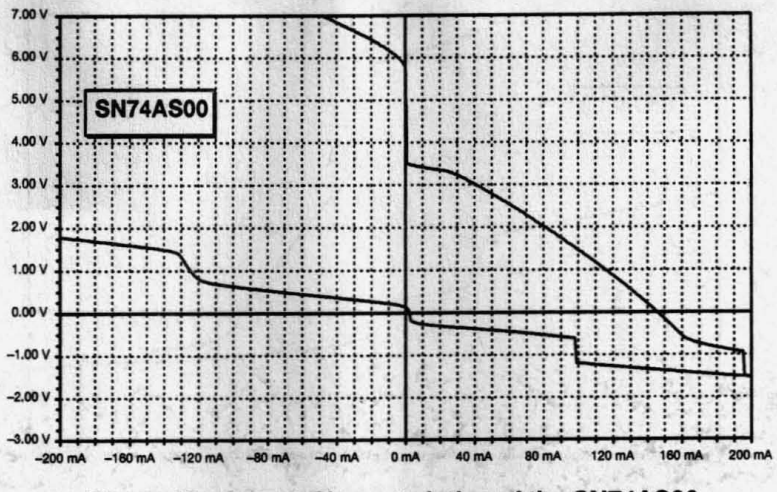


Figure 42. Output Characteristics of the SN74AS00

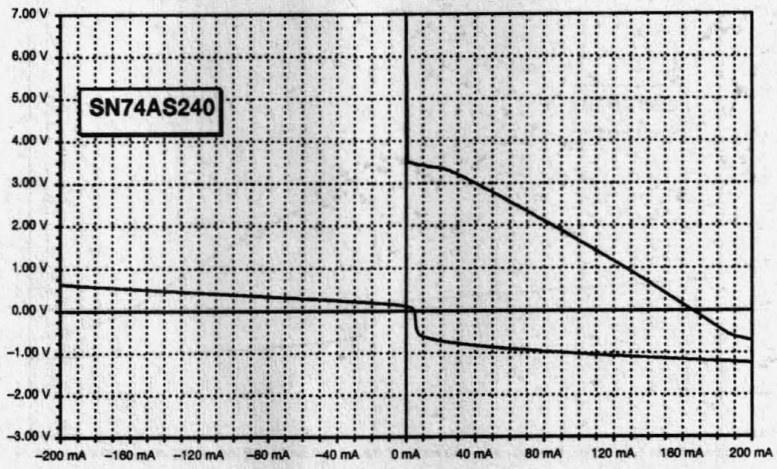


Figure 43. Output Characteristics of the SN74AS240

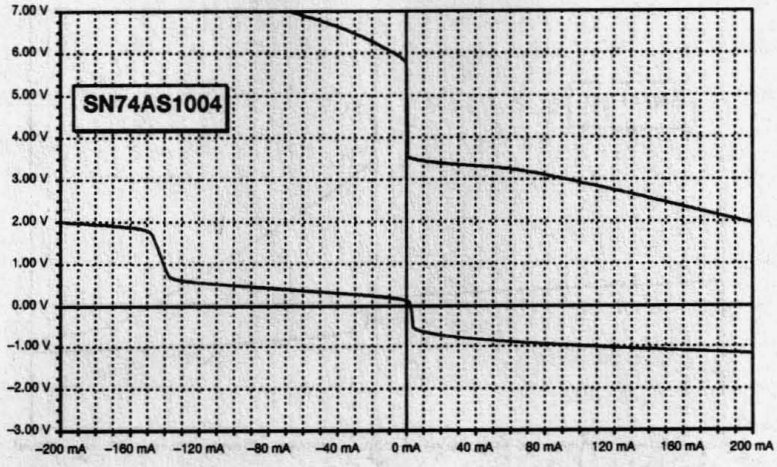


Figure 44. Output Characteristics of the SN74AS1004

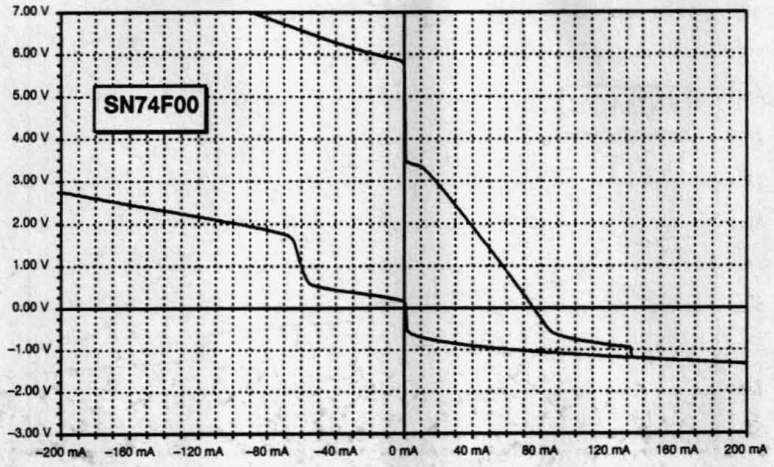


Figure 45. Output Characteristics of the SN74F00

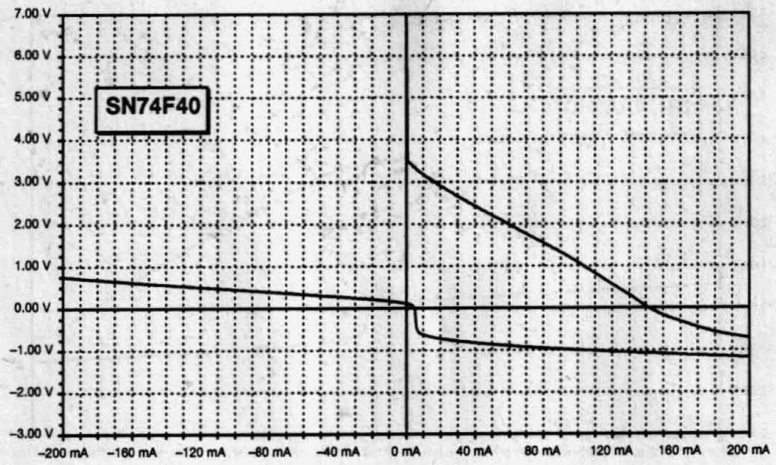


Figure 46. Output Characteristics of the SN74F40

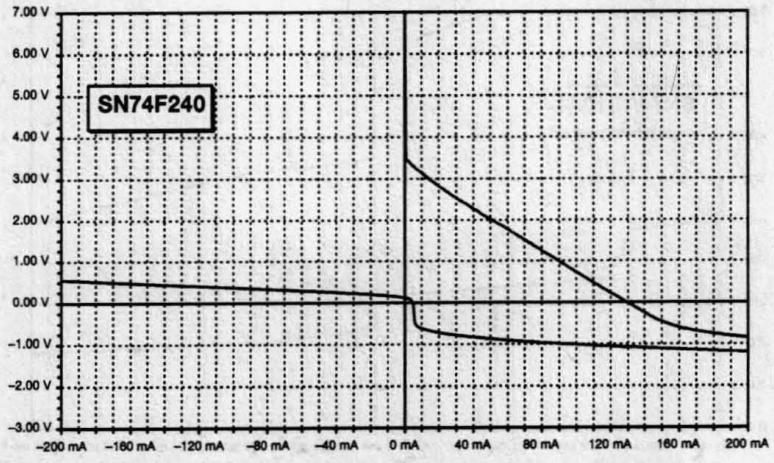


Figure 47. Output Characteristics of the SN74F240

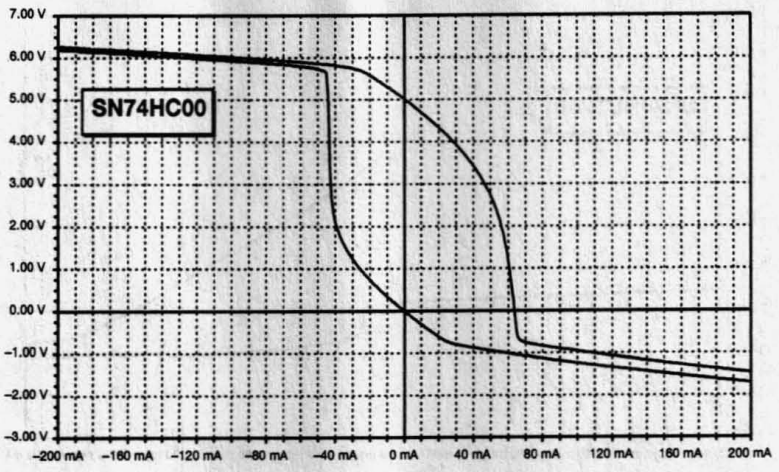


Figure 48. Output Characteristics of the SN74HC00

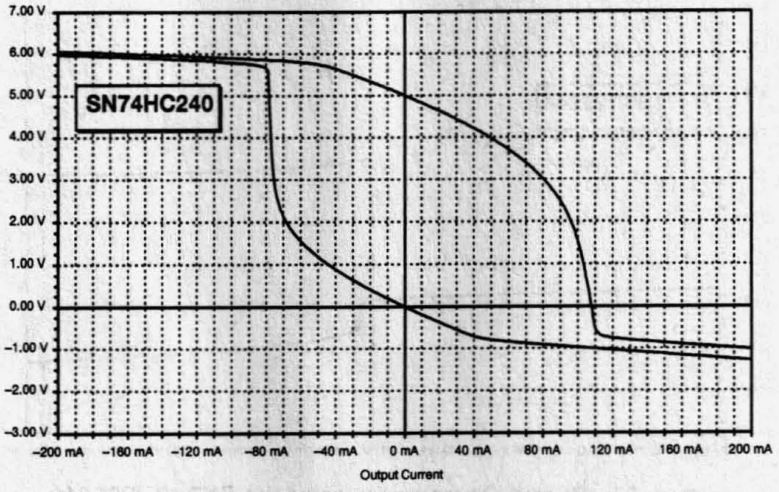


Figure 49. Output Characteristics of the SN74HC240

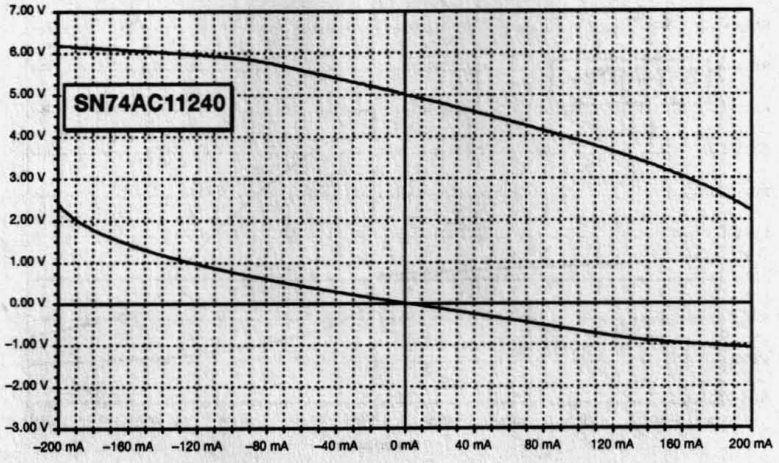


Figure 50. Output Characteristics of the SN74AC11240

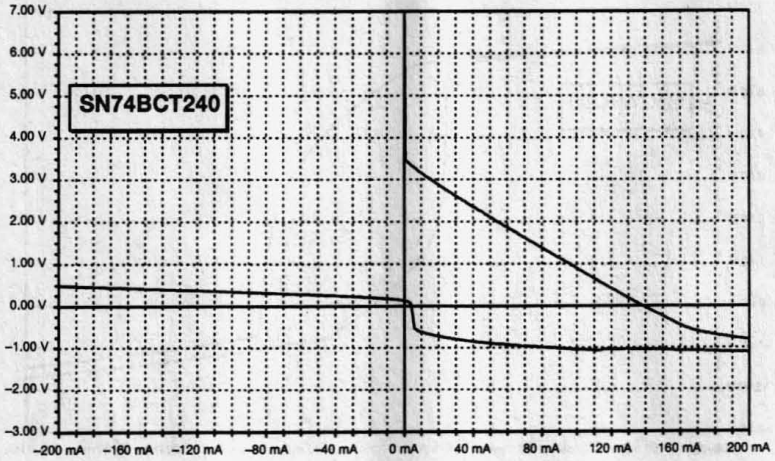


Figure 51. Output Characteristics of the SN74BCT240

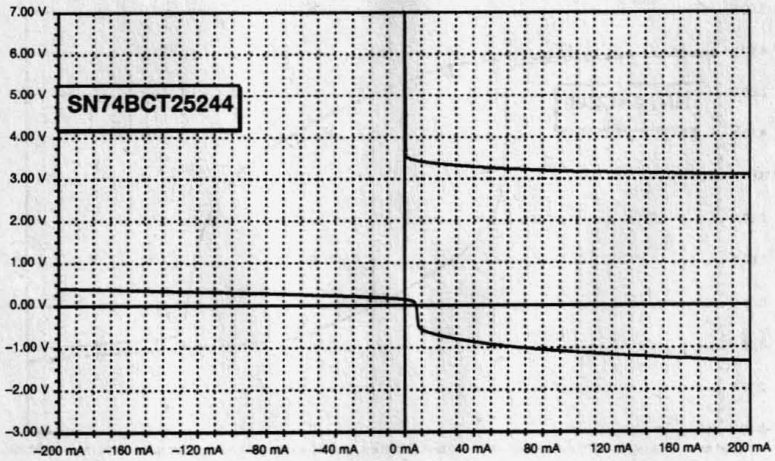


Figure 52. Output Characteristics of the SN74BCT25240

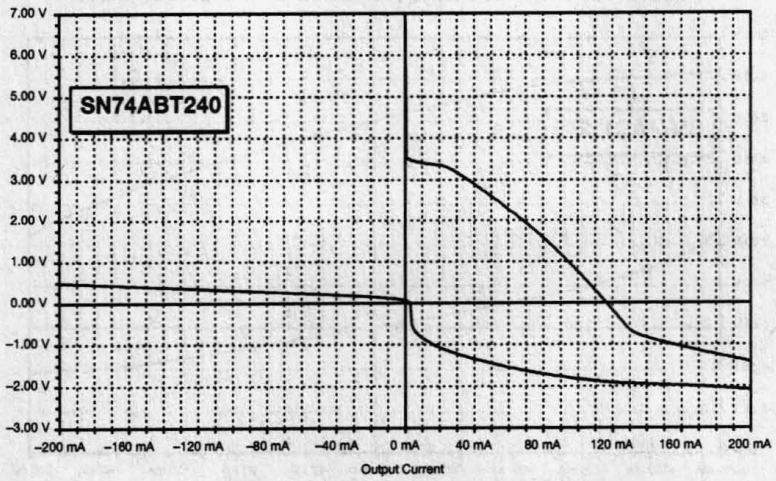


Figure 53. Output Characteristics of the SN74ABT240

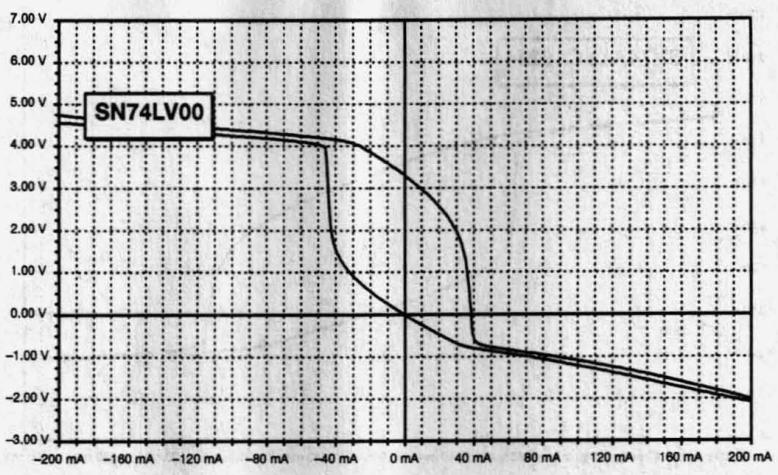


Figure 54. Output Characteristics of the SN74LV00

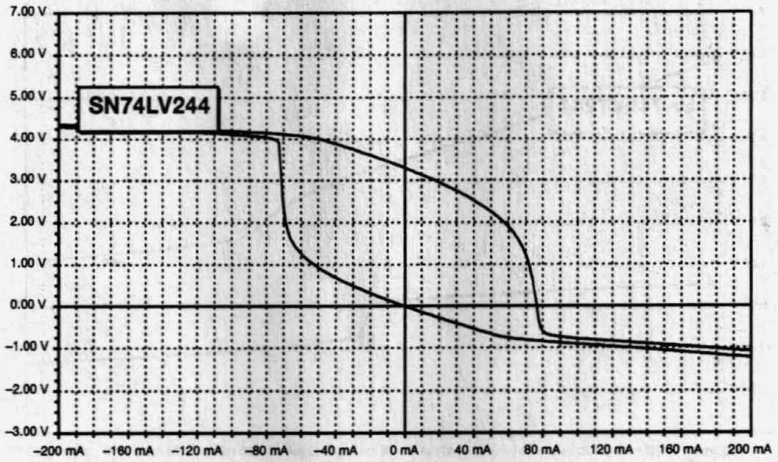


Figure 55. Output Characteristics of the SN74LV244

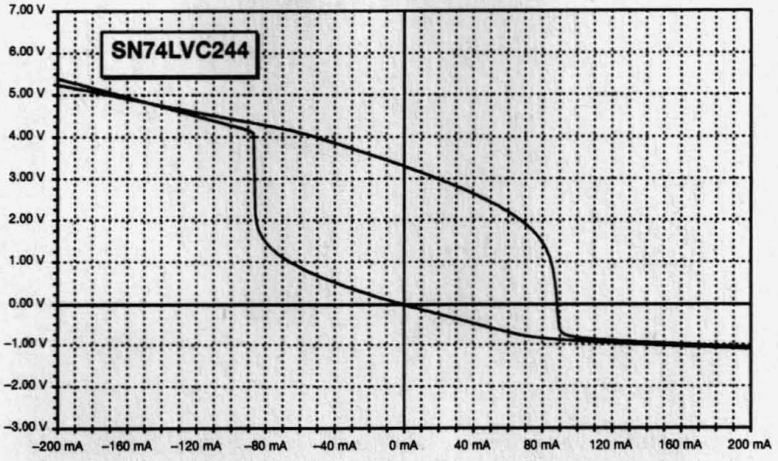


Figure 56. Output Characteristics of the SN74LVC244

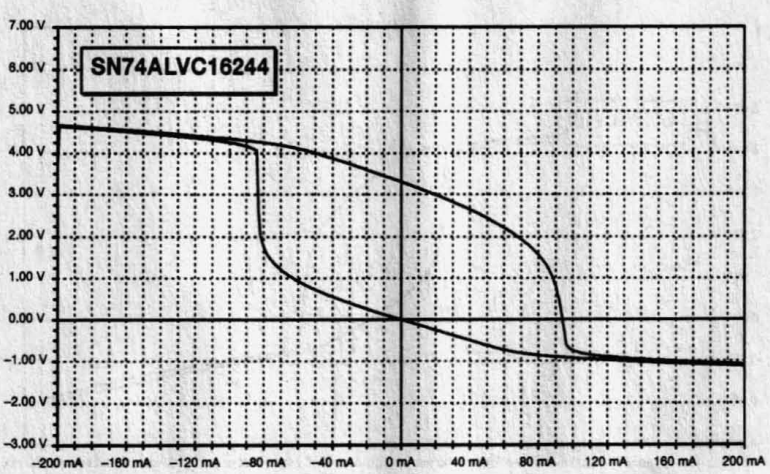


Figure 57. Output Characteristics of the SN74ALVC16244

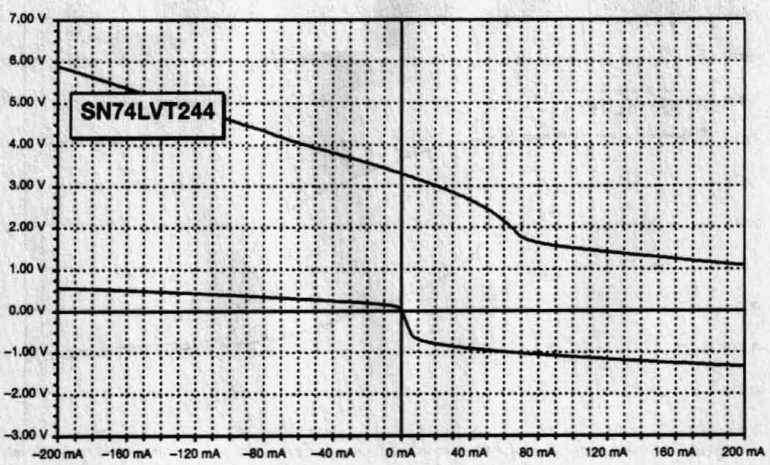


Figure 58. Output Characteristics of the SN74LVT244

Output Waveforms

The setup shown in Figure 59 was used to obtain voltage waveforms of typically representative output stages (see Figures 60 through 88).

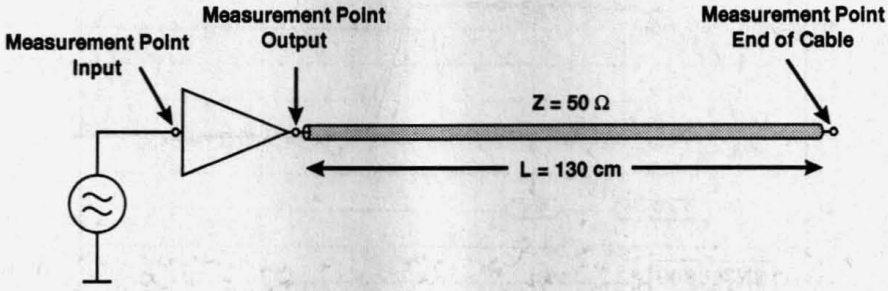


Figure 59. Setup for Obtaining Output Waveforms

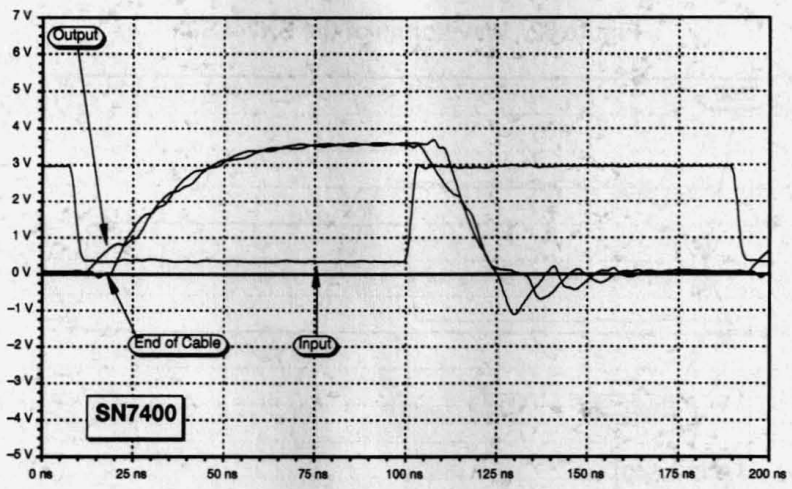


Figure 60. Waveforms of the SN7400

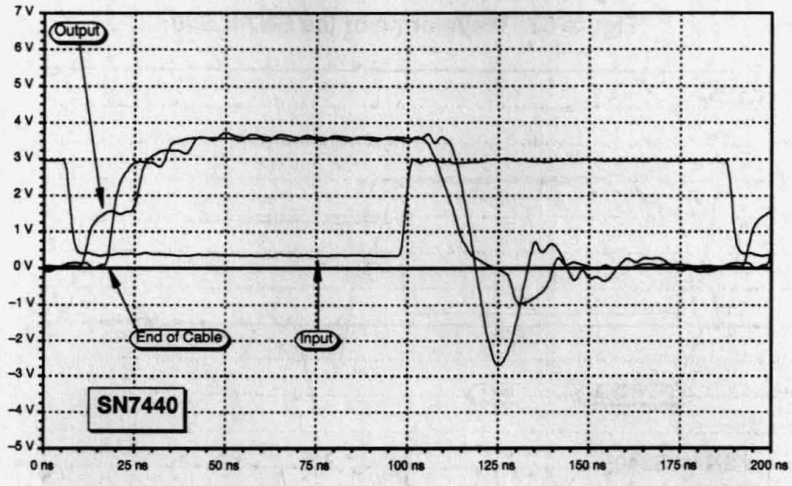


Figure 61. Waveforms of the SN7440

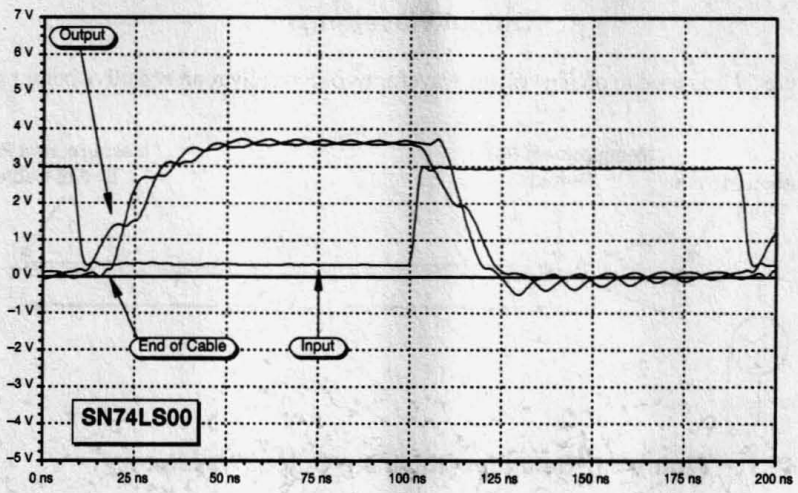


Figure 62. Waveforms of the SN74LS00

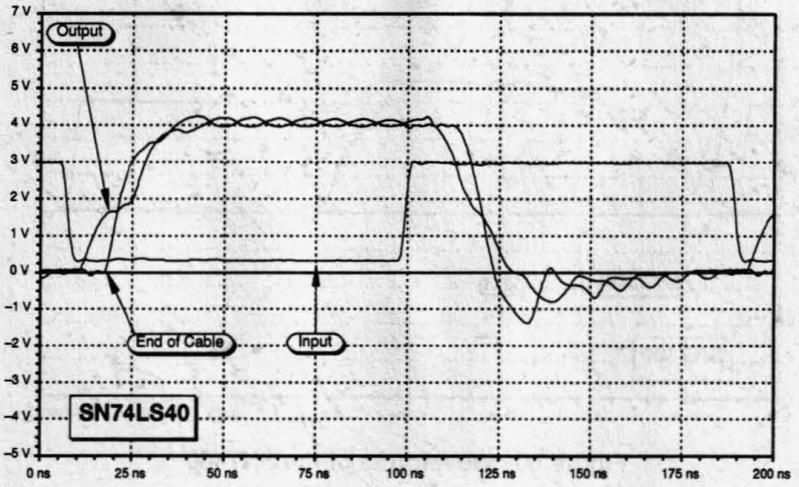


Figure 63. Waveforms of the SN74LS40

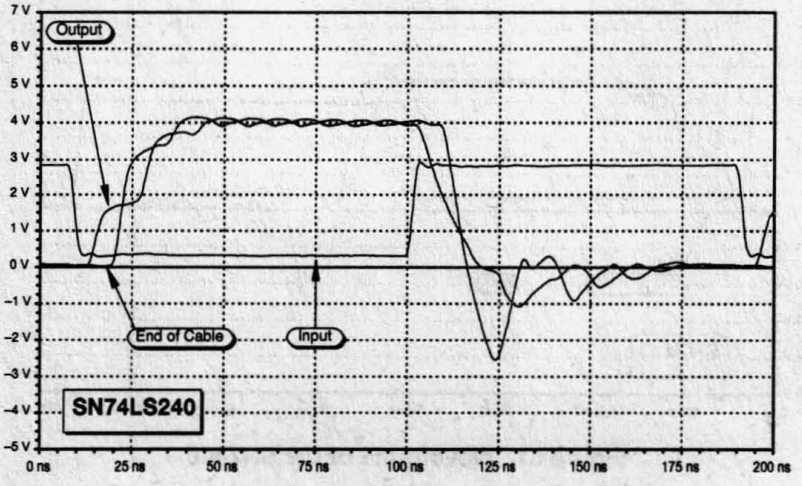


Figure 64. Waveforms of the SN74LS240

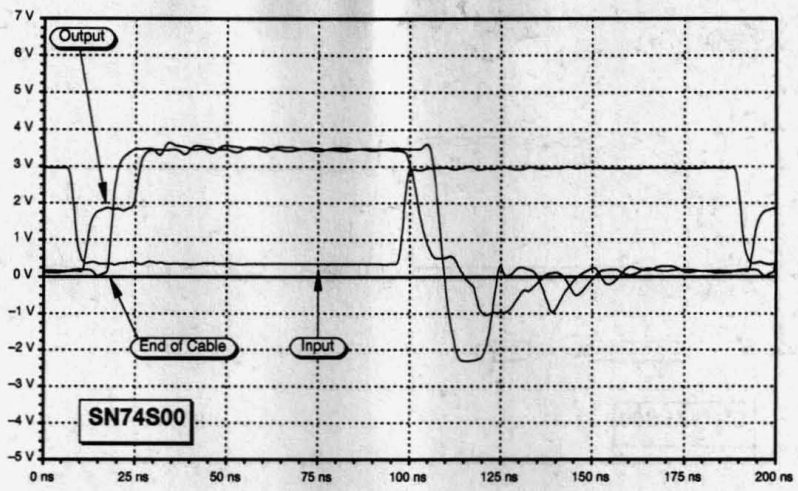


Figure 65. Waveforms of the SN74S00

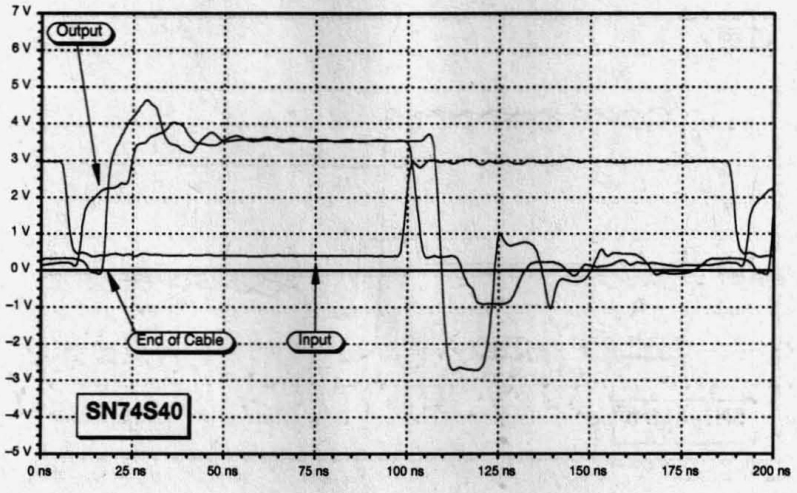


Figure 66. Waveforms of the SN74S40

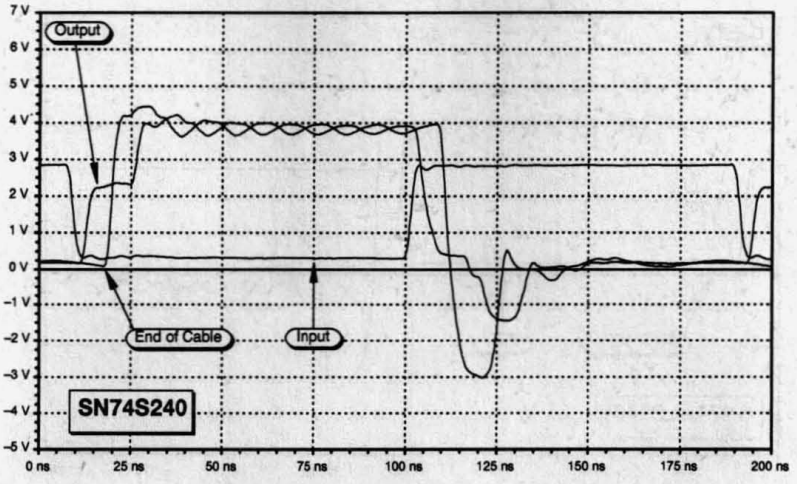


Figure 67. Waveforms of the SN74S240

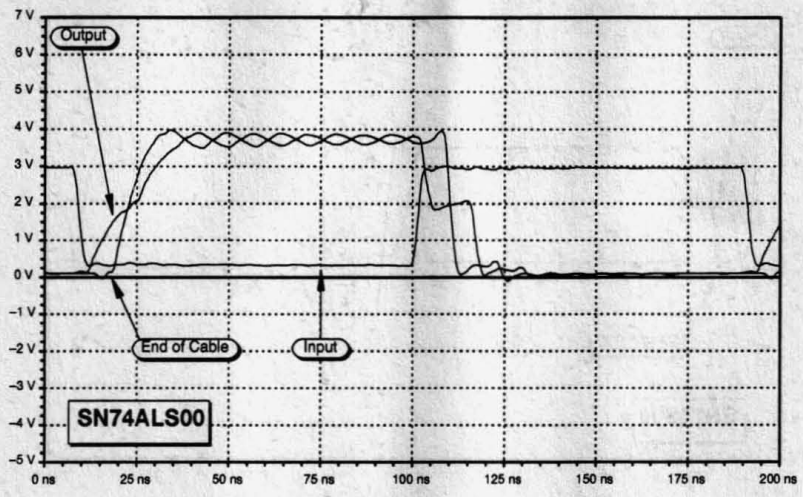


Figure 68. Waveforms of the SN74ALS00

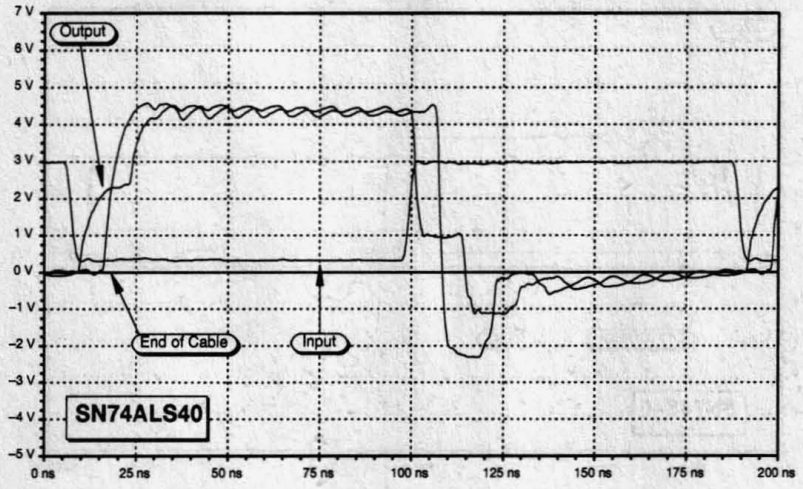


Figure 69. Waveforms of the SN74ALS40

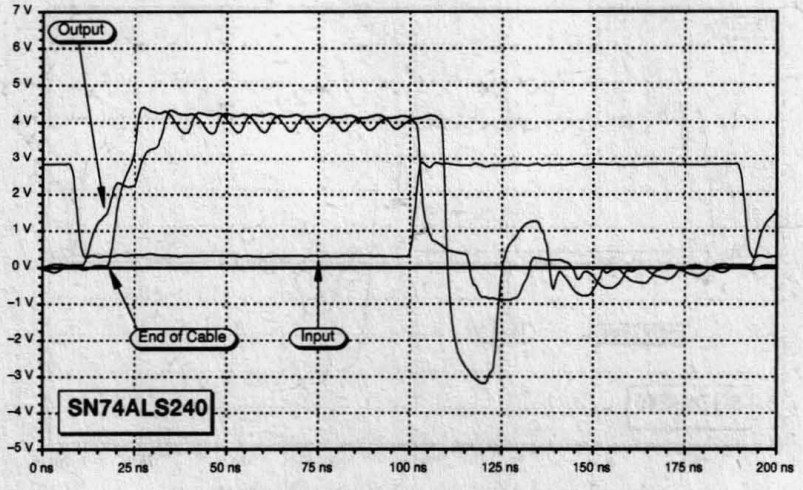


Figure 70. Waveforms of the SN74ALS240

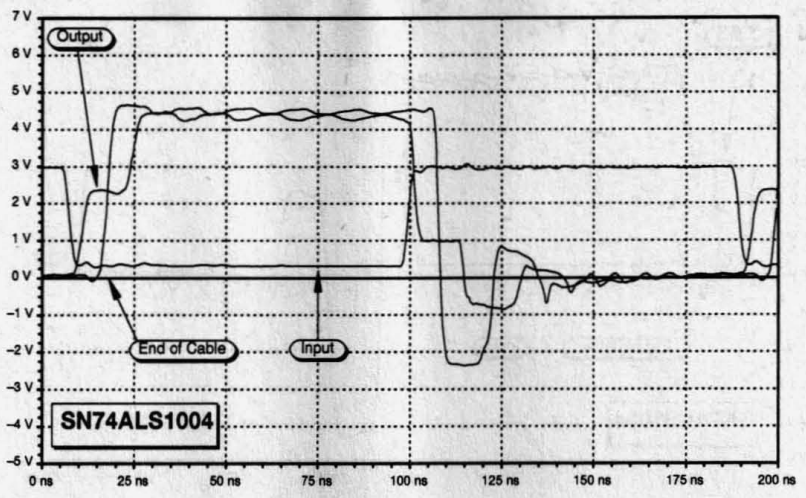


Figure 71. Waveforms of the SN74ALS1004

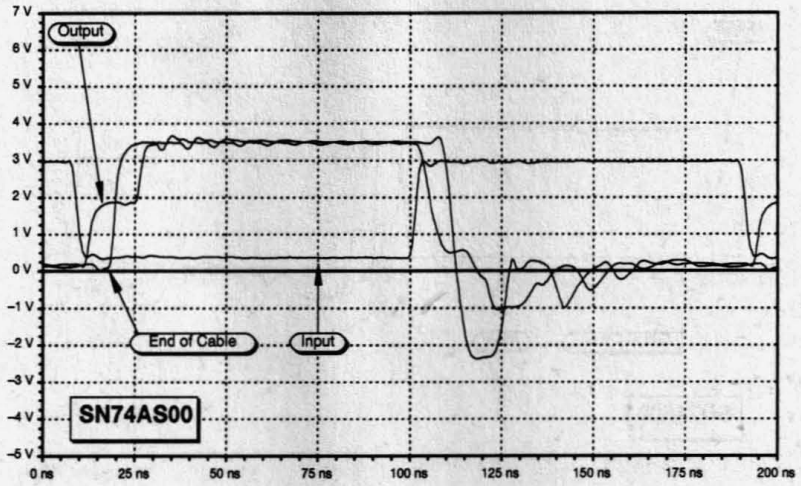


Figure 72. Waveforms of the SN74AS00

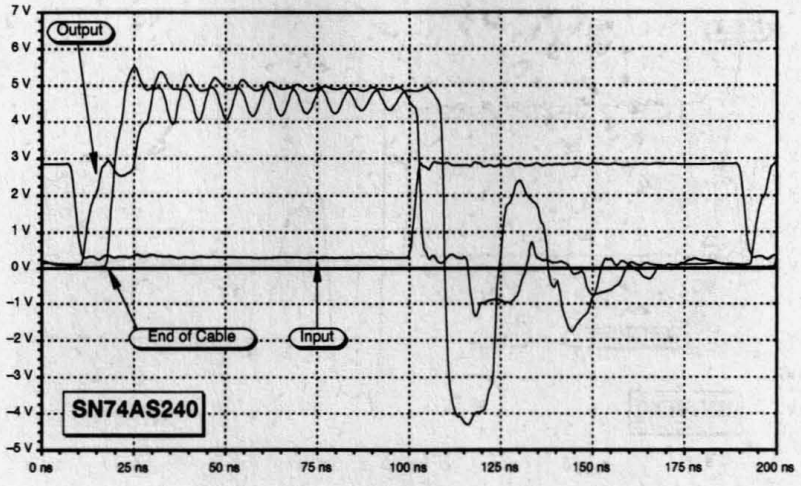


Figure 73. Waveforms of the SN74AS240

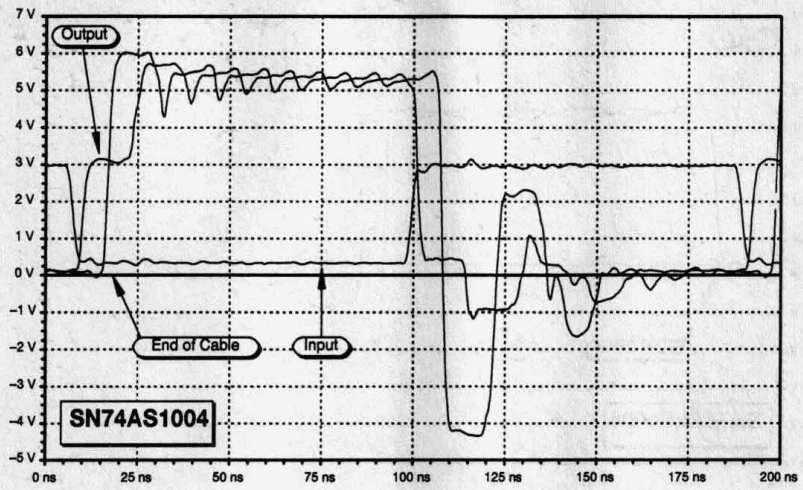


Figure 74. Waveforms of the SN74AS1004

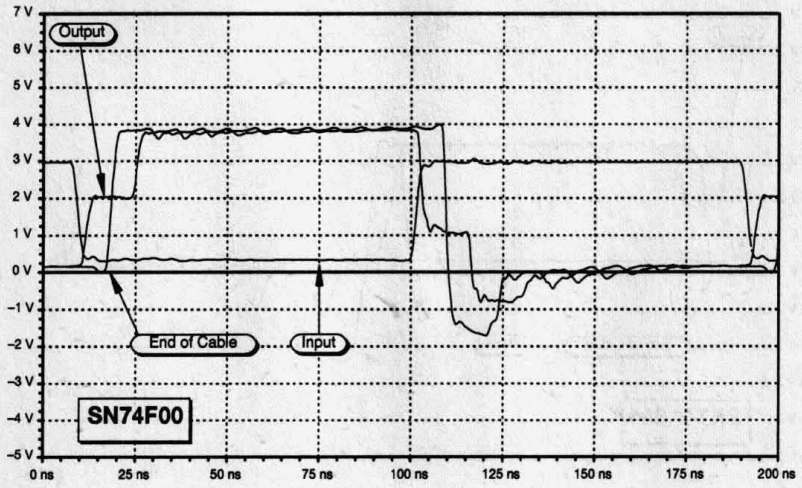


Figure 75. Waveforms of the SN74F00

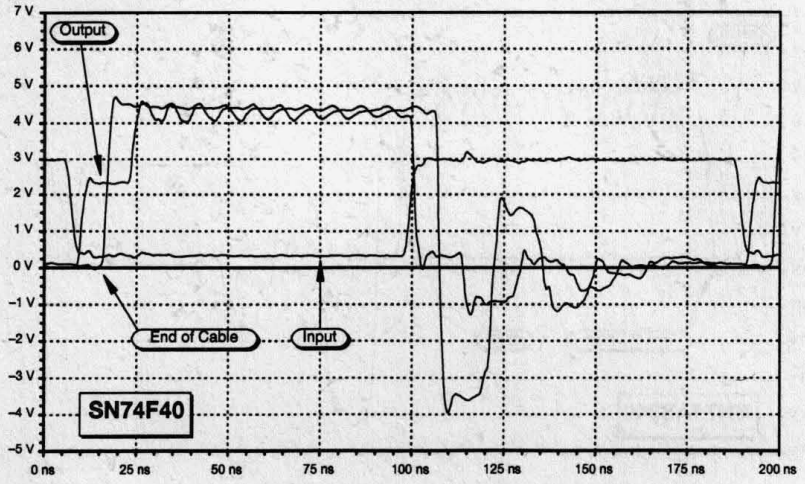


Figure 76. Waveforms of the SN74F40

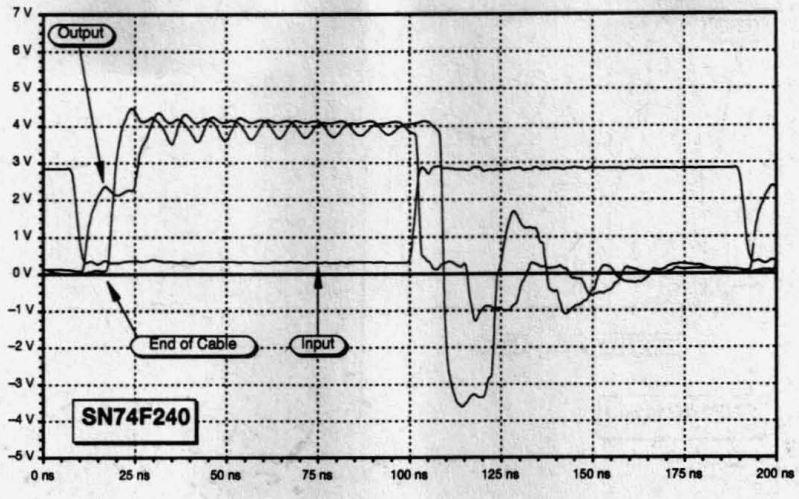


Figure 77. Waveforms of the SN74F240

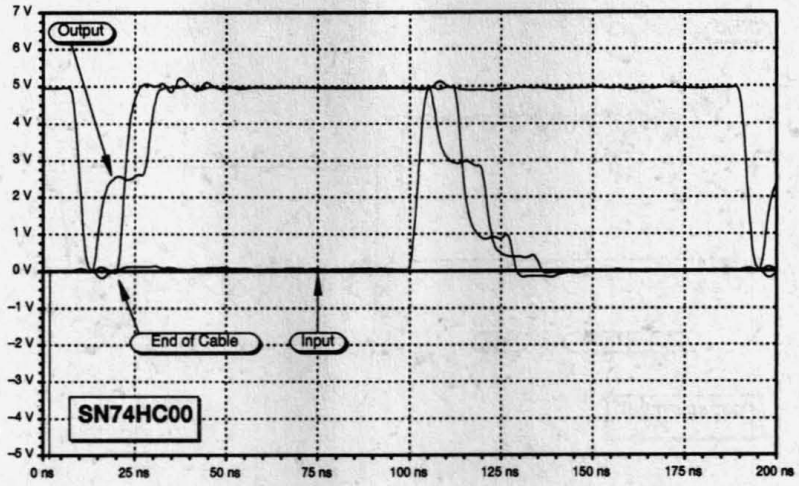


Figure 78. Waveforms of the SN74HC00

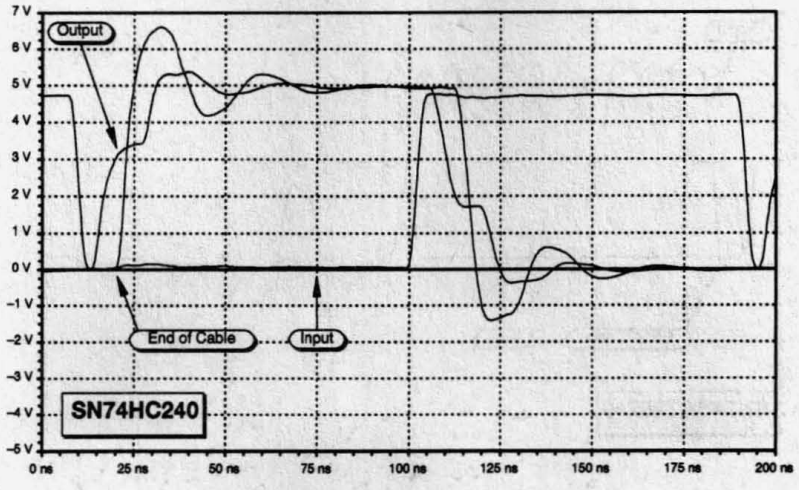


Figure 79. Waveforms of the SN74HC240

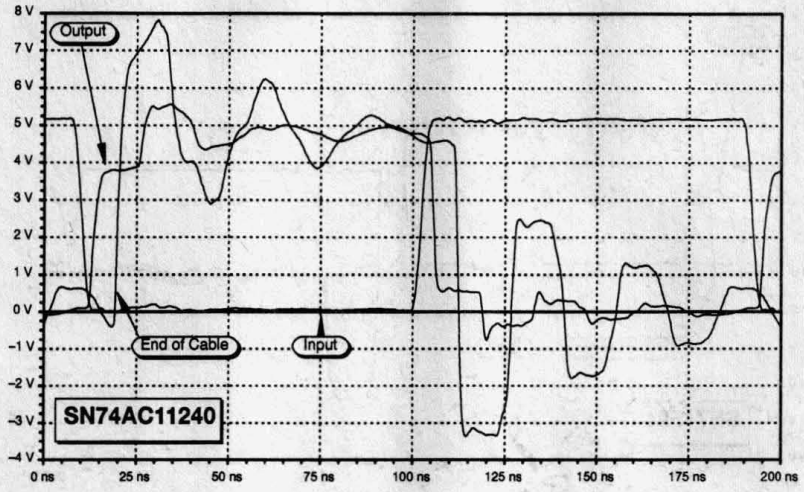


Figure 80. Waveforms of the SN74AC11240

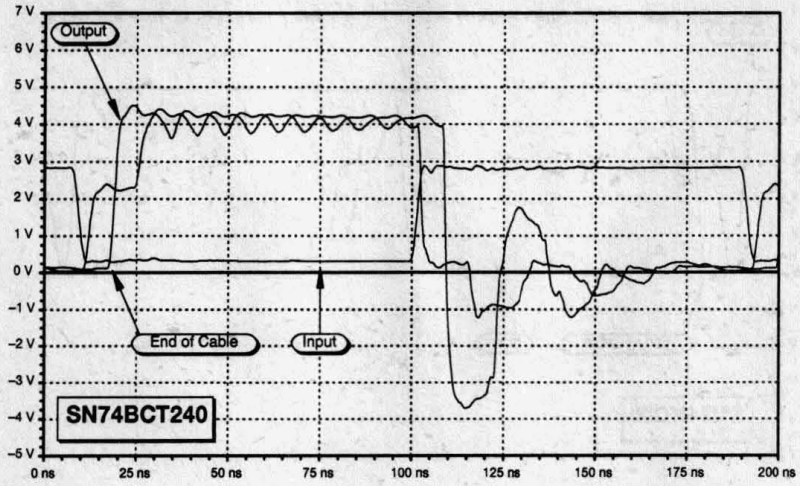


Figure 81. Waveforms of the SN74BCT240

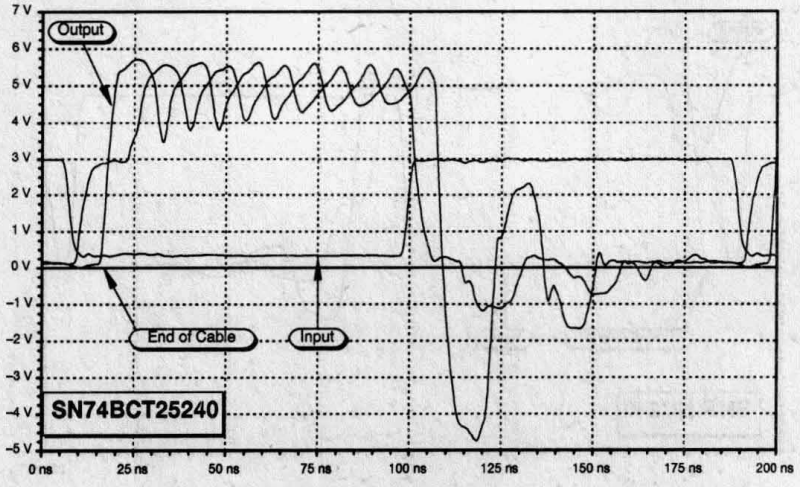


Figure 82. Waveforms of the SN74BCT25240

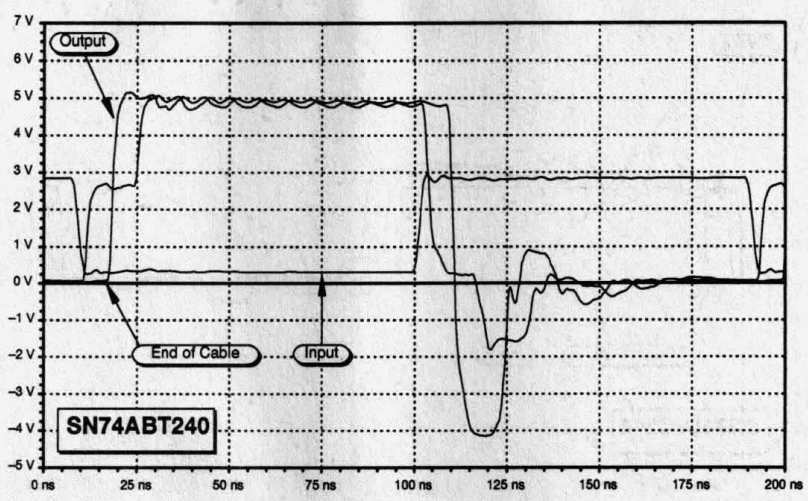


Figure 83. Waveforms of the SN74ABT240

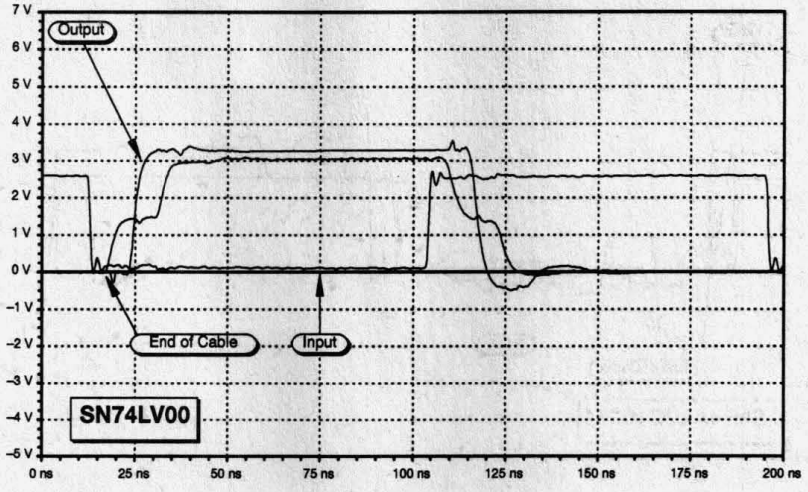


Figure 84. Waveforms of the SN74LV00

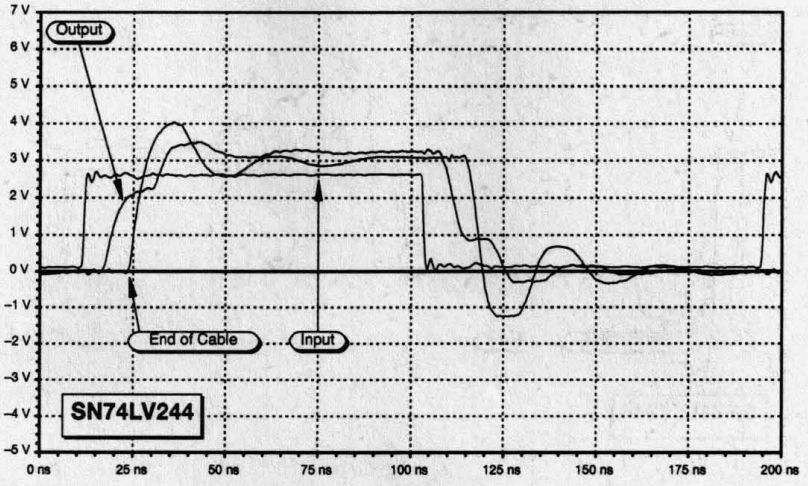


Figure 85. Waveforms of the SN74LV244

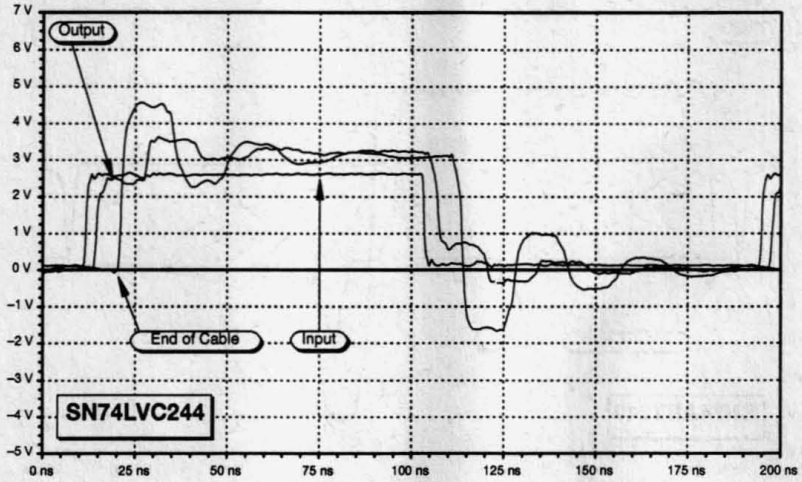


Figure 86. Waveforms of the SN74LVC244

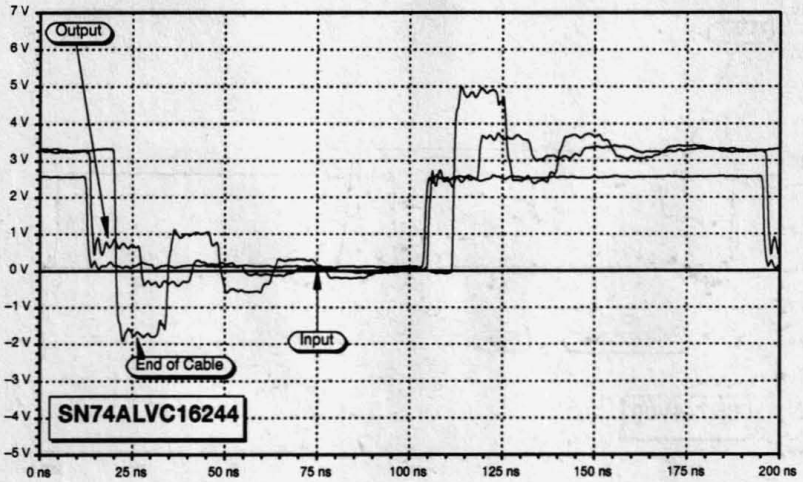


Figure 87. Waveforms of the SN74ALVC16244

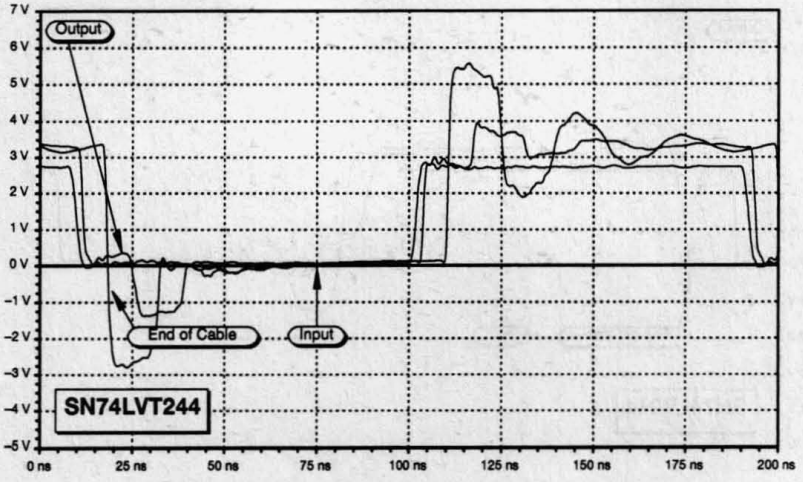


Figure 88. Waveforms of the SN74LVT244

Metastable Response in 5-V Logic Circuits

SDYA006
February 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Abstract	**3–75**
1 Introduction	**3–75**
2 Definition of Metastable State	**3–75**
3 Description of Test Circuit	**3–77**
4 Test Results	**3–79**
5 Circuitry Measures	**3–82**
6 Integrated Synchronization Circuits	**3–85**
7 Summary	**3–86**
8 Acknowledgment	**3–86**

List of Illustrations

Figure	*Title*	*Page*
1	Bipolar Master-Slave D-Type Flip-Flop	3–75
2	Timing Conditions of a D-Type Flip-Flop	3–76
3	Timing of Metastable States	3–76
4	Different Output Signals in the Metastable State	3–77
5	Test Circuit for Examining the Metastable State	3–78
6	Oscillogram of Clock and Data Signal on Flip-Flop FF2	3–78
7	Timing of Test Signals	3–79
8	Metastable Characteristic of Logic Circuits	3–80
9	Interrupt Synchronization	3–82
10	Two-Stage Synchronization Circuit	3–83
11	Timing Conditions of READY Signal in TMS320C25	3–84
12	Synchronization of READY Input	3–85
13	Logic Diagram of SN74AS4374B Synchronization Circuit	3–85

Abstract

This application report describes metastable response in digital circuits. After defining the phenomenon itself, this report describes a test circuit with which the response can be analyzed and gives test results. Using examples, the influence of metastability on the response of asynchronous circuits and measures for improving reliability are assessed.

1 Introduction

Designers of digital systems are constantly confronted with the problem of synchronizing two systems that operate at different frequencies. The problem is usually resolved by synchronizing one of the signals with the local clock generator using a flip-flop. But such a solution, of necessity, leads to a violation of the operating conditions for the flip-flops as defined in the data sheets, i.e., in these cases, the setup time and hold time are not maintained. Therefore, a flip-flop can go into a metastable state, endangering the operability of the circuit and, thereby, the reliability of the whole system. The purpose of this report is, first, to acquaint designers with the phenomenon of metastability in dynamic circuits (flip-flops) and, second, to look at test results on the more common bipolar, CMOS, and BiCMOS circuit families. Using these data the designer can determine the influence of metastable states in an application and take any necessary countermeasures.

2 Definition of Metastable State

Figure 1 illustrates the internal circuitry of a master/slave D-type flip-flop. Only those parts are shown that are of interest for the purpose of this application report. If there is a low on the CLK input, the emitters of transistors Q1 and Q2 (master flip-flop) go high so that they are turned off. By way of the D input, depending on the logic level applied here, there also is high potential on one of the two bases of the transistors. A positive edge on the CLK input means that, first, gates G2 and G3 are disabled. As a result of hole-storage effects, the outputs of these gates can maintain their output voltage for a certain time. At the same time, the emitters of the transistors go low. The transistor on whose base the higher voltage appeared conducts, while the other transistor remains turned off. The flip-flop composed of the two transistors is held in this stable state by feedback resistors R1 and R2. At the same time, the slave flip-flop consisting of gates G4 and G5 is set to the new state and the new level appears on the Q outputs.

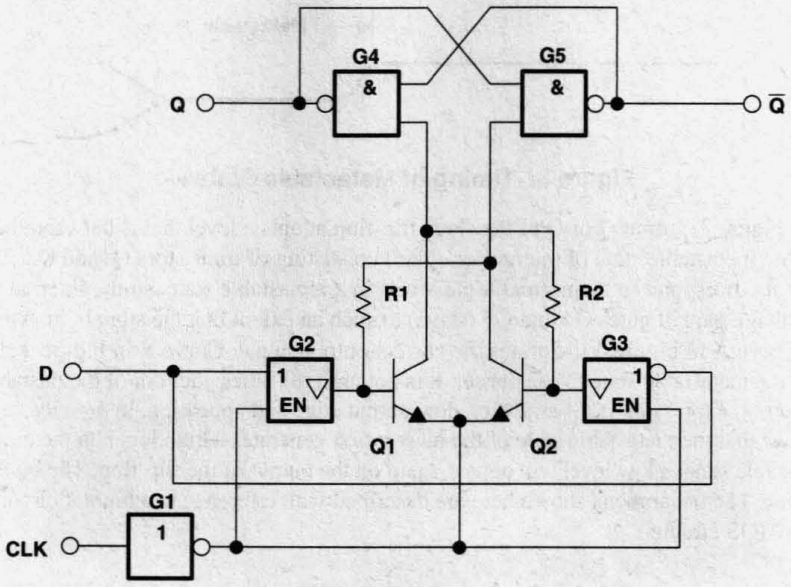


Figure 1. Bipolar Master-Slave D-Type Flip-Flop

Flip-flop operation, as described here, can only be ensured if the setup time and the hold time on the D input are maintained (see Figure 2). This means that for a short time before the positive edge on the CLK input (setup time) and a short time afterward (hold time) the level on the D input must not change if the above function is to be executed correctly.

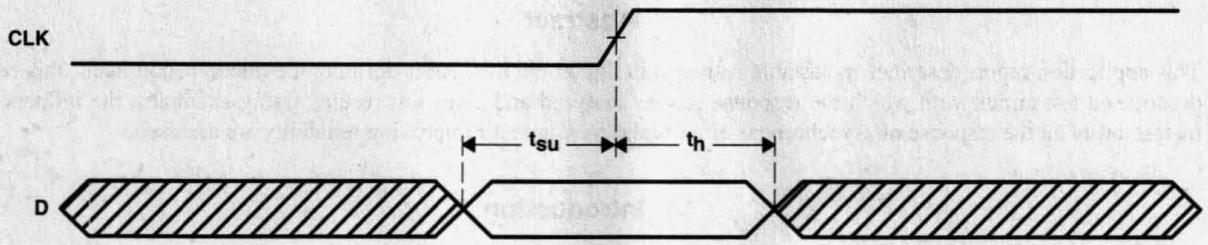


Figure 2. Timing Conditions of a D-Type Flip-Flop

In synchronous systems this timing can be maintained easily. But the situation is different with asynchronous circuits, in particular, synchronization circuits. Assume that, because of a change in level on the D input, the voltage on the output of gate G2 goes from low to high, meaning that the voltage on the output of gate G3 goes from high to low, and that the clock signal switches at the same time. If this happens at the instant when the difference in voltage between the two bases of transistors Q1and Q2 is virtually zero, the master flip-flop will not be able to adopt a stable, defined state. The logic state is neither high nor low. This is known as a metastable state. As a consequence, no defined state of the slave flip-flop is ensured under these circumstances.

The output signal of this flip-flop also adopts an unstable or metastable state (see Figure 3). The noise of transistors Q1 and Q2 (the master flip-flop forms a feedback amplifier) and interference penetrating from the exterior ensures that the master flip-flop and, consequently, the slave revert to one of the two possible but unpredictable stable states after a certain time.

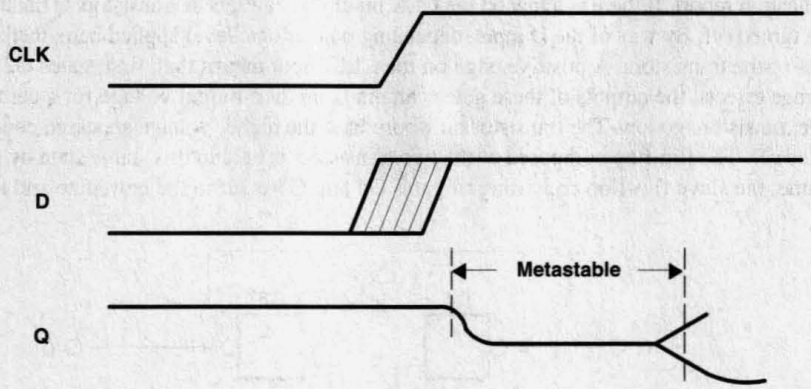


Figure 3. Timing of Metastable States

In the case illustrated in Figure 3, output Q or $\overline{Q}$ of the slave flip-flop adopts a level that is between the proper low and high levels. The output is in the metastable state of the master circuit consisting of transistors Q1and Q2. The output voltages of the master flip-flop do not correspond to the normal logic levels in a metastable state, so the internal voltage values can be corrupted through the voltage gain of gates G4 and G5 (slave) to such an extent that the signals shown in Figure 4 are on the output of the flip-flop. Curve A in Figure 4 illustrates the correct output signal. Curve B in Figure 4 shows that the slave, at first, does not recognize the metastable state of the master. It is not until the latter goes out of the unstable state that a reaction can be detected on the output, expressing itself as a very slow output edge and appearing, in practice, as a much longer delay. Curve C in Figure 4 shows that the metastable state of the master first generates a high level on the output of the slave. If the master then reverts to a stable state, a low level will appear again on the output of the flip-flop. The inverted signal shapes can be viewed in the same way. The phenomena shown here are described with reference to a bipolar circuit, but the same effects occur in CMOS and BiCMOS circuits.

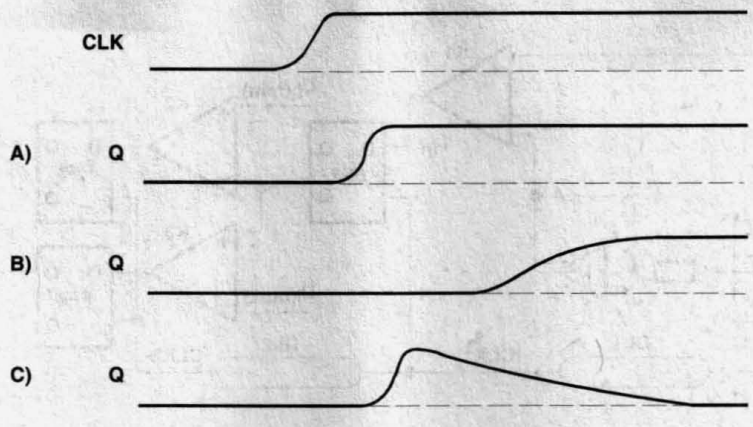


Figure 4. Different Output Signals in the Metastable State

Analyzing the metastable state of flip-flops is difficult because the critical time window in which the unstable state described may be generated is extremely short, about 10 to 100 ps.

In a circuit in which an asynchronous signal is synchronized with a clock, the mean time between failures (MTBF) in which a failure (metastable state) occurs is calculated from the frequency of the asynchronous signal (f_{in}), the clock frequency (f_{clk}), and the duration of the critical time window (t_d):

$$\text{MTBF} = \frac{1}{f_{in} \times f_{clk} \times t_d} \quad (1)$$

For f_{clk} = 1 MHz, f_{in} = 1 kHz, and t_d = 30 ps, the result is:

$$\text{MTBF} = \frac{1}{1\ \text{Hz} \times 1\ \text{MHz} \times 30\ \text{ps}} = 33.3\ \text{s} \quad (2)$$

A designer using a flip-flop to synchronize two signals in this application cannot expect the maximum delays stated in the data sheets. To ensure reliable operation of the system, it is necessary to know how long to wait after the clock pulse before the data can be evaluated. Conventional test equipment is not capable of measuring these parameters. Therefore, a special test circuit is needed to determine the MTBF and the time (t_x) between the clock edge and a valid signal on the Q output. Once these parameters are known, the designer can choose the type of flip-flop to be used and after how much time valid data can be expected.

3 Description of Test Circuit

The probability of a flip-flop going into a metastable state is at its greatest when the input signal (f_{in}) always violates the setup-time and hold-time conditions. This is the case when the state on the D input of a flip-flop changes with each clock edge. Any other relationship between the frequency of the signal on the D input and the clock frequency would reduce the probability of the flip-flop that is to be tested going into a metastable state. The worst case is when the frequency (f_{in}) on the D input is precisely one-half the clock frequency (f_{clk}).

Figure 5 shows a simplified test circuit for determining the MTBF and t_x for a particular flip-flop. An oscillator (O1) with a frequency of 1 MHz drives flip-flop FF1, which is configured as a 2:1 divider, thus satisfying the condition $f_{in} = 0.5\ f_{clk}$. To increase the probability of the tested flip-flop going into a metastable state, the high/low or low/high transition of the signal on the D input must jitter on the edge at the clock input. The width of this jitter should be equal to or greater than the sum of the setup and hold times of the flip-flop being tested. So the output signal of flip-flop FF1 is applied to an integrator (I) that slows down the rise or fall time to about 30 ns ($t_{su} + t_h$). The signal obtained in this way is impressed on the delta signal of the free-running oscillator O2 (f = 30 kHz) in comparator K1. This produces the data signal for the tested flip-flop FF2 on the output of the comparator, with the positive or negative edge jittering by 30 ns. The signal of oscillator O1 is applied at the same time via delay line DL1 to the clock input of the flip-flop that is to be tested (f_{CLK1}). This delay line compensates for the delays of flip-flop FF1, integrator I, and comparator K1. It is chosen so that the jitter on the D input of the flip-flop to be tested covers the setup and hold times stated in the data sheet (see Figure 6).

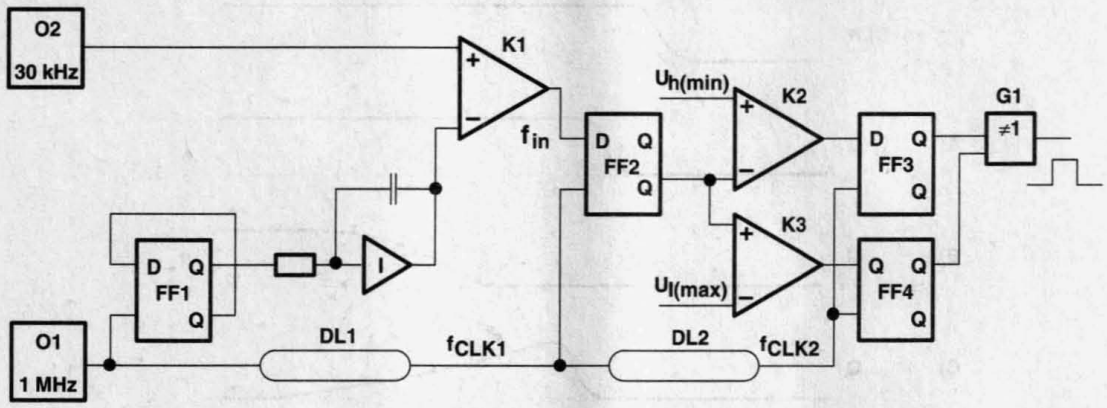


Figure 5. Test Circuit for Examining the Metastable State

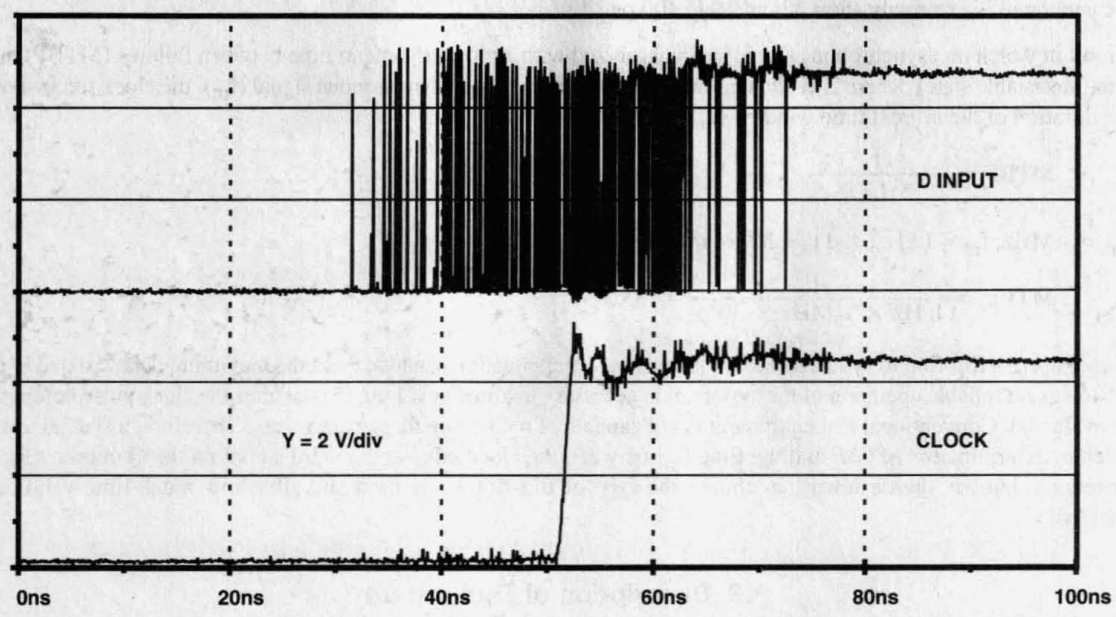


Figure 6. Oscillogram of Clock and Data Signal on Flip-Flop FF2

The output of flip-flop FF2 is then applied to comparators K2 and K3, which form a window comparator. Their outputs adopt the same state when there is a valid high or low level on the output of FF2 but adopt different states when the output voltage (V_O) of the flip-flop is in an undefined range:

$$V_{IH(min)} > V_O > V_{IL(max)} \quad (3)$$

The clock signal (f_{CLK2}), delayed by the time (t_x) by delay line DL2, samples the comparator outputs after this same time and sets flip-flops FF3 and FF4 accordingly. If there is a metastable state present at this time, the output of the exclusive-OR gate goes high.

This event is registered by the following counter. From the number N of metastable states detected within a certain time interval (t), it is then possible to determine the mean time between two metastable states according to equation 4:

$$MTBF = \frac{t}{N} \quad (4)$$

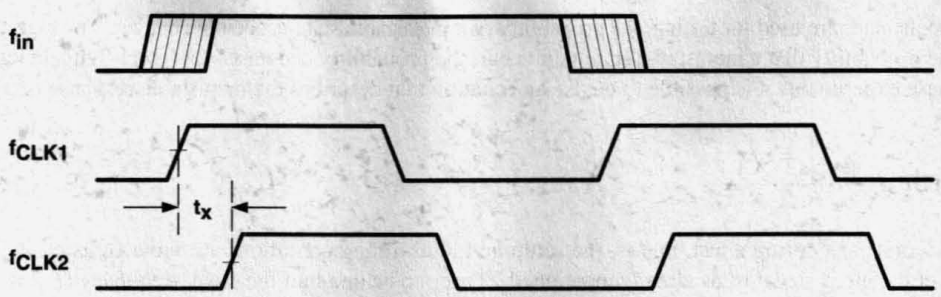


Figure 7. Timing of Test Signals

With the circuit described here, it is possible to determine the time between two failures as a function of the time (t_x). If this relation is entered on a semilogarithmic scale, the metastable characteristic of the flip-flop being examined for the required frequency of the input signal (f_{in}) is obtained.

Before discussing the test results, it is necessary to analyze the limitations of the test circuit, which influence the result. Two things can have a considerable influence on the test results: jitter of the input signal that is not centered on the clock signal and the delay of the evaluating circuit (K2, K3, FF3, and FF4).

If the edge of the input signal (f_{in}) does not jitter around the switching edge of the clock signal (f_{CLK1}), the probability that the flip-flop FF2 being tested will enter a metastable state is reduced. Care must be taken to ensure that the jitter of the input signal covers the time window formed by the setup and hold times.

In equation 1 it is assumed that the asynchronous signal alters in level randomly distributed over the clock period ($t_{fclk} = 1\ \mu s$). As shown in Figure 6, the signal on the D input of the device under test changes only in the mentioned time window (t_j) of 30 ns. The probability of the examined flip-flop being driven into the metastable state increases by the factor F:

$$F = \frac{t_{fclk}}{t_j} = \frac{1\ \mu s}{30\ ns} \tag{5}$$

The test results give the impression of a somewhat poorer response than can be expected in practice.

The evaluating circuit, consisting of comparators K1 and K2 and flip-flops FF3 and FF4, delays the output signal of the device under test and thus influences the result. For example, the flip-flop being tested might have left the metastable state, but the outputs of comparators K1 and K2 have not yet responded (because of the delay of this part of the circuit) when the edge of the clock signal (f_{CLK2}) arrives on flip-flops FF3 and FF4. It is difficult, in practice, to determine the magnitude of these errors precisely. To keep the error as small as possible, extremely fast devices in ECL technology were used in this part of the test circuit. This ensures that the uncertainty resulting from the delay of the comparators and the actual time of their sampling is smaller than 2 ns. When evaluating the test results, this error was taken into consideration by an appropriate horizontal shift of the line in Figure 8.

4 Test Results

Using the test circuit in Figure 5, different devices from the major logic families were examined with different values for t_x. The frequency of f_{clk} was 1 MHz, the frequency on the data input (f_{in}) was 500 kHz. The duration of the test was long enough for a sufficient number of failures to appear. The number of failures was then divided by the test duration. This result is the mean time between failures (MTBF) for a particular time (t_x). The result was also recorded on a semilogarithmic scale for further evaluation (see Figure 8).

Basically, circuits from the faster logic families also leave the metastable state faster. Different circuits of a logic family showed virtually the same response, with only very slight deviations. This was to be expected because the same technology and practically identical circuit techniques are used within a logic family. The curves in Figure 8 are typical. In measurements on circuits of the same type but from different fabrication batches, differences were noted that corresponded roughly to the variation of the propagation delay times stated in the data sheets. An allowance for this variation should be made when calculating the worst case for a particular circuit. Also, devices of the same type from different producers exhibited substantial differences.

If other clock frequencies are used for testing, the probability of a metastable state occurring changes. The higher the frequency, the greater is the probability that a metastable state will occur; the probability decreases for lower frequencies. With the data derived from these experiments it is possible to devise an equation that describes the metastable response of a component for any frequencies:

$$\text{MTBF} = \frac{\exp\,(T \times t_x)}{f_{clk} \times f_{in} \times T_O} \tag{6}$$

To produce the worst case during a test, that is, the setup-and-hold timing conditions are violated as often as possible, the frequency (f_{in}) of the input signal is, as already mentioned, chosen to be one-half the clock frequency ($f_{in} = 0.5\ f_{clk}$). On the basis of this, equation 6 changes to:

$$\text{MTBF} = \frac{\exp\,(T \times t_x)}{0.5 \times f_{clk}^2 \times T_O} \tag{7}$$

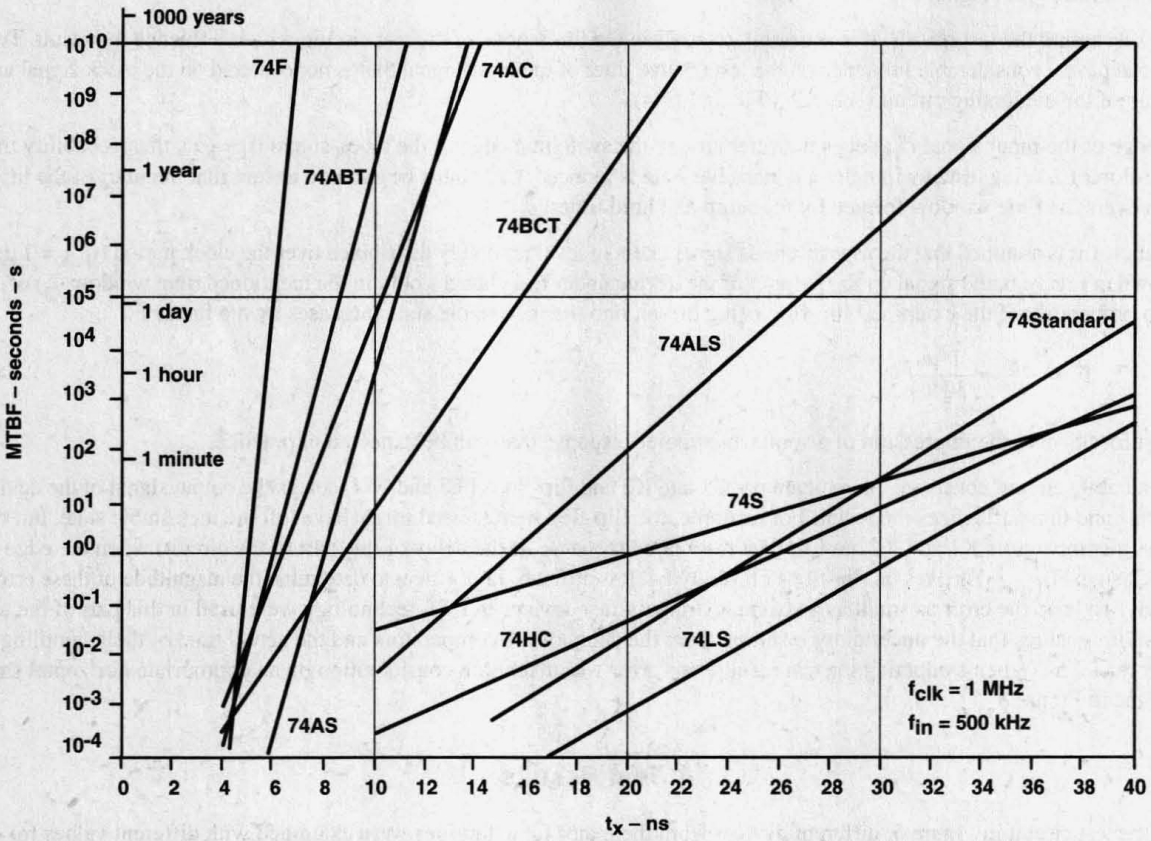


Figure 8. Metastable Characteristic of Logic Circuits

Constants T_O and T describe the metastable response of the circuit. These can be calculated for any circuit family from the experimental data in Figure 8. As an example, the values for the ALS family are determined.

Constant T determines the slope of the lines (for a semilogarithmic representation as in Figure 8, the e function appears as a straight line). So the figure can be determined from the following equation:

$$T = \frac{\ln \text{MTBF}(2) - \ln \text{MTBF}(1)}{t_{x(2)} - t_{x(1)}} \tag{8}$$

And in this case:

$$T = \frac{\ln 10^2 - \ln 10^{-2}}{19.5 \text{ ns} - 10.5 \text{ ns}} = 1.02/\text{ns} \tag{9}$$

To calculate constant T_O, solve equation 7 for T_O:

$$T_O = \frac{2 \times \exp (T \times t_x)}{\text{MTBF} \times f_{clk}^2} \tag{10}$$

So, in this case:

$$T_O = \frac{2 \times \exp (1.02 \times 19.5)}{100 \times 10^{12}} \tag{11}$$

By including the figures found for T and T_O in equation 6, the equation that describes the metastable response of ALS circuits is:

$$\text{MTBF} = \frac{\exp (1.02 \times t_x)}{f_{in} \times f_{clk} \times 8.7 \times 10^{-6}} \tag{12}$$

With this equation, describing the worst case, a designer can calculate the metastable response of ALS circuits for any given input and clock frequencies. The corresponding equations for other digital circuits can be determined by the same method. The values of constants (T) and (T_O) for the most popular logic circuits are listed in Table 1.

Table 1. Constants Describing the Metastable Behavior

FAMILY	T (1/ns)	T_O (s)
Std-TTL	0.74	2.9×10^{-4}
LS	0.74	4.8×10^{-3}
S	0.36	1.3×10^{-9}
ALS	1.0	8.7×10^{-6}
AS	4.0	1.4×10^{3}
F	9.2	1.9×10^{8}
BCT	1.51	1.14×10^{-6}
ABT	3.61	33×10^{-3}
HC	0.55	1.46×10^{-6}
AC	2.8	1.1×10^{-4}

First, equation 7 is logarithmized:

$$\ln \text{MTBF} = t_x \times T - \ln T_O - \ln(0.5 \times f_{clk}^2) \tag{13}$$

This shows that the constant (T) determines the slope of the lines and, consequently, has the greatest influence on the failure rate that can be expected. Constant (T) is in the exponent in equation 7, so it has a more than proportional effect on the probability that the output of a synchronization circuit will adopt a stable state. This means, in turn, that those logic circuits are best suited for this purpose where the constant (T) is a high figure, as in AC, AS, ABT, and F circuits. The circuits of the other families come into question when the circuit has a sufficiently long settling time. Constant (T_O) has a much smaller influence on the characteristics of the circuits. It produces a parallel shift of the lines in the diagram in Figure 8. Although the figures for this constant differ by several powers of ten in the different circuit families, the influence of the constant T is still far more dominant.

5 Circuitry Measures

It is not possible to prevent metastability in flip-flops, so systems must be designed so that, to a sufficient degree of probability, no malfunctions appear in the circuitry. The possible errors and how to avoid them are explained with reference to the circuit in Figure 9. The circuit in question is the interrupt input of a computer system. External interrupts are normally asynchronous to the timing of a system, so an appropriate synchronization stage (FF1) must be provided. If this flip-flop goes into a metastable state, for the reasons mentioned, the voltage levels on its output are no longer defined; in extreme cases they are close to the threshold voltages of the following circuit. Assume that gate G1, which collects the interrupt signals of different sources and signals the presence of an interrupt to the state control of the computer, accepts the metastable level as a valid interrupt signal. But the priority encoder, which is responsible for generating the appropriate interrupt vector, does not recognize this signal (in such a case differences in the threshold voltage of the individual circuits of just a few millivolts are enough to create the situation described here). The result is that the interrupt is triggered in the state control, but the wrong interrupt vector is generated, causing a dramatic malfunctioning of the computer. This result is aggravated by the fact that such errors are practically undetectable, even with high-grade instruments like logic analyzers. The sampling clock of the logic analyzer most likely will not sample the signals in question in the examined circuit at the critical moment. It is also highly improbable that the threshold voltage of this test instrument will have exactly the same value as the circuit examined, meaning that the abnormal operating state cannot be detected without a special, cumbersome test setup.

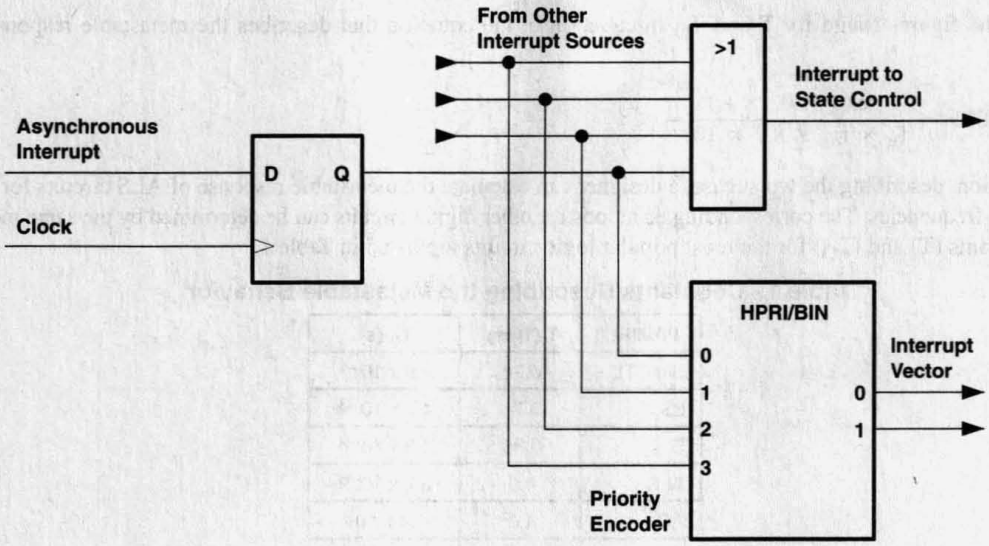


Figure 9. Interrupt Synchronization

Actual figures can be used to calculate the reliability or error rate (MTBF) of the above circuit. The data used are:

Type of flip-flop	SN74ALS74
Mean frequency of asynchronous interrupt signal	f_{in} = 10 kHz
System clock frequency	f_{clk} = 10 MHz
Setup time of following circuit	t_{su} = 25 ns

At the output of the synchronization stage, the settling time (t_x) is calculated as follows:

$$t_x = \frac{1}{f_{clk}} - t_{su} \tag{14}$$

$$t_x = \frac{1}{25\ \text{MHz}} - 15\ \text{ns} = 25\ \text{ns} \tag{15}$$

Taking equation 6 and the values of Table 1:

$$\text{MTBF} = \frac{\exp\ (1.0 \times 25\ \text{ns})}{25\ \text{MHz} \times 10\ \text{kHz} \times 8.8 \times 10^{-6}} = 3273\ \text{s} \approx 54\ \text{min} \tag{16}$$

This error rate is much too high. To reduce it, there is, first of all, the possibility of using circuits that exhibit a much shorter settling time and, therefore, leave the metastable state faster. As mentioned previously, these are the components in which the constant (T) is high, e.g., circuits of the SN74AS series. If you make the same calculation for an SN74AS74, the mean time between two failures (MTBF) is 2.4 x 10^{21} years, ensuring adequate reliability.

However, there are many applications in which you cannot just switch to a different family of circuits, e.g., where programmable circuits are used and one type of flip-flop is prescribed for all parts of the densely integrated circuitry. One remedy in this case is the use of a two-stage synchronization circuit (see Figure 10).

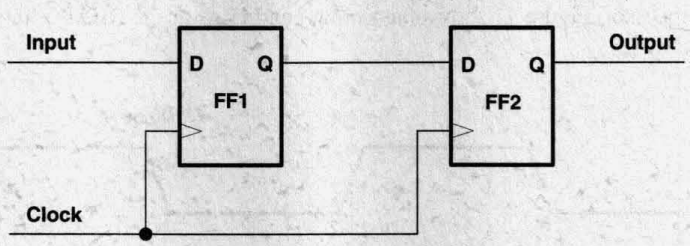


Figure 10. Two-Stage Synchronization Circuit

The second flip-flop receives the output signal of the first stage one clock period later and can go into a metastable state only if its input conditions are also violated. That is, the output of the first flip-flop is still metastable during its setup and hold time. So the critical input frequency $f_{in(2)}$ of the second stage is calculated from the reciprocal of the mean time between two failures of the first stage:

$$f_{in(2)} = \frac{1}{\text{MTBF}(1)} = \frac{f_{in(1)} \times f_{clk} \times T_O}{\exp\left[T \Big/ \left(\frac{1}{f_{clk} + t_{su}}\right)\right]} \tag{17}$$

If you again take equation 6 and insert the $f_{in(2)}$ value calculated here as the input frequency, the result, assuming that the same type of flip-flop is used in both stages of the synchronization circuit, is:

$$\text{MTBF}(2) = \frac{\exp\ (T - t_x)}{f_{in(2)} \times f_{clk} \times T_O} \tag{18}$$

or

$$\text{MTBF}(2) = \frac{\exp\ (T \times t_x) \times \exp\left[T \times \left(\frac{1}{f_{clk} - t_{su}}\right)\right]}{f_{in(2)} \times f_{CLK2} \times T_{O(2)}} \tag{19}$$

Now, go back to the synchronization circuit of the interrupt input that was described previously. Using one SN74ALS74 flip-flop, the MTBF was 54 minutes. Again, assuming that the second flip-flop is sampled after 25 ns, the result is:

$$\text{MTBF}(2) = \frac{\exp\ (1.0 \times 25\text{ns})}{\left(\frac{1}{54\ \text{min}}\right) \times 25\ \text{MHz} \times 8.8 \times 10^{-6}} = 2\ \text{million years} \tag{20}$$

By selecting the right component or the right circuit, excellent reliability can be achieved without any difficulty, even in time-critical applications. In the example shown above, the problem was resolved by incorporating an additional flip-flop stage, and without having to resort to especially fast circuit families. This was possible, for the most part, because an extra delay of one clock period in the interrupt input has no marked effect on system characteristics. In most modern microprocessors there are already appropriate circuits integrated (like the above two-stage synchronization circuit), which is why the engineer only has to take particular measures when designing special interrupt control circuits). With the READY input of a microprocessor, for example, things are different. For this kind of input there are setup and hold times specified in the data sheets for the devices, as with flip-flops, that must be maintained. The integration of an extra flip-flop in the processor, reducing the probability of errors through metastable states, is not wise because such a circuit would extend each bus cycle by one clock period in synchronous systems also and, in most cases, the processor works synchronously with the assigned memory. Such integration is not acceptable. For asynchronous operation an additional synchronization stage must be provided externally (see Figure 12). To arrive at a reliable circuit and avoid unnecessary delays, the critical times must be analyzed closely. This now will be done for the TMS320C25 microprocessor. Figure 11 shows the timing conditions of the READY input and the associated clock signals CLKOUT1 and CLKOUT2.

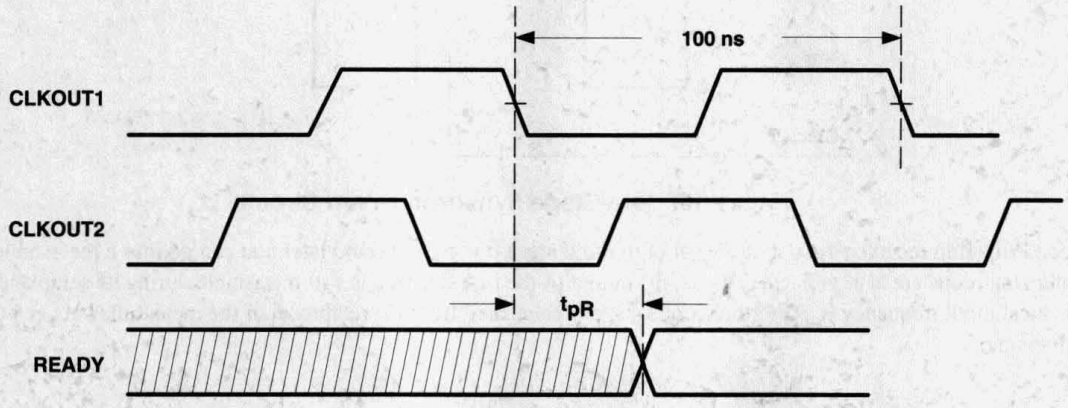


Figure 11. Timing Conditions of READY Signal in TMS320C25

For synchronization purposes, the negative edge of the clock CLKOUT1 is used. The READY signal must, when referred to this event, be valid after a time of t_{pR} = 30 ns. A D-type flip-flop, as required in this application, is triggered with the positive edge, so the CLKOUT1 signal has to be inverted. The SN74AS04 inverter that is used for this delays the clock signal by a maximum of t_{pd} = 5 ns. The system clock frequency is f_{clk} = 10 MHz. Assuming that the mean data rate is f_D = 5 MHz and that a flip-flop of the type SN74ALS74 is used, equation 6 and Table 1 produce:

$$\text{MTBF} = \frac{\exp\left[T \times \left(t_{pR} - t_{pd}\right)\right]}{f_{CLKOUT1} \times f_D \times T_O} \tag{21}$$

$$\text{MTBF} = \frac{\exp\left[1.0 \times (30\text{ ns} - 5\text{ ns})\right]}{10\text{ MHz} \times 5\text{ MHz} \times 8.8 \times 10^{-6}} = 163\text{ s} \tag{22}$$

In this case, a synchronization error can be expected about every 2.3 min, which, as experience shows, leads to a crash, making it unacceptable. If you use an SN74AS74 flip-flop instead, the MTBF is more acceptable:

$$\text{MTBF} = \frac{\exp\left[4.03 \times (30\text{ ns} - 5\text{ ns})\right]}{10\text{ MHz} \times 5\text{ MHz} \times 1.4 \times 10^{3}} = 2.58 \times 10^{19}\text{ years} \tag{23}$$

Figure 12 illustrates the circuit in question.

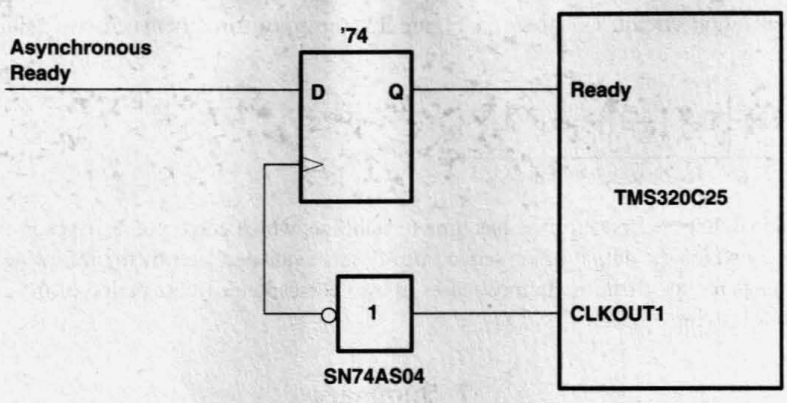


Figure 12. Synchronization of READY Input

6 Integrated Synchronization Circuits

There is nothing more obvious than integrating the two-stage synchronization devices described previously into one circuit in order to reduce the component count in a system. Figure 13 shows the circuit of such a synchronization stage in an SN74AS4374B.

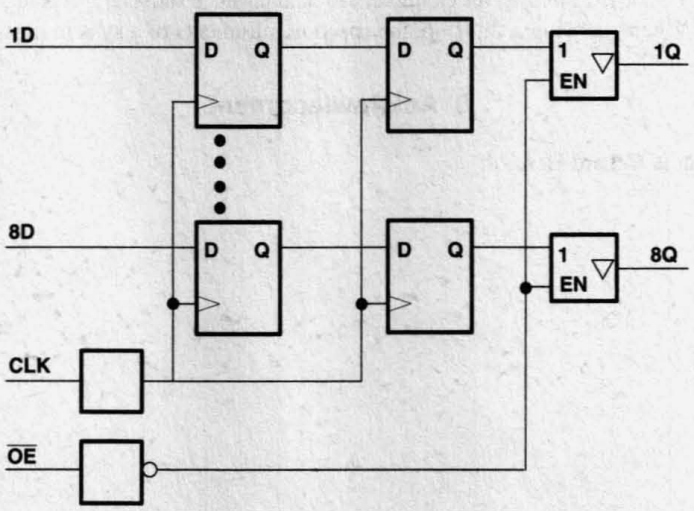


Figure 13. Logic Diagram of SN74AS4374B Synchronization Circuit

This integration produces additional advantages in terms of metastable response and, thus, system reliability. The first flip-flop requires no buffer stage at its output, which is largely responsible for the delay of the flip-flop, so its delay is considerably shorter than with an SN74AS74, for example. This time saving (about 1 to 2 ns) is then available in addition for stabilization of the first flip-flop if it goes into a metastable state. Furthermore, the D input of the second flip-flop does not need an input buffer stage, thus reducing the setup time at this point by about 0.5 to 1 ns. The time gained here is also available for stabilization of the first stage after a metastable state.

Constants (T) and (T_O) for this flip-flop were derived experimentally and are:

$$T = 2.4 \text{ and } T_O = 3.96 \times 10^{-9} \quad (24)$$

In a two-stage synchronization circuit, as shown in Figure 13, the mean time between two failures is calculated using equation 25:

$$\text{MTBF} = \frac{\exp\left[T \times \left(\frac{1}{f_{clk}}\right)\right] \times \exp\,(T \times t_x)}{f_{in} \times f_{CLK2} \times T_{O(2)}} \tag{25}$$

For simplicity, it is assumed that the first flip-flop has time to stabilize, which corresponds to precisely the clock period. The time t_x is again the time by which the output of the second flip-flop is evaluated later by the following circuit, that is, the time that the second flip-flop has for stabilization. In most cases, it also corresponds to the period of the clock frequency reduced by the setup time of the following circuit.

7 Summary

The metastable characteristic of a flip-flop in a synchronization circuit determines, to a large degree, the reliability of a system. On the basis of what has been said in this report, the designer can decide what type of flip-flop should be used in a given application and to what extent the metastable response will be manifest.

From the experimental data in Figure 8 it can be seen that fast logic circuits, like those of the series SN74AS, SN74F, 74AC, or SN74ABT, exhibit the best metastable response. These devices have a very short setup-and-hold time window, thus reducing the probability that they will go into a metastable state. Apart from this, they return to a stable state much faster if they have gone metastable. But ALS, LS, or HC circuits, for example, can also produce satisfactory results if the clock frequency in the application is low enough. When choosing a flip-flop, the speed requirements of a system must be considered.

8 Acknowledgment

The author of this document is Eilhard Haseloff.

Timing Measurements With Fast Logic Circuits

SDYA015
November 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title *Page*

Abstract **3–93**

1 Introduction **3–93**

2 Theory **3–93**
2.1 Methods of Impedance Matching 3–94
2.2 Theoretical Voltage Waveforms 3–95
2.3 Impedance of Striplines 3–99

3 Test Setup **3–102**
3.1 Inputs 3–102
3.2 Outputs 3–102
3.3 Bidirectional Connections 3–104
3.4 Supply Voltage 3–104
3.5 Example of a Test Setup 3–104
3.5.1 ac-Test Motherboard 3–105
3.5.2 ac-Test DUT Board 3–106
3.5.3 Test Results With ac-Test Motherboard 3–110

4 Summary **3–110**

Acknowledgment **3–110**

List of Illustrations

Figure *Title* *Page*

1 Wave Propagation Along a Line 3–93
2 Methods of Line Matching 3–94
3 Voltage Waveforms With Incorrect Termination (Z_L = 40 Ω, No Terminating Resistor) 3–96
4 Voltage Waveforms With Incorrect Termination (Z_L = 40 Ω, Terminating Resistor of 50 Ω) 3–96
5 Voltage Waveforms With Impedance Matching (Z_L = 50 Ω, No Terminating Resistor) 3–97
6 Voltage Waveforms With Impedance Matching (Z_L = 50 Ω, Terminating Resistor of 50 Ω) 3–97
7 Voltage Waveforms With Incorrect Termination (Z_L = 60 Ω, No Terminating Resistor) 3–98
8 Voltage Waveforms With Incorrect Termination (Z_L = 60 Ω, Terminating Resistor of 50 Ω) 3–98
9 L′ and C′ of Microstriplines 3–100
10 Characteristic Impedance of a Microstripline 3–101
11 Theoretically Calculated Waveform at the Beginning and End of an Unterminated 50-Ω Line Driven by an SN74F245 3–103
12 Decoupling of a Signal Using a Load of 500 Ω and 50 pF to GND and Test Equipment With an Input Resistance of 50 Ω 3–104
13 Interconnection Area for the Configuration of Each Channel 3–105
14 ac-Test Motherboard Rev 2.0 3–106

List of Illustrations (continued)

Figure	*Title*	*Page*
15	Circuit at the Input of the SN74ACT7801FN DUT Board	3–106
16	Circuit of an Output of the SN74ACT7801FN DUT Board	3–107
17	Circuit of an Output of the SN74ACT7801FN DUT Board With a Load Circuit of 500 Ω/50 pF to GND, Assuming a Signal Analyzer With an Input Resistance of 50 Ω	3–107
18	Cross-Section of the SN74ACT7801FN DUT Board, With the Printed Line and the Position of Passive Components for One Input or Output	3–107
19	Topside of the ac-Test DUT Board for the FIFO SN74ACT7801FN in 68-Pin PLCC Package	3–108
20	Underside of the ac-Test DUT Board for the FIFO SN74ACT7801FN in 68-Pin PLCC Package	3–109
21	Transmission Loss Measured on Channel 82 of the ac-Test Motherboard Connected to the ac-Test DUT Board for the SN74ACT7801FN FIFO	3–110

Appendices

Title	*Page*
Appendix A	**3–111**
ac-Performance Board Documentation	**3–111**
A-1 Introduction	**3–111**
A-2 Specifications	**3–111**
A-2.1 Mechanical Dimensions	3–111
A-2.2 Electrical Characteristics	3–111
A-2.3 Temperature Range	3–111
A-3 Description of Operation	**3–112**
A-3.1 ac-Performance Board	3–112
A-3.2 Jumper Matrix	3–112
A-3.3 DUT Board Rev. 21 for 24-/28-Pin SO Package	3–113
A-3.4 DUT Board Rev. 22 for 56-Pin SSO Package	3–115
A-3.5 DUT Board Rev. 23 for 100-Pin SQF Package	3–117
A-4 Description of Applications	**3–119**
A-4.1 Measuring Transit Time	3–119
A-5 Description of Signals	**3–120**
A-5.1 Signal Waveforms	3–120
A-5.2 Description of the Transmission-Loss Measurement	3–121
A-5.3 Results of the Transmission-Loss Measurement	3–122
A-5.4 Description of the TDR Measurement	3–123
A-5.5 Result of the TDR Measurement	3–124
A-6 Parts List	**3–125**
Acknowledgment	**3–125**

List of Illustrations

Figure	*Title*	*Page*
A-1	ac-Performance Board	3–112
A-2	Jumper Matrix	3–113
A-3	DUT Board Rev. 21 (Top)	3–113
A-4	DUT Board Rev. 21 (Bottom)	3–114
A-5	DUT Board Rev. 22 (Top)	3–115
A-6	DUT Board Rev. 22 (Bottom)	3–116
A-7	DUT Board Rev. 23 (Top)	3–117
A-8	DUT Board Rev. 23 (Bottom)	3–118
A-9	Transit-Time Measurement Setup	3–119
A-10	Signal Waveforms Using ac-Performance Board and DUT Board Rev. 23	3–120
A-11	Principal Test Setup for Transmission-Loss Measurement	3–121
A-12	Frequency Dependency of the Transmission Loss Using Channel 62 of the ac-Performance Board in Conjunction With the DUT Board Rev. 23	3–122
A-13	Frequency Dependency of the Transmission Loss Using Channel 82-57 of the ac-Performance Board in Conjunction With the DUT Board Rev. 23	3–122
A-14	Principal Test Setup for the TDR Measurement	3–123
A-15	Time Dependency of rho Using Channel 32 on the ac-Performance Board With the DUT Board Rev. 23	3–124
A-16	Time Dependency of rho Using Channel 32 With the Symmetrical Cross-Coupled Channel 73 (in Push-Pull) on the ac-Performance Board With the DUT Board Rev. 23	3–124

Abstract

This application report describes problems that can occur when making timing measurements with fast logic circuits. Introduction to methods of impedance matching and the determination of the impedance of a stripline are followed by the requirements for an efficient test setup. The report concludes with an example of such a test setup.

1 Introduction

The availability of ever-faster electronic components allows the design of more effective and efficient end equipment. However, this has led to increased problems from line reflections, resulting in signals having serious overshoot, undershoot, and steps on pulse edges.

When measuring the switching-time behavior of individual circuits, problems can arise with outputs having very steep edges, even under laboratory conditions. An appropriate test setup is the prerequisite for reliable, repeatable, and comparable measurement results. Essential conditions for a satisfactory test setup include:

- A stable power supply that also shows no voltage changes under conditions of varying high-frequency current
- An undistorted signal at the input of the device under test with no overshoots, undershoots, or steps on pulse edges
- A connection to the outputs of the device under test that does not influence the switching behavior
- Appropriate test equipment and knowledge of the influence of the equipment on the test setup

This report discusses problems and indicates possible solutions for timing measurements on individual devices.

2 Theory

If the rise and fall times of a signal are shorter than the signal transit time from the source to the end of the line, the designer must consider the resulting transient phenomena of voltage and current waves flowing forward and back along the line (see Figure 1). The signal waveform is determined by the:

- Internal resistance of the source (R_i)
- Characteristic impedance of the line (Z_L)
- Load resistance (R_L)
- Length of the line (L)

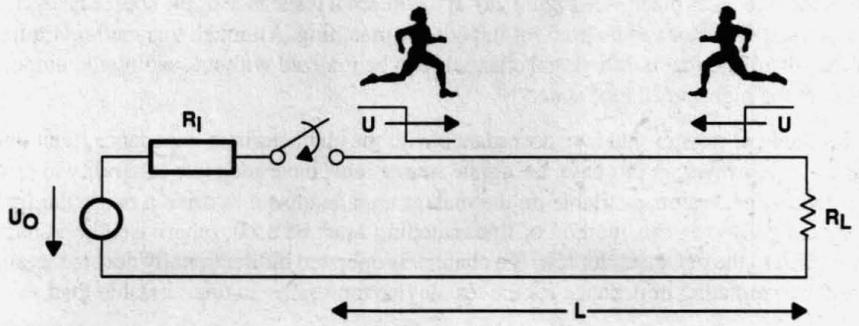


Figure 1. Wave Propagation Along a Line

2.1 Methods of Impedance Matching

Reflections of signals along an unterminated line cause overshoots, undershoots, or steps on pulse edges. Various methods of line matching are shown in Figure 2.

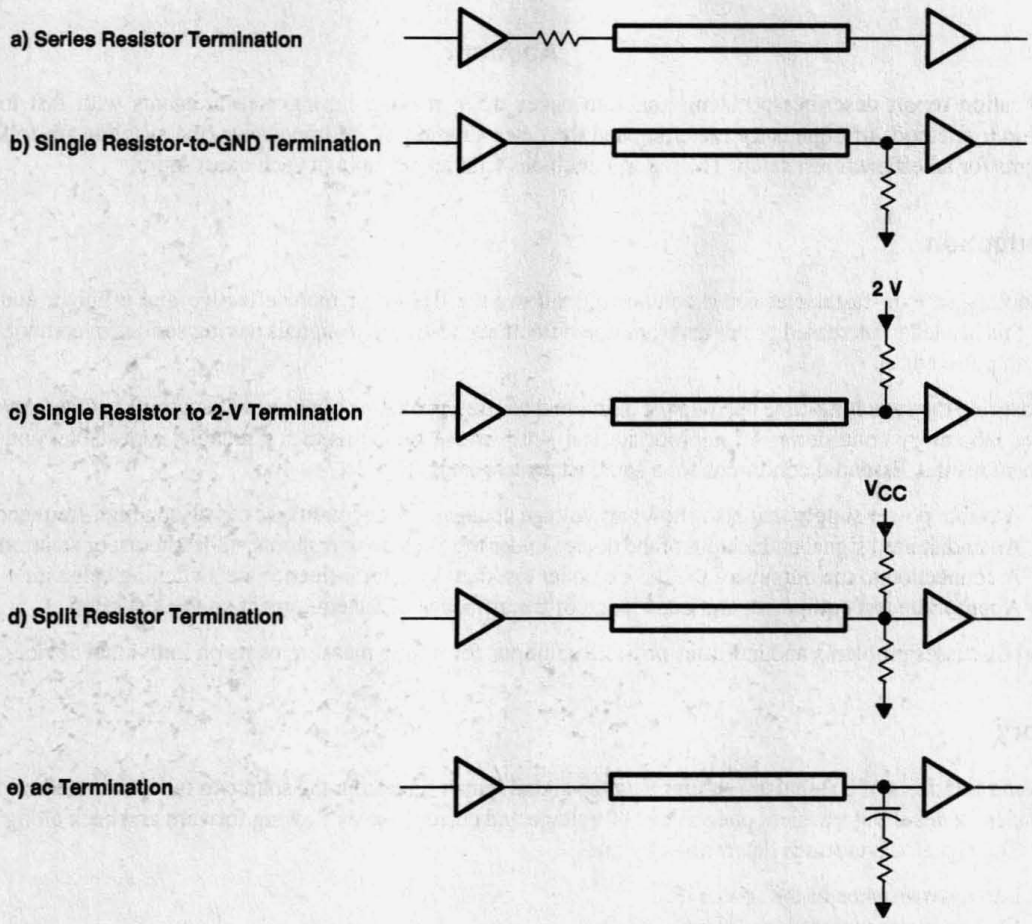


Figure 2. Methods of Line Matching

If the internal resistance of the source and the characteristic impedance of the line are matched exactly, no distortion of the waveform at the end of the line takes place (see Figure 2a). If the internal resistance of the source is less than the characteristic impedance of the line, a series resistor can be used for impedance matching. Although this method limits the drive capability of the source, it has the advantage that bidirectional channels can be realized without loading the output of the device under test when the source is in the high-impedance state.

If a value is chosen for the load resistor that is in accordance with the characteristic impedance, then line reflections will be eliminated (see Figure 2b). However, in this case, the signal source must have adequate capability to drive the relatively low resistance load. Many of the generators available on the market are already set to drive a particular terminating resistance, mostly 50 Ω. With such a generator, this method of line matching must be used; otherwise, the voltage level preset at the generator cannot be applied to the device under test. If a channel is operated bidirectionally during measurement, this method is not usable because the terminating impedance for the test device represents an unacceptable load.

If the dc current in the load resistance (and power consumption) needs to be reduced, the terminating resistance can be connected to a voltage other than 0 V, for example to 2 V (see Figure 2c). However, with this method, the voltage level at the input of the device under test will be determined by the voltage level of the source and, to a greater extent, by the voltage source of the line termination. In such a case, a precise test setup is no longer possible.

An additional option for matching the line is by using two resistors; the first is connected to 0 V and the second to V_{CC} (see Figure 2d). However, this method is not good practice for a test setup because the advantage of low dc current and power consumption is insignificant in this case; the resulting voltage level also depends on the source as well as on the supply voltage V_{CC}.

Another way of matching the line is to use a resistor and a capacitor in combination (see Figure 2e). In this case, the power consumption is reduced since the dc component is eliminated. The value of the capacitor can be estimated with the following equation:

$$R \times C > 4T \quad (1)$$

Where:

R = terminating resistor
C = terminating capacitor
T = signal propagation time from the beginning to the end of the line

The value of the capacitor needs to be chosen by trial and error so that when making a precise test setup, the type of line termination is not in question.

Signal generators commonly available are provided with an output resistor of 50 Ω, and the methods of line matching in Figures 2a and 2b can be chosen. The setting of the output voltage level is usually calibrated for a load resistor of 50 Ω, which is also the usual termination resistor of laboratory setups (see Figure 2b). The variation in Figure 2a is mainly applicable to production testing because, with it, bidirectional channels can be realized. The other three methods are not used for precise measurements in the laboratory.

2.2 Theoretical Voltage Waveforms

Using the Bergeron method, it is possible to theoretically determine waveforms on lines. The Bergeron method will not be explained here, but details can be found in the application report *The Bergeron Method*, literature number SDYA014.

Figures 3 through 8 show the voltage waveforms of a rising pulse at the beginning, in the middle, and at the end of a line. Falling pulses show similar behavior but with opposite polarities. The time of transit (T) of the signal from the beginning to the end of the line can be calculated using equation 4.

Figures show combinations of different series resistors without terminations (see Figures 3, 5, and 7) and with terminating resistors at the end of the line (see Figures 4, 6, and 8). Voltage waveforms with correctly terminated lines are shown in Figure 6; incorrect terminations are shown in Figures 3, 4, 5, 7, and 8.

The figures show that incorrect termination causes steps on the pulse edges or an overshoot of the signal. A line that is correctly matched with a series resistor delivers an undistorted waveform only at the end of the line; along the line there is a step on the pulse edge. Terminating the line with a load resistor ensures clean pulses along the entire length of the line.

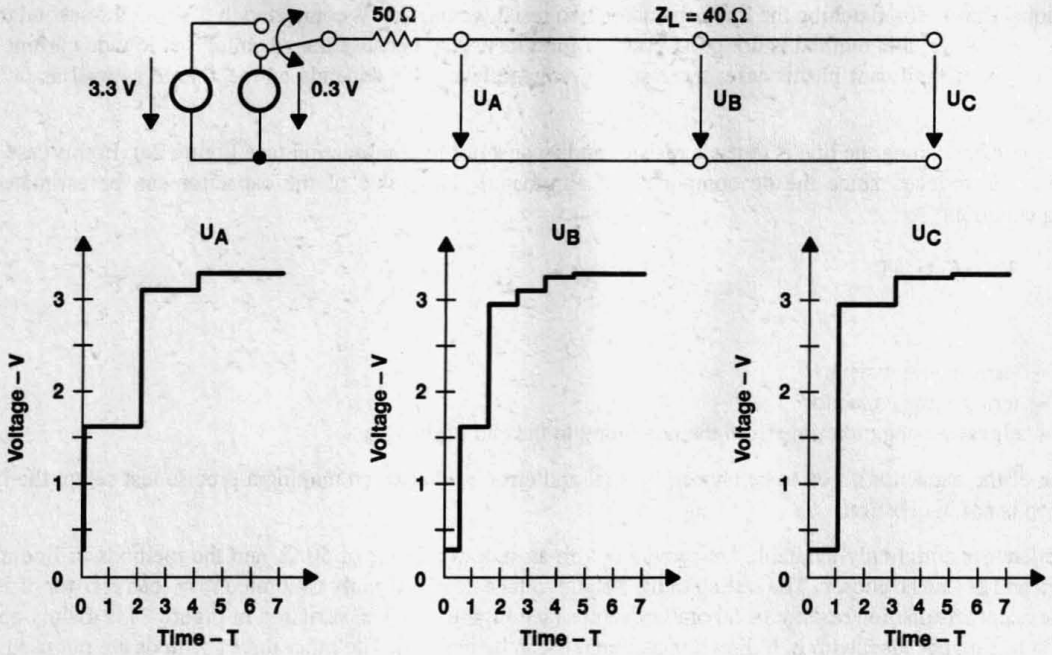


Figure 3. Voltage Waveforms With Incorrect Termination (Z_L = 40 Ω, No Terminating Resistor)

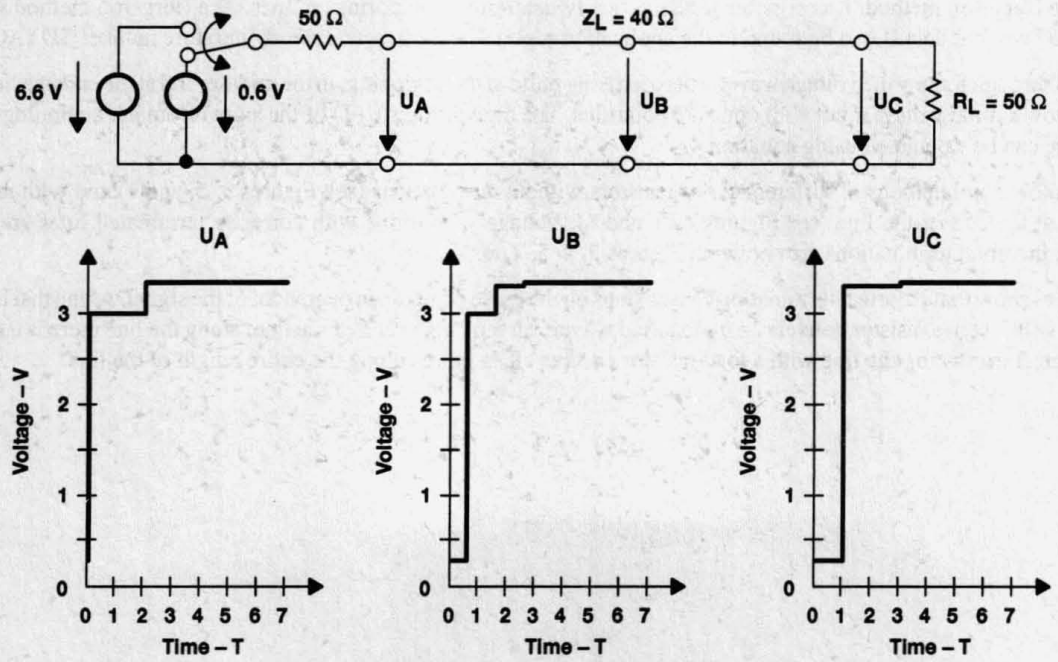


Figure 4. Voltage Waveforms With Incorrect Termination (Z_L = 40 Ω, Terminating Resistor of 50 Ω)

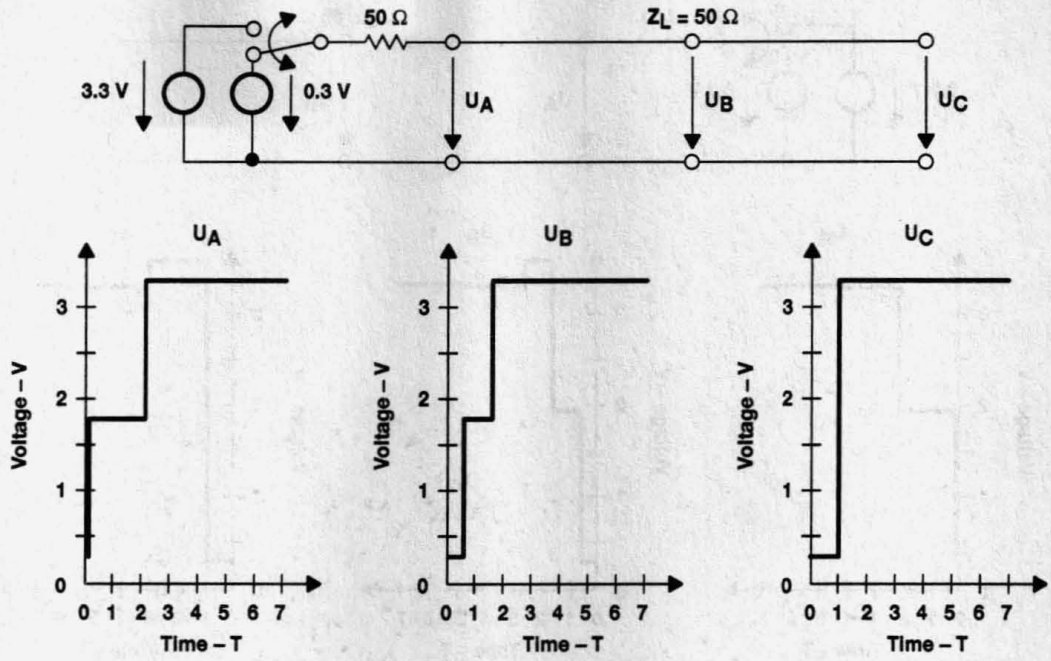


Figure 5. Voltage Waveforms With Impedance Matching (Z_L = 50 Ω, No Terminating Resistor)

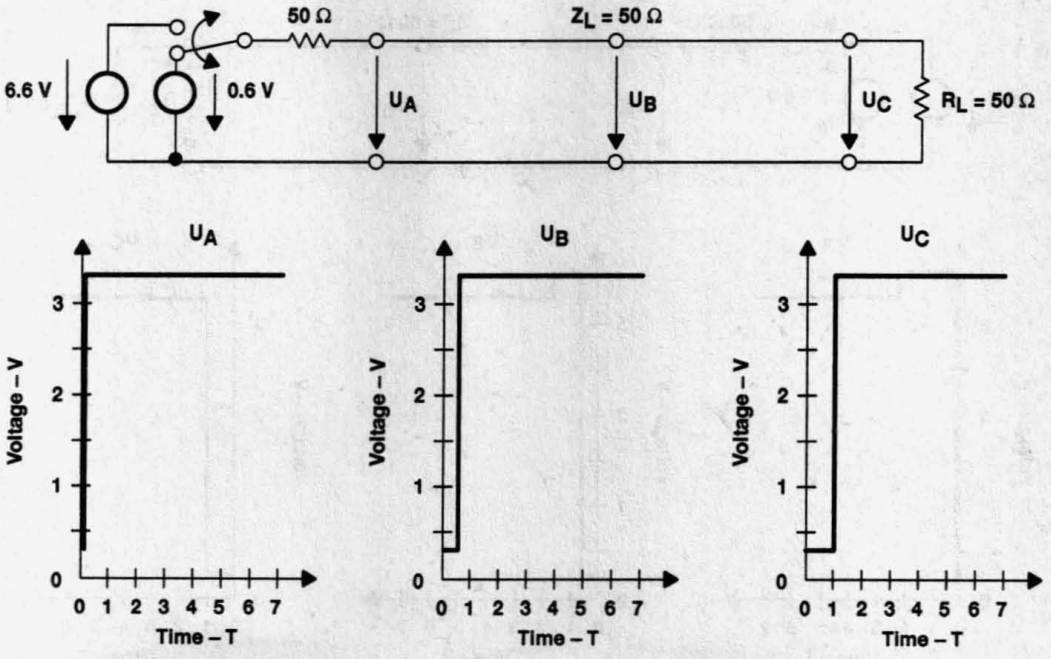


Figure 6. Voltage Waveforms With Impedance Matching (Z_L = 50 Ω, Terminating Resistor of 50 Ω)

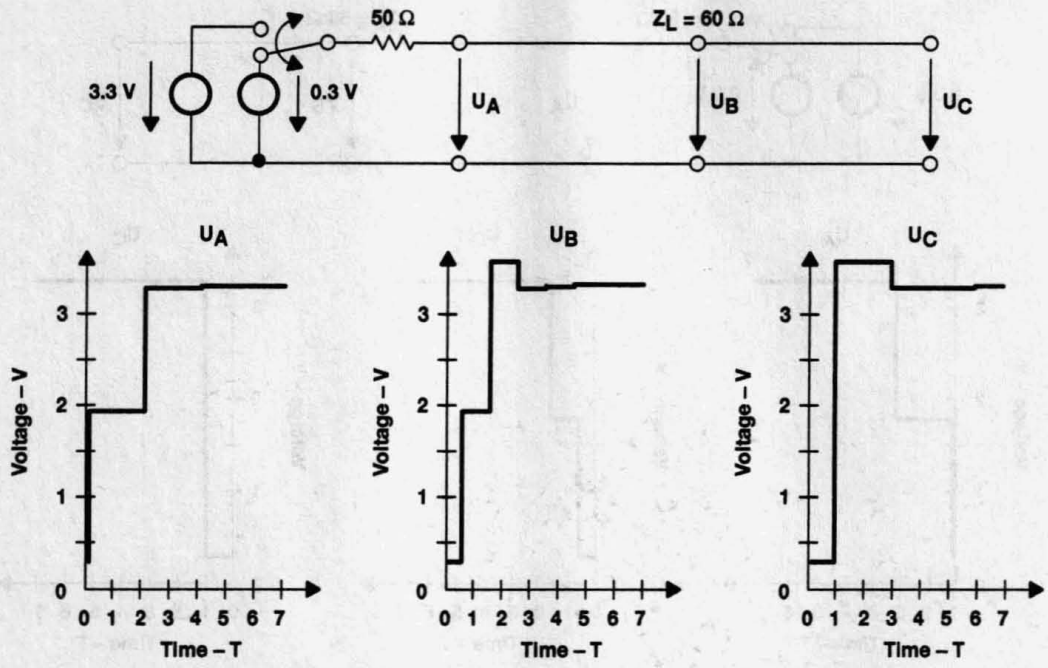


Figure 7. Voltage Waveforms With Incorrect Termination (Z_L = 60 Ω, No Terminating Resistor)

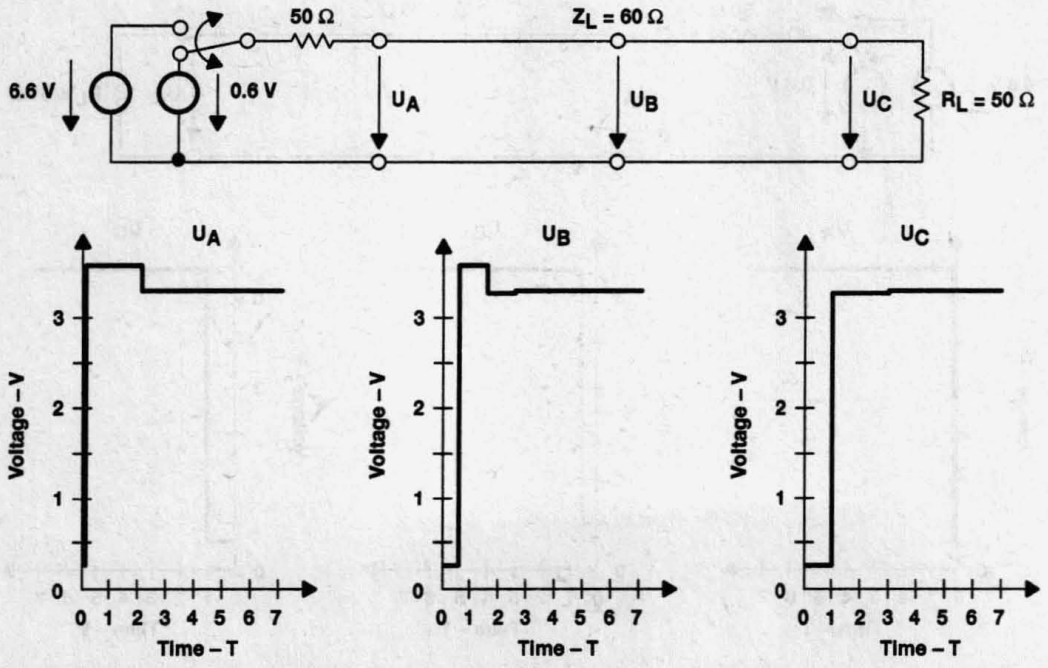


Figure 8. Voltage Waveforms With Incorrect Termination (Z_L = 60 Ω, Terminating Resistor of 50 Ω)

2.3 Impedance of Striplines

The characteristic dimension of a line is its impedance (Z_L), which, ignoring the resistive part, can be calculated as follows:

$$Z_L = \sqrt{\frac{L'}{C'}} \tag{2}$$

Where:

Z_L = impedance of the line
L' = inductance per unit of line length (nH/cm)
C' = capacitance per unit of line length (pF/cm)

The transit time (T) from the beginning to the end of the line can be calculated from the speed (v) of the signal:

$$v = \frac{1}{\sqrt{L' \times C'}} \tag{3}$$

$$T = \frac{1}{v} = 1 \times \sqrt{L' \times C'} \tag{4}$$

The two basic dimensions of a microstripline, the inductance per unit of line length (L') and the capacitance per unit of line length (C'), depend solely on the cross-sectional geometry and the relative permittivity (ε_r) (see Figure 9). The following expression can be deduced for the characteristic impedance of a microstripline:

$$Z_L = \frac{Z_O}{\sqrt{\epsilon_{r.eff}} \frac{w_{eff}}{h}} \tag{5}$$

Where:

Z_O = 120 π Ω; characteristic impedance of free space
$\varepsilon_{r.eff}$ = effective relative permittivity
w_{eff} = effective width of the microstripline
h = height of the dielectric

If $\varepsilon_r \leq 16$ and $w/h \geq 0.05$, the effective relative permittivity can be determined from equation 6 with a margin of error of < 1%.

$$\epsilon_{r.eff} = \frac{\epsilon_r + 1}{2} + \frac{(\epsilon_r - 1)F\left(\frac{w}{h}\right)}{2} \tag{6}$$

whereby the following applies:

if $w/h \leq 1$:

$$F\left(\frac{w}{h}\right) = \frac{1}{\sqrt{1 + 12\frac{w}{h}}} + 0.041\left(1 - \frac{w}{h}\right)^2$$

if $w/h \geq 1$:

$$F\left(\frac{w}{h}\right) = \frac{1}{\sqrt{1 + 12\frac{w}{h}}}$$

Where:

ε_r = relative permittivity of the dielectric
w = width of the microstripline
h = height of the dielectric

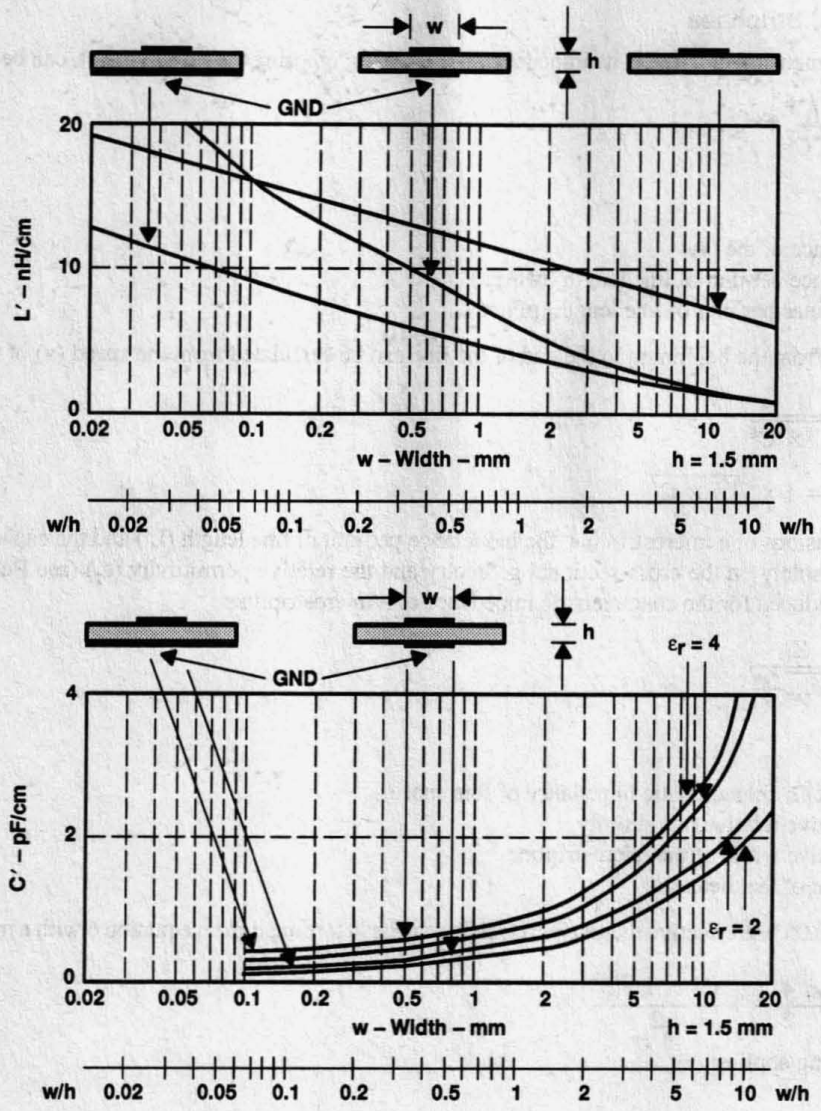


Figure 9. L′ and C′ of Microstriplines

The approximate ratio of the effective width of the microstripline to the width of the dielectric is determined using the following equation:

if w/h ≤ 1:

$$\frac{w_{eff}}{h} = 2\pi \frac{1}{\ln\left(8\frac{h}{w} + 0.25\frac{w}{h}\right)} \tag{7}$$

if w/h ≥ 1:

$$\frac{w_{eff}}{h} = \frac{w}{h} + 2.46 - 0.49\frac{h}{w} + \left(1 - \frac{h}{w}\right)^6$$

Where:

w = width of the microstripline
h = height of the dielectric

The characteristic impedance of a microstripline can be derived from the cross-sectional geometry and the relative permittivity of the circuit-board material using equations 5, 6, and 7. The curves in Figure 10, drawn using these calculations, show the characteristic impedance of a microstripline as a function of the parameters mentioned above.

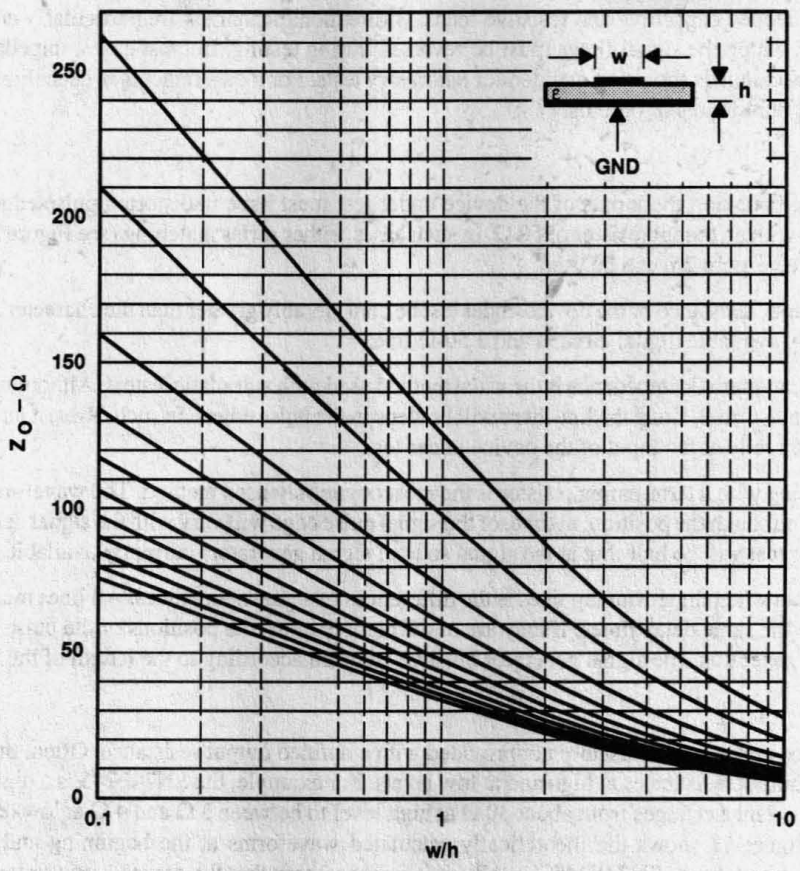


Figure 10. Characteristic Impedance of a Microstripline

Typical figures for the cross-sectional geometry and the dielectric constant for a line with a characteristic impedance of 50 Ω are given in Table 1.

Table 1. Typical Cross-Sectional Geometry and Dielectric Constant for a Line With a Characteristic Impedance of 50 Ω

w (μm)	h (μm)	ε_r	Z_L (Ω)
412	200	4.0	50.0
515	250	4.0	50.0
618	300	4.0	50.0
376	200	4.5	50.0
470	250	4.5	50.0
565	300	4.5	50.0
346	200	5.0	50.0
433	250	5.0	50.0
520	300	5.0	50.0

3 Test Setup

If the timing behavior of a fast logic circuit is evaluated, great care must be taken with the setup and the procedures used. Undistorted signals must be provided to the inputs of devices under test. Outputs must not be subjected to outside interference, apart from that of the intended capacitive and resistive loads. Bidirectional channels are particularly critical in this respect, because the direction in which the signal flows must be reversed during testing. In most cases, impedance matching is not possible, so bidirectional channels should be avoided for laboratory tests. For measurements in each direction, these channels should be configured as pure inputs or outputs.

3.1 Inputs

When evaluating timing behavior, the inputs of the device under test must have undistorted pulse edges. Generally, signal generators are provided with an output resistor of 50 Ω. In such cases, either series matching (see Figure 2a) or matching with a terminating resistor (see Figure 2b) can be used.

It is important that the input resistance of the device under test be considerably greater than the characteristic impedance. This is the case with currently available digital circuits and a 50-Ω line.

Series matching to the characteristic impedance is the usual method used with automatic testers. Although the signal waveform at the end of the line is undistorted, along the line there will be steps in the pulse edges. In such cases, if an oscilloscope is used, it should be connected directly at the input of the device under test.

In the laboratory, matching with a terminating resistor is the most commonly used method. The waveform of the signal along the line will not change, although the position, in time, of the signal pulse edge will vary with the signal delay time. The voltage level at the device under test will be half that at the signal source; signal generators currently available account for this.

A further important aspect when dimensioning lines is the differences of signal delay times. All lines must be the same length if all signals are to have the same delay times. If they are of different lengths, the positions of the pulse edges will no longer conform to those at the generator. The signal generator must be adjusted according to the length of the line.

3.2 Outputs

The outputs of the device under test are usually not provided with a defined output resistance. Often, there is a considerable difference between the output resistances at high and at low levels. For example, the SN74F245 is a digital IC with a bipolar output, whose output resistance changes from about 30 Ω at high level to between 3 Ω and 4 Ω at low level. In this case, line matching is difficult. Figure 11 shows the theoretically calculated waveforms at the beginning and end of a line of an unterminated 50-Ω line driven by an SN74F245. Usually, it is not necessary that the device being tested should drive a line.

Outputs usually have defined loads that should be as close as possible to the device under test.

An oscilloscope with a high resistance probe is usually used for precise measurement of timing behavior. Therefore, the input resistance of the measuring instrument can be ignored. However, the capacitive loading of the output by the probe may need to be taken into account.

All these requirements lead to the conclusion that, at the output:

- The load circuit and the probe head should be positioned as close as possible to the device under test.
- No stub line should be connected to the output (see Figure 11).

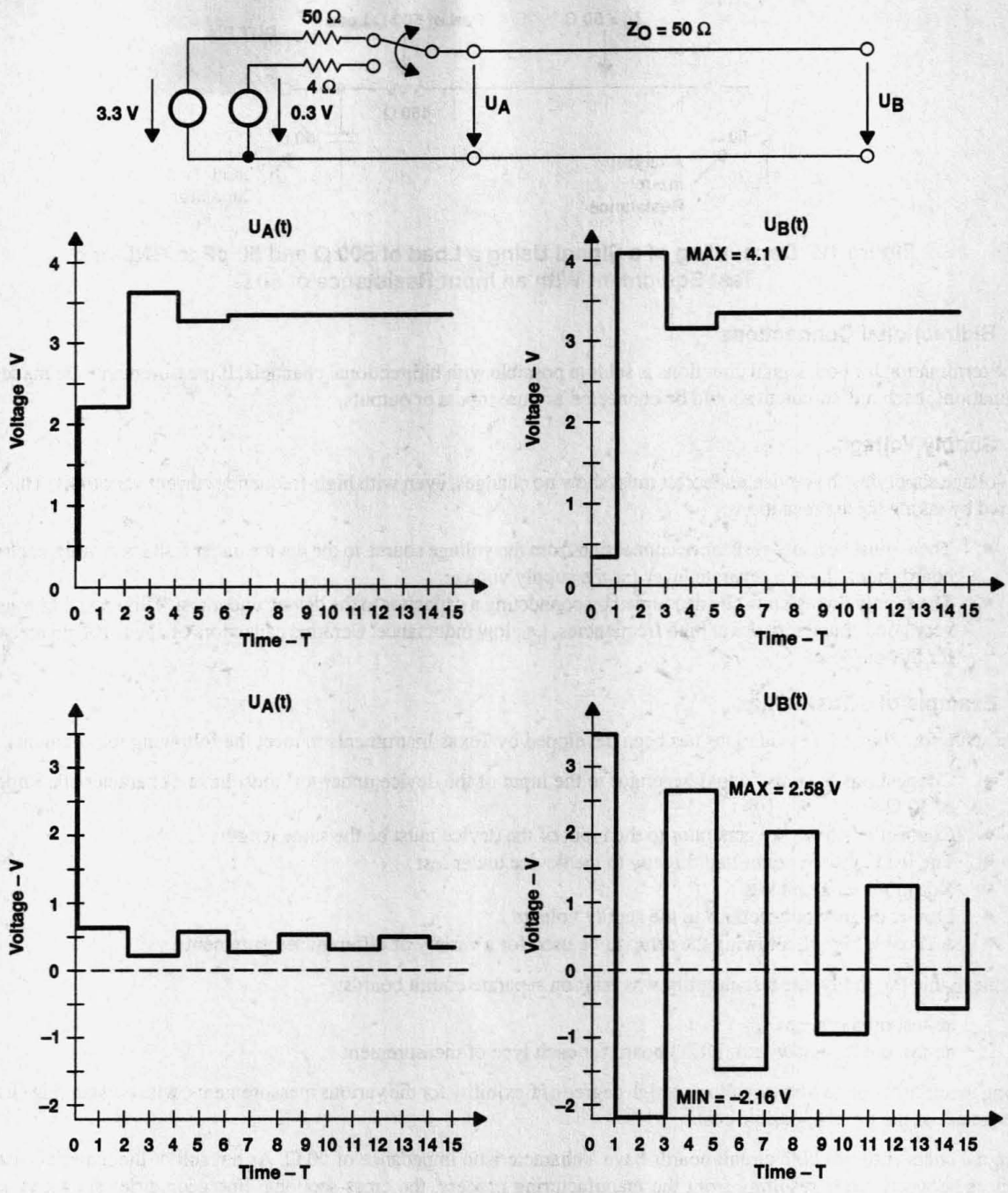


Figure 11. Theoretically Calculated Waveform at the Beginning and End of an Unterminated 50-Ω Line Driven by an SN74F245

Often, when evaluating the timing behavior of ICs, a load of 500 Ω and 50 pF to GND is specified. Figure 12 shows a measuring instrument with an input resistance of 50 Ω that solves the loading problem. The 50-Ω input resistance of the measuring instrument behaves as the terminating resistance of the 50-Ω line, although it is part of the 500-Ω load resistance. Thus, a 10:1 potential divider has been created, made up of the 450-Ω series resistor and the 50-Ω input resistance of the measuring equipment. When evaluating test results, the 10:1 potential divider and the signal transit time along the 50-Ω line to the test equipment must be taken into account. Again, the load capacitance of 50-pF should, if possible, be placed close to the output of the device under test.

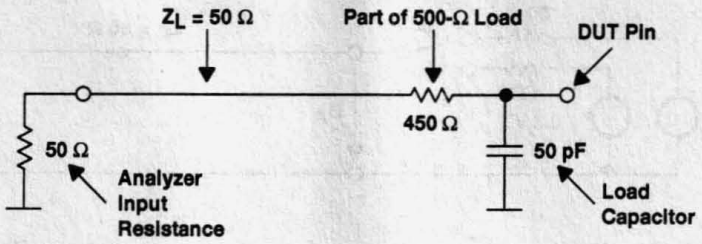


Figure 12. Decoupling of a Signal Using a Load of 500 Ω and 50 pF to GND and Test Equipment With an Input Resistance of 50 Ω

3.3 Bidirectional Connections

A line termination for both signal directions is seldom possible with bidirectional channels. If measurements are made at line terminations, each measurement should be connected as pure inputs or outputs.

3.4 Supply Voltage

The voltage supplying the device under test must show no changes, even with high-frequency current variations. This can be ensured by taking these precautions:

- There must be a low-resistance connection from the voltage source to the device under test. Preferably, each circuit board should have a separate layer for the supply voltage.
- The supply voltage must be decoupled by connecting a capacitor to the device under test. This capacitor must have very good characteristics at high frequencies, i.e., low inductance. Ceramic capacitors of about 100 nF are suitable for this purpose.

3.5 Example of a Test Setup

A test setup for laboratory evaluations has been developed by Texas Instruments to meet the following requirements:

- Connections from the signal generator to the input of the device under test must have a characteristic impedance of 50 Ω
- Connections from the generator to the input of the device must be the same length
- The load must be connected directly to the device under test
- No stub lines at outputs
- Low-resistance connections to the supply voltage
- A flexible layout, allowing the setup to be used for a variety of different measurements

To achieve this flexibility, the test circuitry was built on separate circuit boards:

1. ac-test motherboard
2. ac-test device-under-test (DUT) board for each type of measurement

Placing the circuitry on two boards allows a high degree of flexibility for the various measurements, with outstanding electrical performance at the lowest possible cost.

All signal connections to both circuit boards have a characteristic impedance of 50 Ω. As a result of the materials used and distances between layers resulting from the manufacturing process, the cross-sectional line geometries shown in Table 2 were achieved.

Table 2. Sectional Geometries of the Test-Setup Circuit Boards

w (μm)	h (μm)	ε_r	Z_L (Ω)
418	300	4.35	50.0

3.5.1 ac-Test Motherboard

The ac-test motherboard has five internal layers. One of each is used for the three voltage sources (DPS1, DPS2, and DPS3); the ground connection is made with two separate layers, and the layers are brought out with banana-plug sockets.

The board has HF sockets for a maximum of 84 channels that provide connections for word and pulse generators. These sockets are arranged in a circle to ensure the same line length from socket to test device. These sockets connect to an interconnection area through 50-Ω lines. This area has jumpers that allow the flexible configuration of each channel individually (see Figure 13). Signals that are applied to the device under test can be chosen as follows:

- Signal from the generator via the HF plug
- Supply voltage DPS1
- Supply voltage DPS2
- Supply voltage DPS3
- Ground connection

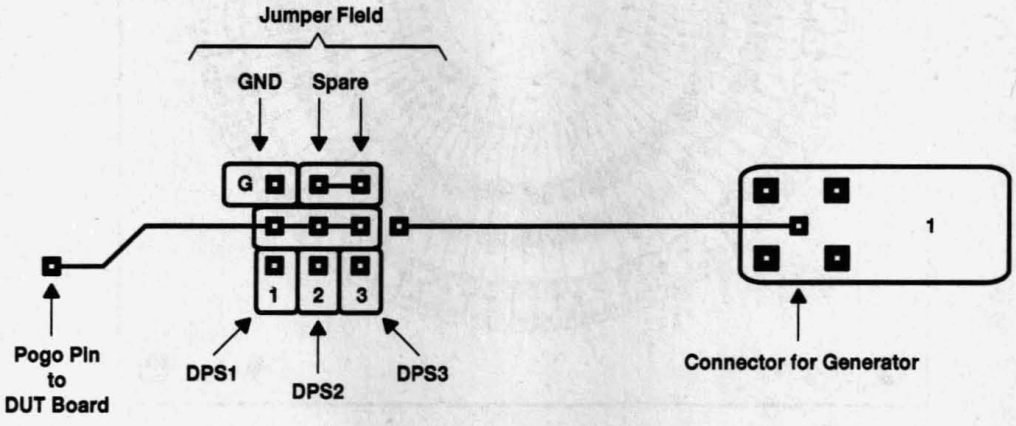


Figure 13. Interconnection Area for the Configuration of Each Channel

The signal goes from the interconnection area to the Pogo pins, arranged in a circle, which pass the signal on to the ac-test DUT board.

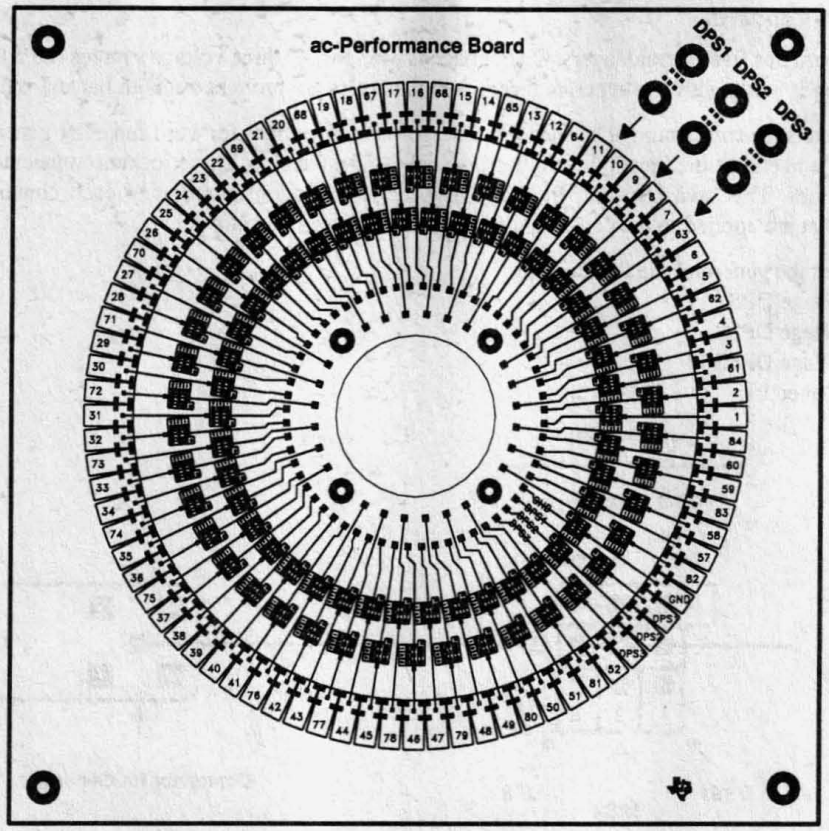


Figure 14. ac-Test Motherboard Rev. 2.0

3.5.2 ac-Test DUT Board

As an example of a DUT board, the circuit board for the SN74ACT7801FN 1024 × 18 first-in, first-out (FIFO) memory with a 68-pin plastic chip-carrier package is used. This IC has 27 inputs, 22 outputs, nine V_{CC} connections, and ten GND connections.

A track on the circuit board can be used equally well for either inputs or outputs.

The signal from the ac-test motherboard was taken to the input of the DUT using a jumper (a 0-Ω resistor). The circuit at the input of the DUT (see Figure 15) includes a 50-Ω terminating resistor between the end of the line and GND.

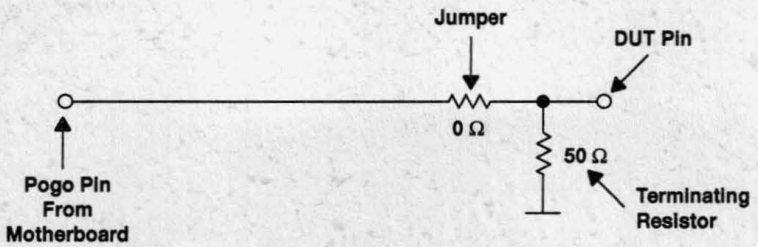


Figure 15. Circuit at the Input of the SN74ACT7801FN DUT Board

The jumper mentioned previously is removed when making timing measurements at the output pins. In this way, there are no unterminated stub lines at the output, and reflections are avoided. In addition, there is the possibility of soldering load circuits to V_{CC} and to GND (see Figure 16). The layout of the circuit board also allows the connection of measuring instruments with an input resistance of 50 Ω (see Figure 17).

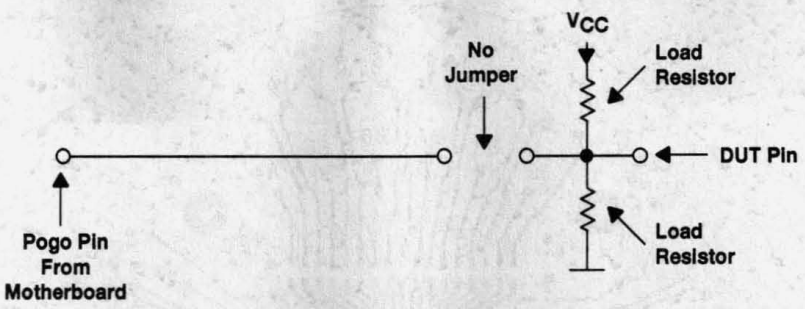


Figure 16. Circuit of an Output of the SN74ACT7801FN DUT Board

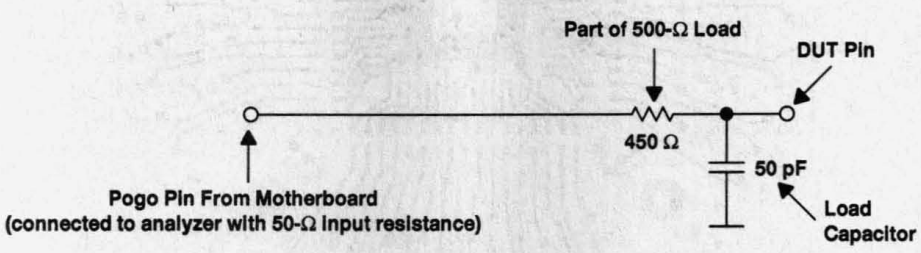


Figure 17. Circuit of an Output of the SN74ACT7801FN DUT Board With a Load Circuit of 500 Ω/50 pF to GND, Assuming a Signal Analyzer With an Input Resistance of 50 Ω

Jumpers, terminating resistors, and the load circuit are as close as possible to the DUT. These passive components are in space-saving surface-mount device (SMD) packages. The jumper is soldered to the topside of the board; the terminating resistor or the load circuit is on the underside (see Figure 18). The complete layout of the topside and underside of the DUT board for the SN74ACT7801FN is shown in Figures 19 and 20.

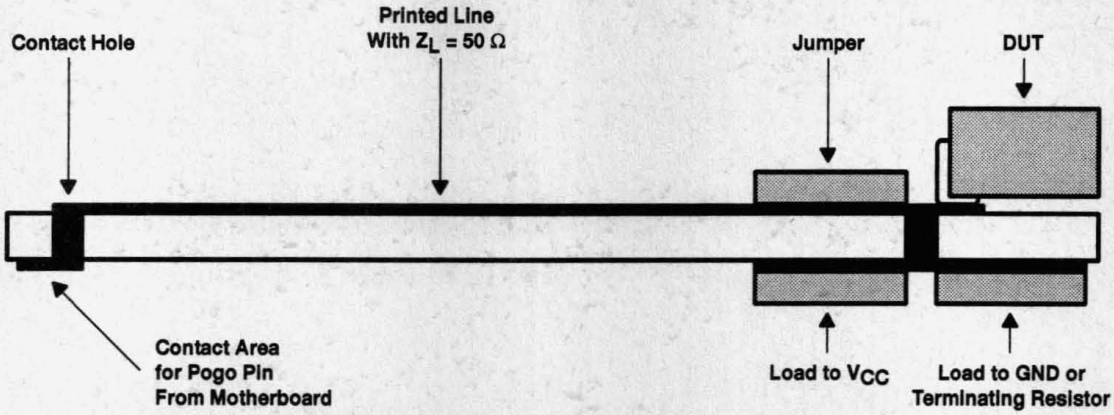


Figure 18. Cross-Section of the SN74ACT7801FN DUT Board, With the Printed Line and the Position of Passive Components for One Input or Output

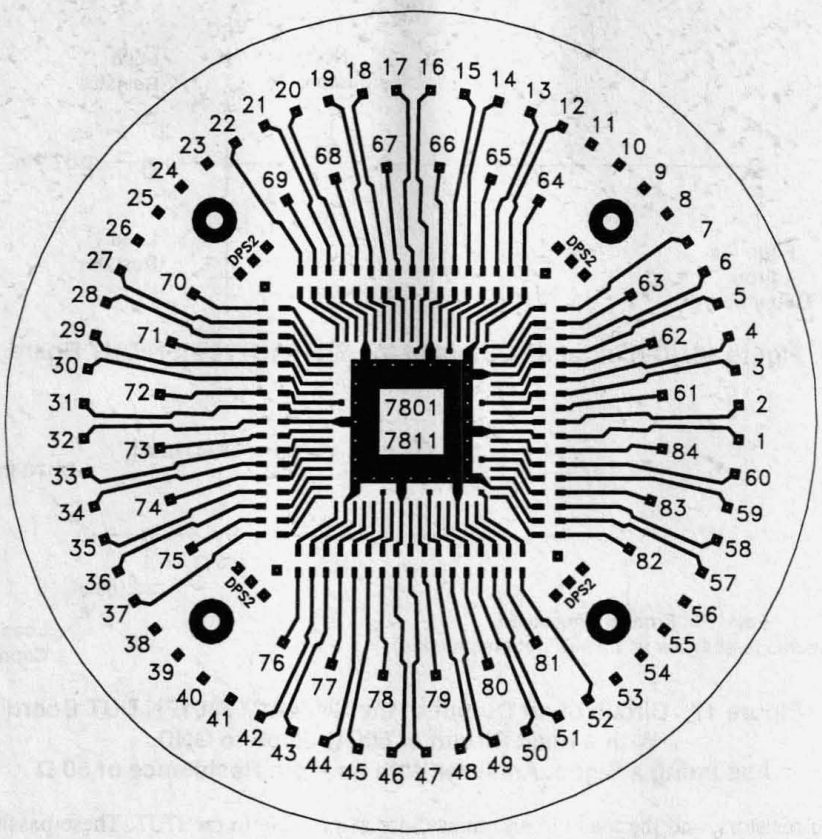


Figure 19. Topside of the ac-Test DUT Board for the FIFO SN74ACT7801FN in 68-Pin PLCC Package

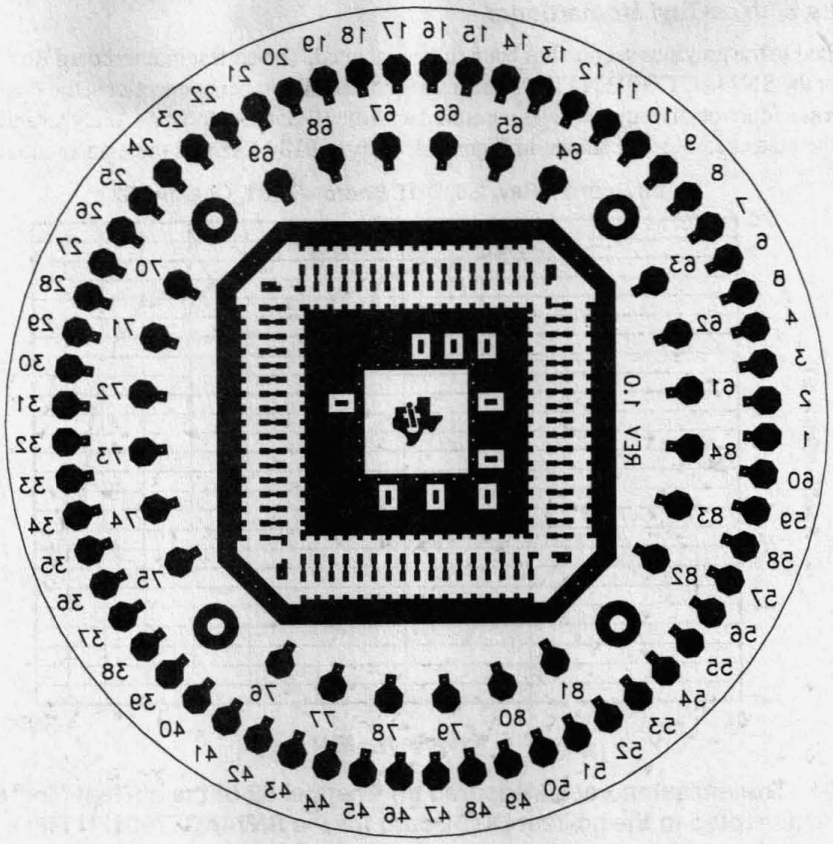


Figure 20. Underside of the ac-Test DUT Board for the FIFO SN74ACT7801FN in 68-Pin PLCC Package

3.5.3 Test Results With ac-Test Motherboard

The test setup described in the previous section has been fully evaluated. The ac-test motherboard Rev. 2.0 was used with the ac-test DUT board for the SN74ACT7801FN FIFO. The tests included all jumper connections, the Pogo pins, and the jumper field. The attenuation as a function of frequency was measured with the HP8505A Network Analyzer and HP8503 S-Parameter Test Set. Results of the measurements are shown in Figure 21. Only at 910 MHz was there an attenuation of 3 dB.

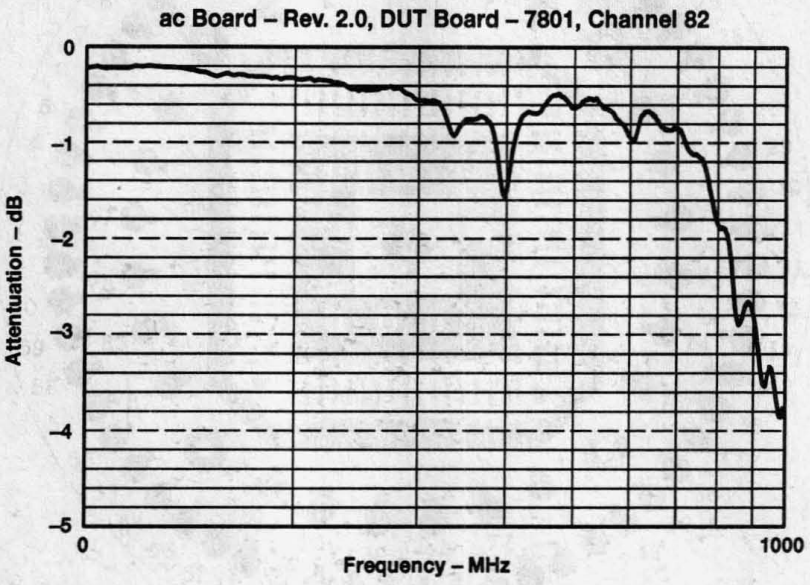


Figure 21. Transmission Loss Measured on Channel 82 of the ac-Test Motherboard Connected to the ac-Test DUT Board for the SN74ACT7801FN FIFO

Measurements with various DUT boards led, in some cases, to considerably lower limiting frequencies, which demonstrates that the DUT board must also be constructed with great care if precise measurement results are desired.

4 Summary

When evaluating the timing behavior of circuits that produce very steep pulse edges, an appropriate test setup is essential to achieve reliable, repeatable, and comparable test results. A good test setup has these characteristics:

- Each supply voltage and the ground connection should have separate layers on the circuit board. This ensures a stable voltage supply that will not change, even when there are high-frequency current fluctuations.
- The wiring on the test boards must have a defined characteristic impedance, normally 50 Ω, and be terminated with a series or a load resistor. This provides undistorted signals free from overshoot, undershoot, and without steps on the pulse edges to the input of the device under test.
- There must be no stub lines at the output, otherwise reflections will be generated. For this reason, the load circuit must be as close as possible to the device under test.
- Test equipment must be suitable for measurements to be made and its influence on the complete test setup recognized.

If these requirements are met, accurate and orderly measurements can be made.

Acknowledgment

The author of this document is Peter Forstner.

Appendix A

ac-Performance Board Documentation

A-1 Introduction

The construction, operation, and typical applications of the ac-performance board are presented in this appendix. The ac-performance board has the following features:

- The contacts of the device-under-test (DUT) are compatible with industrial-standard 84-pin DUT boards.
- It is possible to switch the input to up to 80 pins.
- Three separate dc-voltage connection options are available.
- Suitable for measuring characteristic curves
- Suitable for simultaneous-switching applications
- Suitable for all common ac measurements

A-2 Specifications

A-2.1 Mechanical Dimensions

Performance board

Length :	300 mm
Width :	300 mm
Thickness :	3.0 mm

DUT board

Diameter :	110 mm
Thickness :	3.0 mm

A-2.2 Electrical Characteristics

Performance board

Capacitance between signal and ground level :	300 mm
Impedance of signal line :	300 mm
Difference of delay times between signal lines without DUT board :	3.0 mm

DUT board

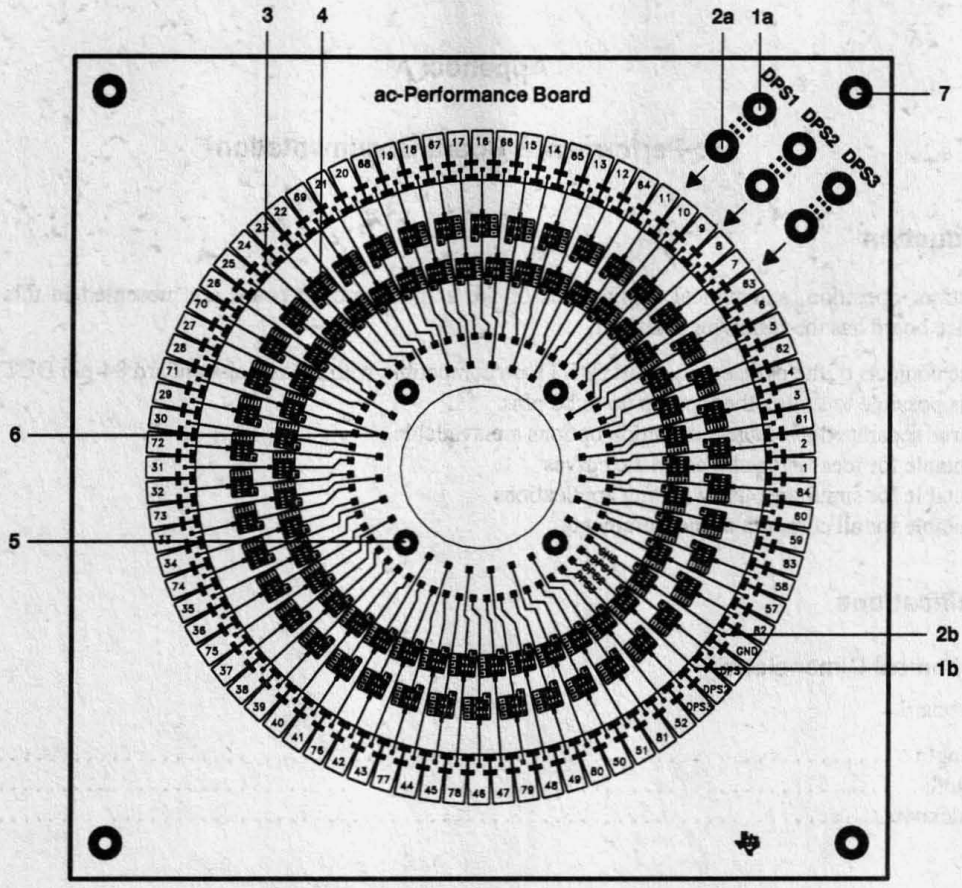
Impedance of signal line :	300 mm

A-2.3 Temperature Range

Temperature range :	–40°C to 110°C

A-3 Description of Operation

A-3.1 ac-Performance Board



1a, 1b	Separate dc-voltage connections (DPS1, DPS2, DPS3)
2a, 2b	Ground connection options (3)
3	Signal connectors (SMB)
4	Jumper matrix (detailed information in paragraph A-3.2)
5	Screw and grounding connection to the DUT board
6	Signal connections to DUT boards via Pogo pins
7	Holes for spacers (4)

Figure A-1. ac-Performance Board

A-3.2 Jumper Matrix

The jumper matrix allows connecting various dc voltages (DSP1, DSP2, DSP3) or GND, via gold bridges, to each signal pin. A connection between the SMB contact and the Pogo pin can be made with a gold bridge in the signal path.

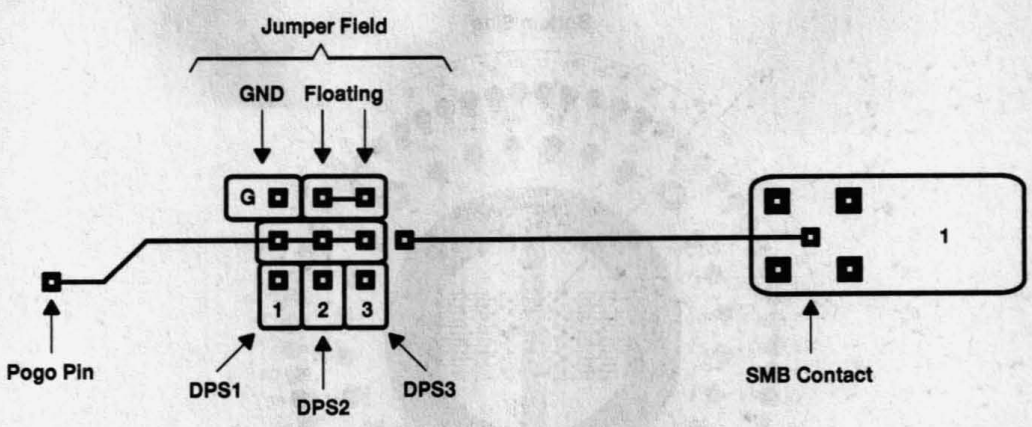
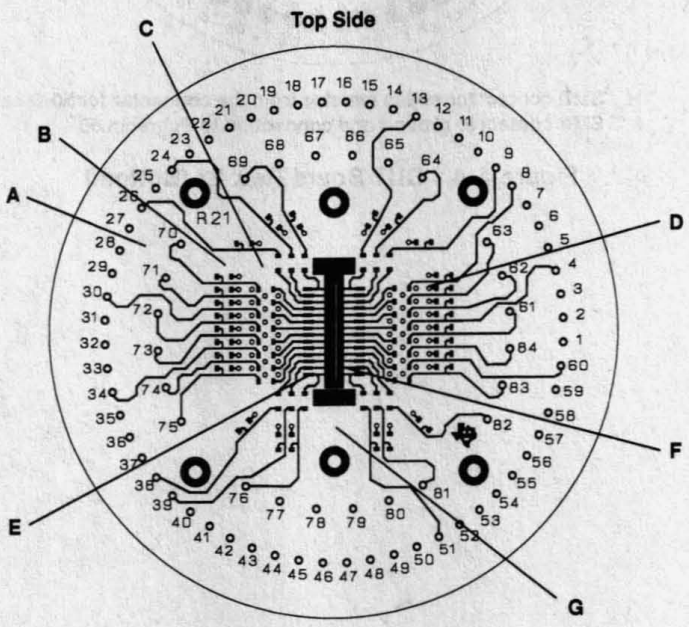
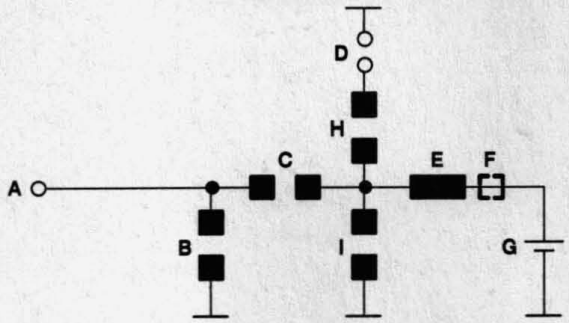


Figure A-2. Jumper Matrix

A-3.3 DUT Board Rev. 21 for 24-/28-Pin SO Package

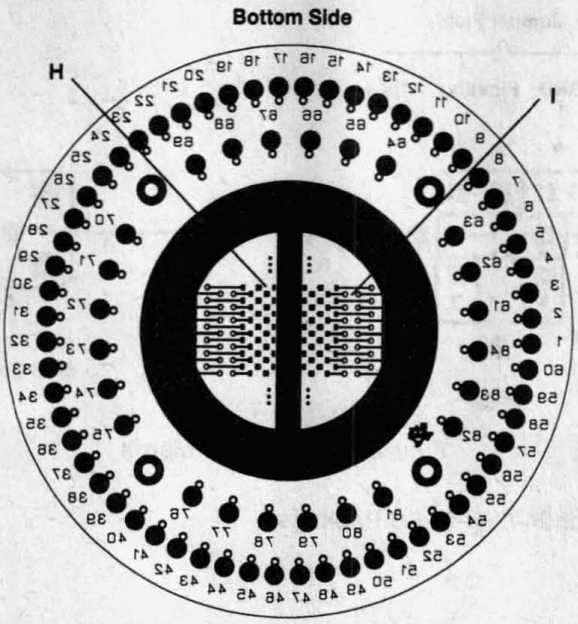


Layout of Each Channel



- A Connection to Pogo pin
- B SMD contact to ground and connection to Pogo pin 56
- C SMD contact for input bridges
- D Connection for 50-Ω cable
- E IC pin contact area
- F Optional point to isolate the IC from V_{CC}
- G V_{CC} connection to Pogo pin 56
- H SMD contact for series resistor from the connector for 50-Ω cable
- I SMD contact to ground and connection to Pogo pin 56

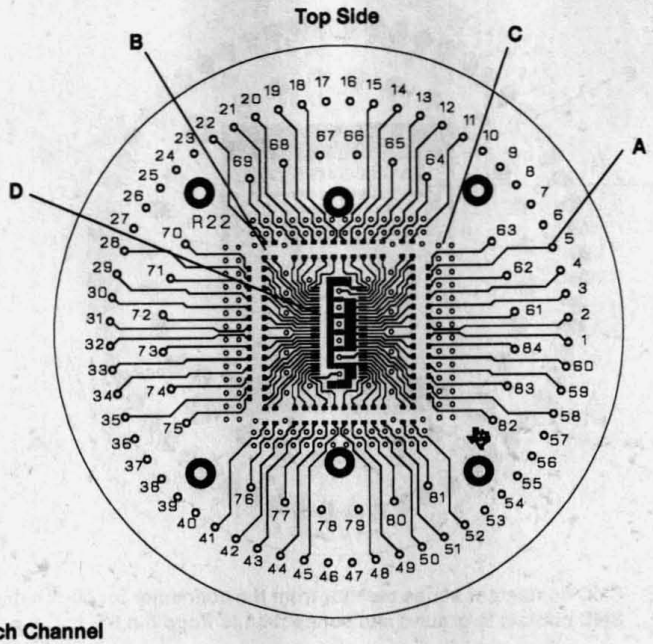
Figure A-3. DUT Board Rev. 21 (Top)



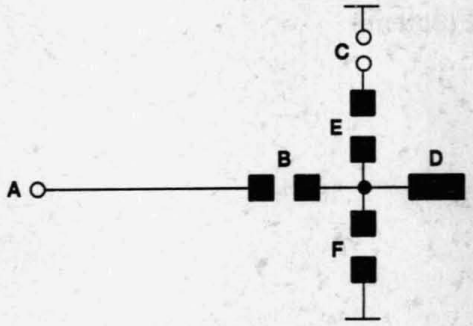
H SMD contact for series resistor from the connector for 50-Ω cable
I SMD contact to ground and connection to Pogo pin 56

Figure A-4. DUT Board Rev. 21 (Bottom)

A-3.4 DUT Board Rev. 22 for 56-Pin SSO Package

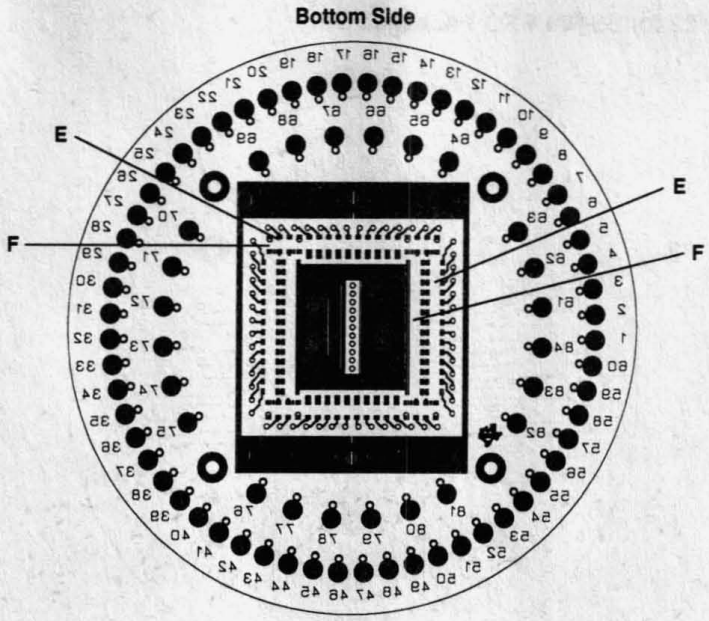


Layout of Each Channel



A Connection to Pogo pin
B SMD contact for input bridge
C Connection for 50-Ω cable
D IC pin contact area
E SMD contact for series resistor from the connector for 50-Ω cable
F SMD contact to ground and connection to Pogo pin 56

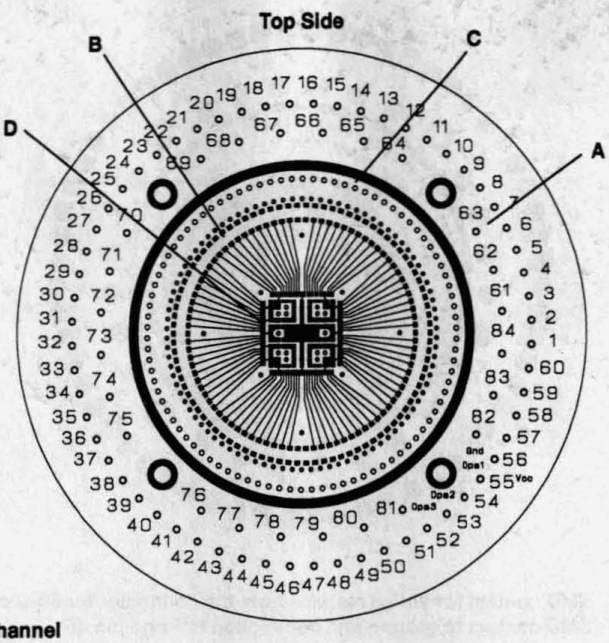
Figure A-5. DUT Board Rev. 22 (Top)



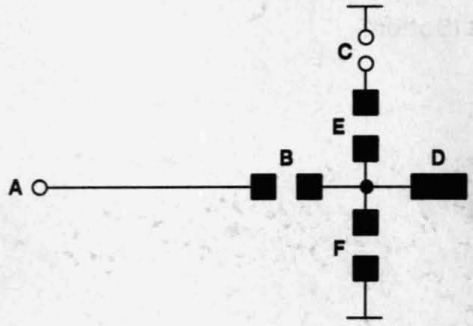
E SMD contact for series resistor from the connector for 50-Ω cable
F SMD contact to ground and connection to Pogo pin 56

Figure A-6. DUT Board Rev. 22 (Bottom)

A-3.5 DUT Board Rev. 23 for 100-Pin SQF Package

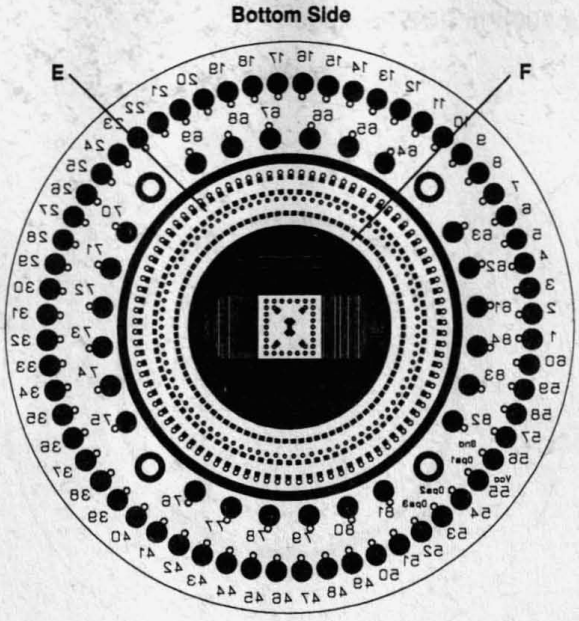


Layout of Each Channel



A Connection to Pogo pin
B SMD contact for input bridge
C Connection for 50-Ω cable
D IC pin contact area
E SMD contact for series resistor from the connector for 50-Ω cable
F SMD contact to ground and connection to Pogo pin 56

Figure A-7. DUT Board Rev. 23 (Top)



E SMD contact for series resistor from the connector for 50-Ω cable
F SMD contact to ground and connection to Pogo pin 56

Figure A-8. DUT Board Rev. 23 (Bottom)

A-4 Description of Applications

A-4.1 Measuring Transit Time

The oscilloscope inputs have an impedance of 50 Ω. The effective load capacitance includes the specific load capacitance at the output plus the board capacitance.

All connections from generator to board, generator to oscilloscope, and oscilloscope to board are made with 50-Ω cable.

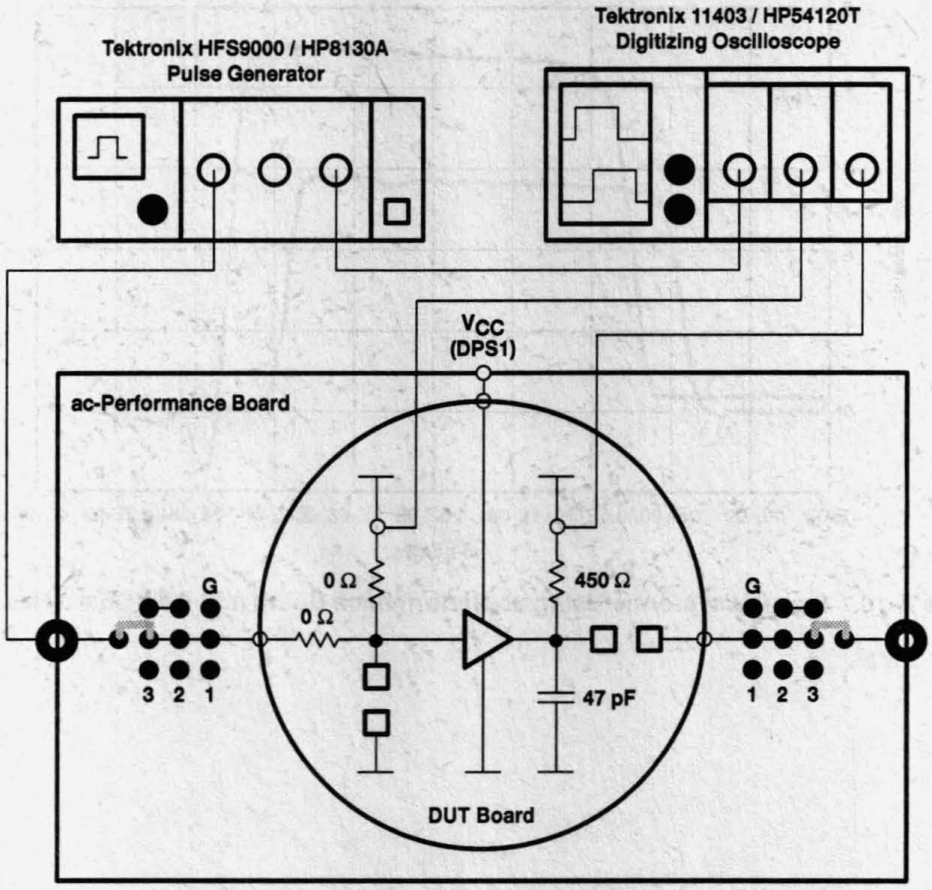


Figure A-9. Transit-Time Measurement Setup

A-5 Description of Signals

A-5.1 Signal Waveforms

The curves in Figure A-10 have been measured with the test setup described in paragraph A-4.1 Measuring Transit Time.

The device under test is a ABT32501, soldered on the DUT board Rev. 23. The ABT32501 has been configured to measure the propagation delay time (t_{PHL}/t_{PLH}) of one driver (1A1 to 1B1).

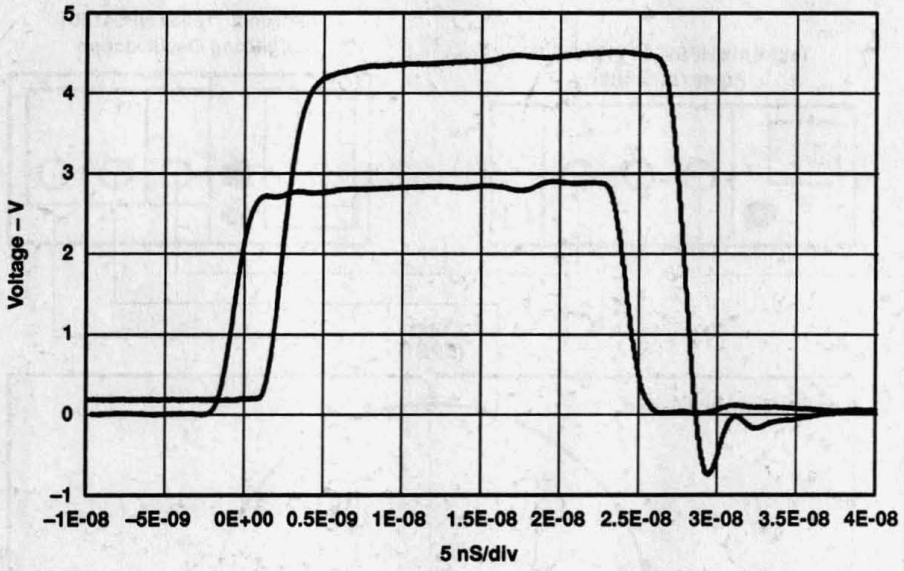


Figure A-10. Signal Waveforms Using ac-Performance Board and DUT Board Rev. 23

A-5.2 Description of the Transmission-Loss Measurement

Measured values were determined using the HP8505A Network Analyzer and the HP8503 S-Parameter Test Set (see Figure A-11). As the test setup shows, the measurement has been made using one channel of the ac-performance board in conjunction with the DUT board Rev. 23 and a combination of two channels. Here it was important to include the complete lines of the DUT board of each channel.

Results of the transmission-loss measurement are shown graphically in paragraph A-5.3.

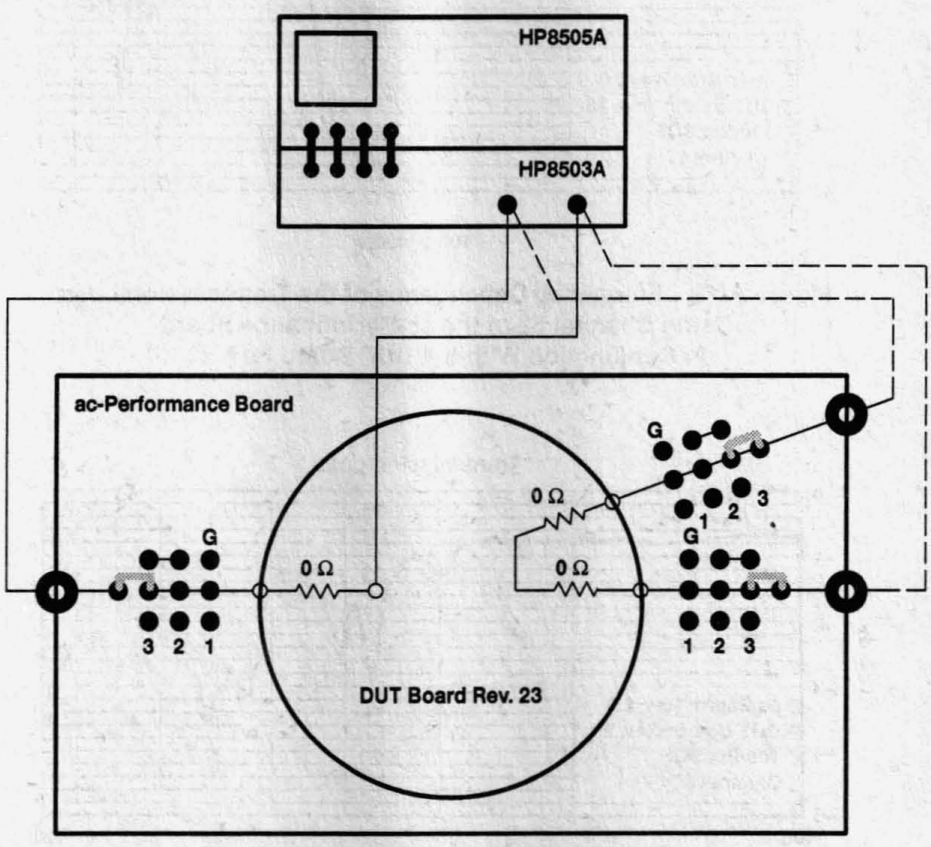


Figure A-11. Principal Test Setup for Transmission-Loss Measurement

A-5.3 Results of the Transmission-Loss Measurement

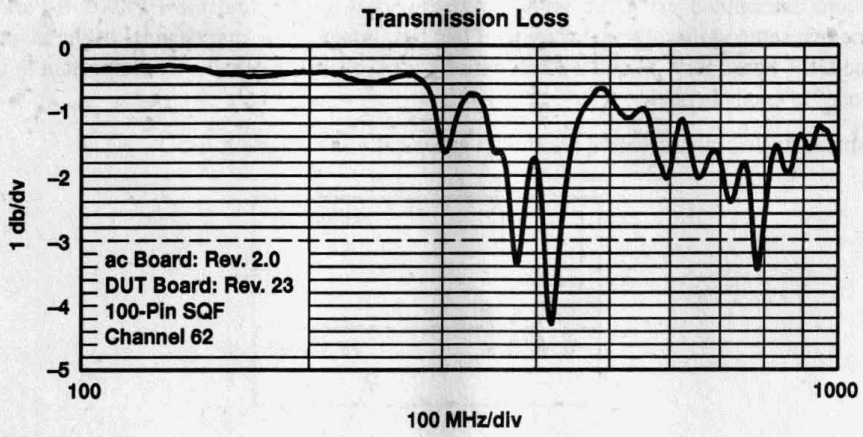


Figure A-12. Frequency Dependency of the Transmission Loss Using Channel 62 of the ac-Performance Board in Conjunction With the DUT Board Rev. 23

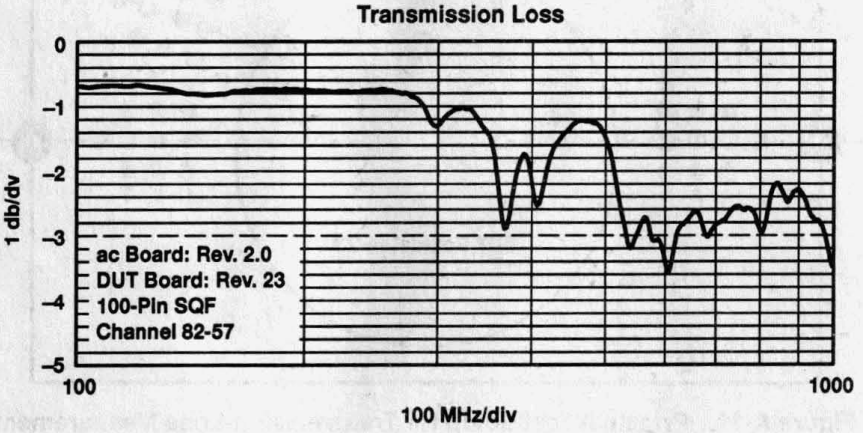


Figure A-13. Frequency Dependency of the Transmission Loss Using Channel 82-57 of the ac-Performance Board in Conjunction With the DUT Board Rev. 23

A-5.4 Description of the TDR Measurement

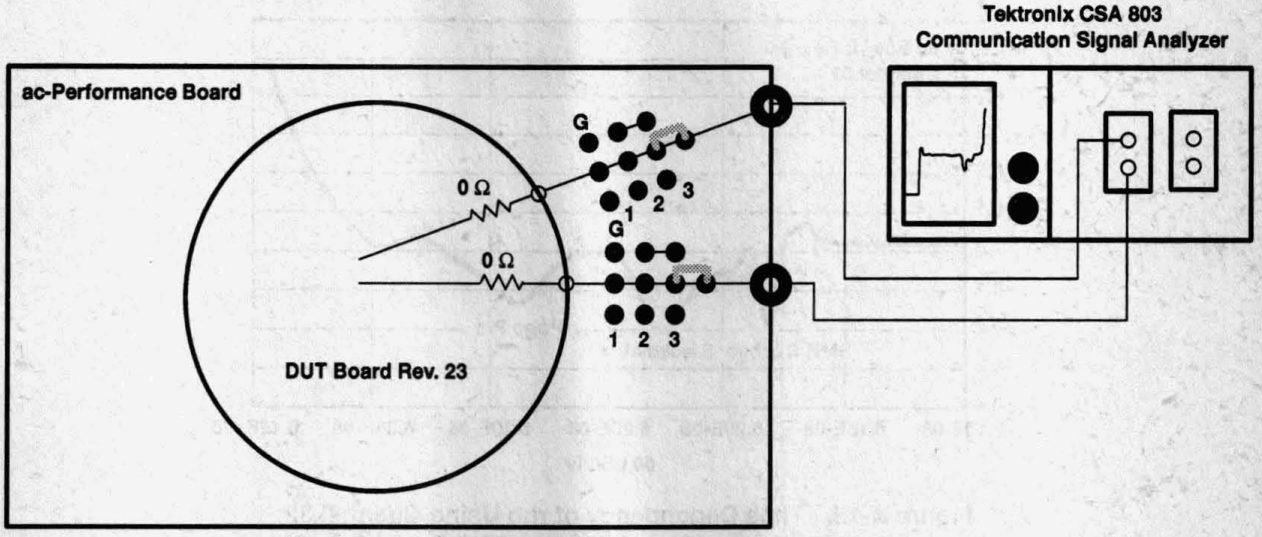


Figure A-14. Principal Test Setup for the TDR Measurement

The measurement was made using a Tektronix CSA 803 Communication Signal Analyzer with a special Sampling Head (SD-24, 20 GHz). To make this measurement, a voltage slope with defined amplitude must be applied to the test line. Analyzing the waveform at the signal source leads to the impedance and the delay time of the line. The CSA 803 makes the calculation and shows the impedance and the delay time directly. A signal generator with a defined resistance (R_i = 50 Ω) is integrated in the sampling head. It generates an amplitude of U = 500 mV with a rise time of about 25 ps. A second internal generator is available in the sampling head.

Because both generators can be driven in push-pull, the basic line dimension (Z_{Lodd}) of two symmetrical cross-coupled lines can be determined.

Paragraph A-5.5 shows, in the first figure, the time dependency of rho (ρ) for a single line. The result of two symmetrical cross-coupled lines is shown in the second figure.

The formula for the calculation of the impedance is:

$$Z_L = Z_o \frac{1 + \rho}{1 - \rho} \qquad (1)$$

A-5.5 Result of the TDR Measurement

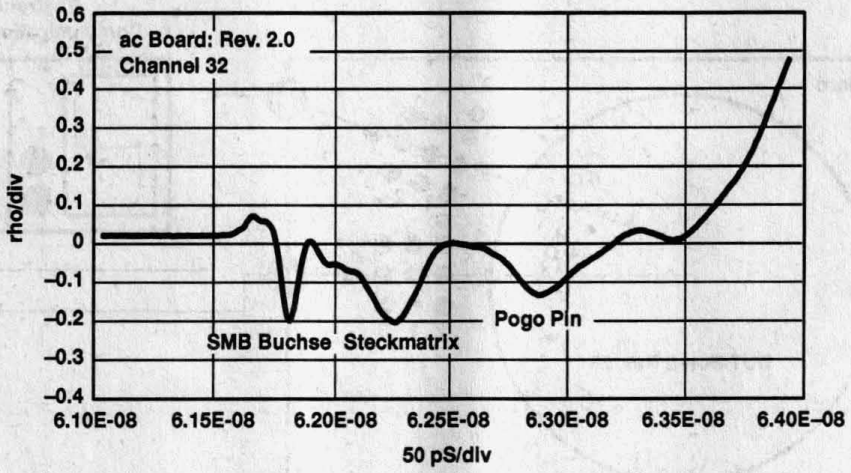


Figure A-15. Time Dependency of rho Using Channel 32 on the ac-Performance Board With the DUT Board Rev. 23

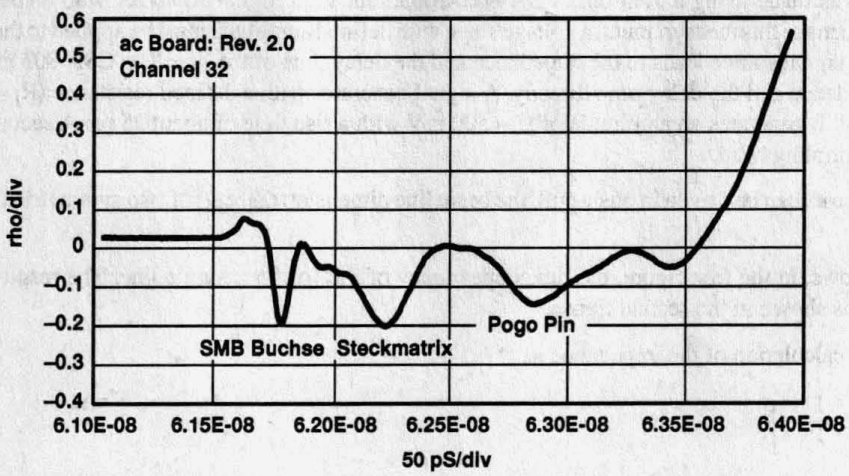


Figure A-16. Time Dependency of rho Using Channel 32 With the Symmetrical Cross-Coupled Channel 73 (in Push-Pull) on the ac-Performance Board With the DUT Board Rev. 23

A-6 Parts List

DESCRIPTION	SUPPLIER	PART NUMBER	QUANTITY
ac Board Rev. 2.0	Texas Instruments	AC-Board 2.0	1
Inset nuts Ø4.5	Bürklin	16H600	4
Sockets, black	Bürklin	25F220	3
Sockets, red	Bürklin	25F230	3
Hex posts M5	Bürklin	18H236	4
Hex nuts M5	Bürklin	16H7906	4
Washers Ø5.3	Bürklin	16H864	8
SMB plug	Bürklin	77F210	84
SMC plug	Suhner	82SMC-50-0-1	84
Sub mini sockets Ø1.0	Infratron	H3153-05	756
Pogo pins	Feinmetall	FM670/15	84
Sleeves	Feinmetall	FM6010-10 S003	84

Addresses of suppliers:

Hans Bürklin
Schillerstr. 40
D–80336 München

Feinmetall
Zeppelinstr. 2
D–71083 Herrenberg

Infratron
Am Schnepfenweg 34
D–80995 München

Suhner Elektronik GmbH
Mehlbeerenstr. 6
D–82024 Taufkirchen

Acknowledgment

The author of this appendix is Claus Kuch.

Designing With the SN54/74LS123

SDLA006A
March 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**3–131**
Features	**3–131**
Rules for Operation	**3–132**
Output Pulse Duration	3–133
Output Pulse Duration Versus Supply Voltage	3–134
Special Considerations	**3–135**
Device-to-Device Variation	3–137
74LS123N/J Device-to-Device Variation	3–138
Applications	**3–140**
Delayed-Pulse Generator With Override	3–140
Missing-Pulse Detector	3–141
Low-Power Pulse Generator	3–142
Negative/Positive Edge-Triggered One-Shot	3–143
Pulse-Duration Detector	3–144
Frequency Discriminator	3–145

List of Illustrations

Figure	*Title*	*Page*
1	'LS123 Logic Diagram	3–131
2	Remote Trimming Circuit	3–132
3	Retrigger Pulse-Duration Calculation	3–132
4	Multiplier Factor Versus External Capacitor (C_{ext})	3–133
5	Output Pulse Duration Versus External Timing Capacitance	3–134
6	Output Pulse Duration Versus Supply Voltage	3–134
7	Average Percent Change Versus Pulse-Duration Tolerance	3–135
8	Pulse-Duration Variation Versus Supply Voltage	3–136
9	Pulse-Duration Variation Versus Free-Air Temperature	3–136
10	Multiplier Factor Versus Capacitance	3–137
11	Delayed-Pulse Generator With Override	3–140
12	Missing-Pulse Detector	3–141
13	Low-Power Pulse Generator	3–142
14	Negative/Positive Edge-Triggered One-Shot	3–143
15	Pulse-Duration Detector	3–144
16	Frequency-Discriminator Circuit	3–145
17	'LS123 Schematic	3–146

Introduction

The Texas Instruments (TI) SN54/74LS123 dual retriggerable monostable multivibrator is a one-shot device capable of very long output pulses and up to 100% duty cycle. The 'LS123 also features dc triggering from gated low-level active A and high-level active B inputs and provides a clear input that terminates the output pulse of any predetermined time independent of timing components, R_{ext} and C_{ext}. The output pulse duration can also be extended by retriggering the input prior to the termination of an existing output pulse. Retrigger pulses starting before 0.22 C_{ext} (in pF) ns after the initial trigger pulse will be ignored and the output duration will remain unchanged.

The B input on an 'LS123 is designed to handle pulses with a transition rate as slow as 0.1 mV/ns, (Schmitt-trigger input) with jitter-free one-shot action. This capability allows the 'LS123 to be used as an interface element between circuits with very slow-rising output pulses and circuits that require fast-rising input pulses.

Features

- 100% maximum duty cycle
- Dc triggered from active-high or active-low logic inputs
- Input clamp diodes
- Low power dissipation
- Compensated for V_{CC} and temperature variations

Figure 1 is a functional block diagram of the 'LS123. Each one-shot has two inputs, one active-low and one active-high, which allow both leading or trailing edge triggering. When triggered, the basic pulse duration can be extended by retriggering the gated low-level active A or high-level active B inputs, or the pulse duration can be reduced by use of the overriding clear. Therefore, an input cycle time shorter than the output cycle time will retrigger the 'LS123 and result in a continuously high Q output.

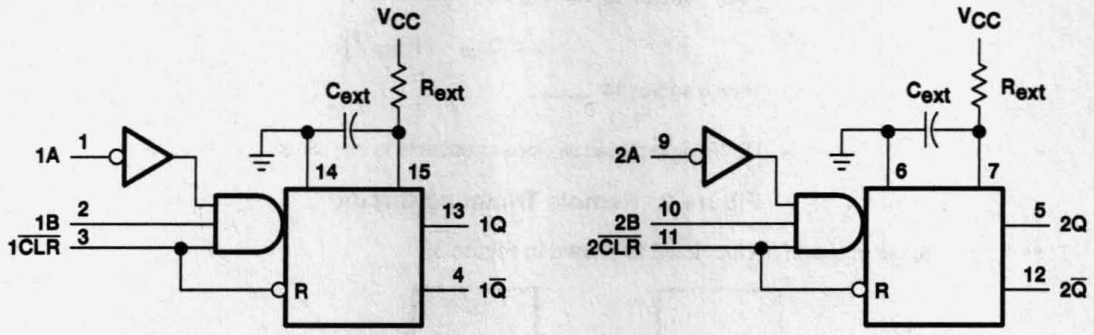


Figure 1. 'LS123 Logic Diagram

FUNCTION TABLE

CLEAR	A INPUT	B INPUT	Q	$\overline{Q}$
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑	LHL‡	HLH§
H	↓	H	LHL‡	HLH§
↑	L	H	LHL‡	HLH§

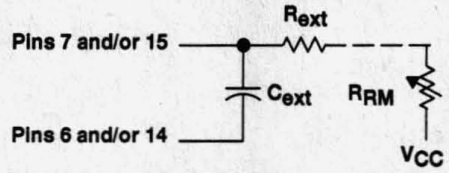
† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the setup.
‡ This is a low-to-high-to-low pulse.
§ This is a high-to-low-to-high pulse.

Rules for Operation

1. An external resistor (R_{ext}) and an external capacitor (C_{ext}) are required, as shown in Figure 1, for proper circuit operation.

NOTE:
For best results, system ground should be applied to the C_{ext} terminals.

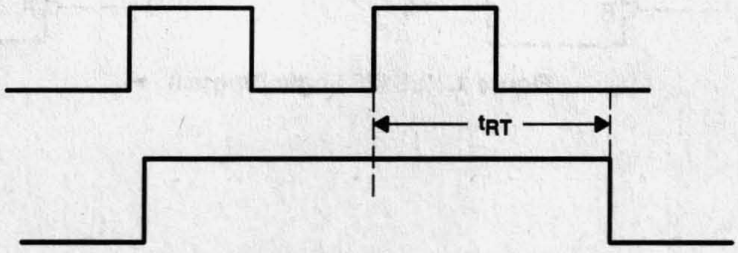
2. This value of R_{ext} may vary from 5 kΩ to 180 kΩ between –55°C and 125°C.
3. C_{ext} may vary from 0 pF to any necessary value.
4. The input may have a minimum amplitude of –0.5 V and a maximum of 5.5 V.
5. When an electrolytic capacitor is used as C_{ext}, the switching diode required by most one-shots is *not needed* for 'LS123 operation.
6. For remote trimming, the circuit shown in Figure 2 is recommended.



NOTE: R_{RM} is placed as close as possible to the 'LS123.

Figure 2. Remote Trimming Circuit

7. The retrigger pulse duration is calculated as shown in Figure 3.



$$t_{RT} = t_W + t_{PLH} = K \bullet R_{ext} \bullet C_{ext} + t_{PHL}$$

Figure 3. Retrigger Pulse-Duration Calculation

8. A 0.001-μF to 0.1-μF bypass capacitor between V_{CC} and GND as close as possible to the 'LS123 is recommended (see Figure 4).

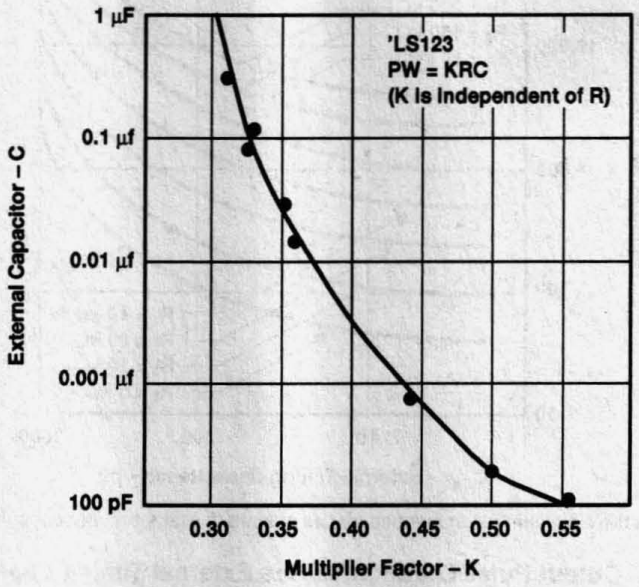


Figure 4. Multiplier Factor Versus External Capacitor (C_{ext})

Output Pulse Duration

The basic output pulse duration is essentially determined by the values of external capacitance and timing resistance. For pulse durations when C_{ext} is < 1 μF, use the following formula:

$$t_w = K \cdot R_t \cdot C_{ext} \text{ (also see Figure 5)} \quad (1)$$

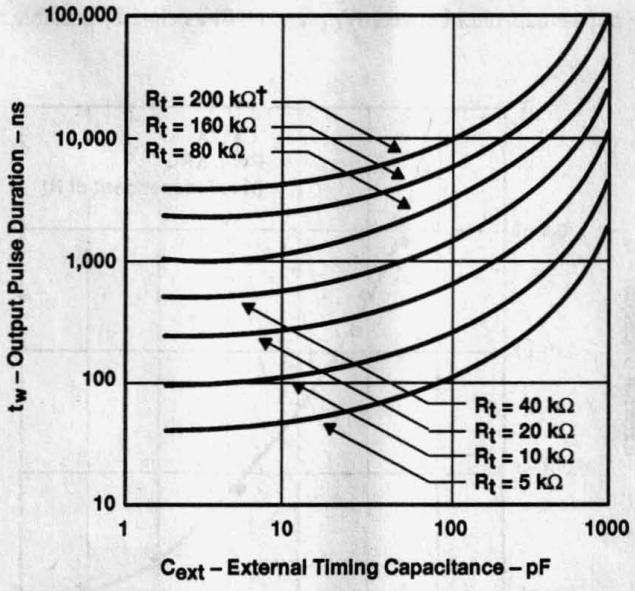
When C_{ext} is > 1 μF, the output pulse duration is defined as:

$$t_w = 0.33 \cdot R_t \cdot C_{ext} \quad (2)$$

Where, for the two previous equations, as applicable:

K = multiplier factor
R_t = given in kΩ (Internal or External Timing Resistance)
C_{ext} = in pF
t_w = in ns

For capacitor values of less than 1000 pF, the typical curves in Figure 5 can be used.



† This value of resistance exceeds the maximum recommended for use over the full temperature range of the SN54LS circuits.

Figure 5. Output Pulse Duration Versus External Timing Capacitance

Output Pulse Duration Versus Supply Voltage

Figure 6 shows the relationship between the output pulse duration and V_{CC} at specific temperatures.

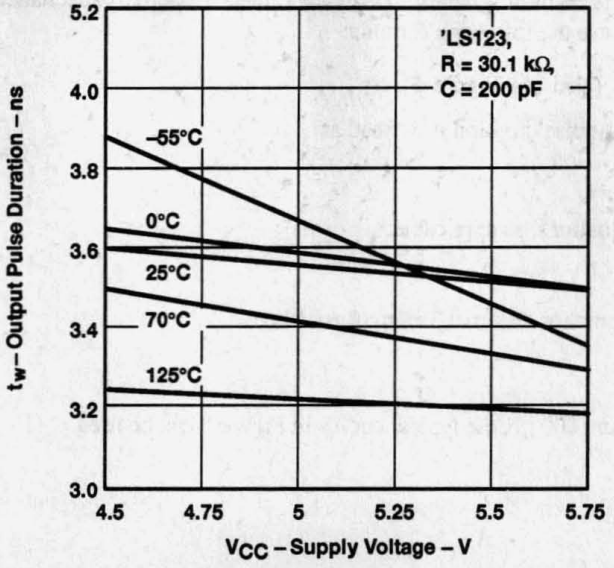


Figure 6. Output Pulse Duration Versus Supply Voltage

Special Considerations

Because these monostable multivibrators are half analog and half digital, they inherently are more sensitive to noise on the analog portion (timing leads) than standard digital circuits. They should not be located near noise-producing souces or transient-carrying conductors and liberal power-supply bypassing is recommended for greater reliability and repeatibility. Also, a monostable should not be used as a fix for asynchronous systems; synchronous design techniques always provide better performance. For time delays over 1.5 s or timing capacitors over 100 µF, it is usually better to use a free-running astable multivibrator and a couple of inexpensive decade counters (such as a 7490A) to generate the equivalent of a long-delay one-shot. Astable oscillators made with monostable building blocks have stabilities approaching five parts in 100 and should not be used if system timing is critical. Crystal oscillators provide better stability.

In all one-shot applications, follow these guidelines:

- Use good high-frequency 0.1-µF (ceramic disk) capacitors, located 1 to 2 inches from the monostable package, to bypass V_{CC} to ground.
- Keep timing components (R_t, C_t) close to the package and away from high transient voltage or current-carrying conductors.
- Keep the Q-output trace away from the $\overline{CLR}$ lead; the negative-going edge when the one-shot times out may cause the C lead to be pulled down, which may restart the cycle. If this happens, constantly high (Q = H, $\overline{Q}$ = L) outputs with 50-ns low spikes will occur at the repetition rate determined by R_t and C_t. If sufficient trace isolation cannot be obtained, a 50-pF capacitor bypassing the C lead to ground usually eliminates the problem.
- Beware of using the diode or transistor protective arrangement when retriggerable operation is required; the second output pulse may be shorter due to excess charge left on the capacitor. This may result in early time out and apparent failure of retriggerable operation. Use a good capacitor, one that is able to withstand 1 V in reverse and meet the leakage current requirements of the particular one-shot.
- Remember that the timing equation associated with each device has a prediction accuracy. Generally, for applications requiring better than ±10% accuracy, trimming to pulse duration is necessary.

Variations in performance versus applicable parameters are shown in Figures 7 through 10.

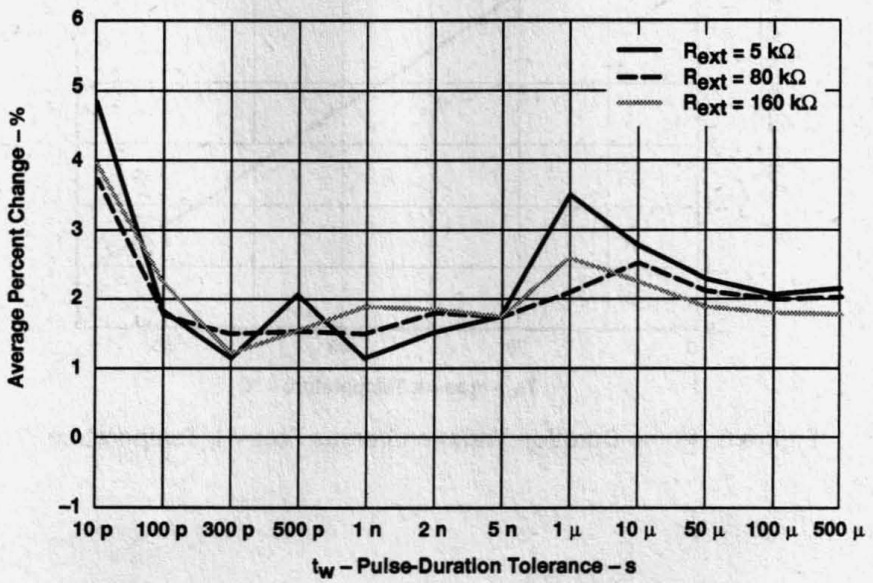


Figure 7. Average Percent Change Versus Pulse-Duration Tolerance

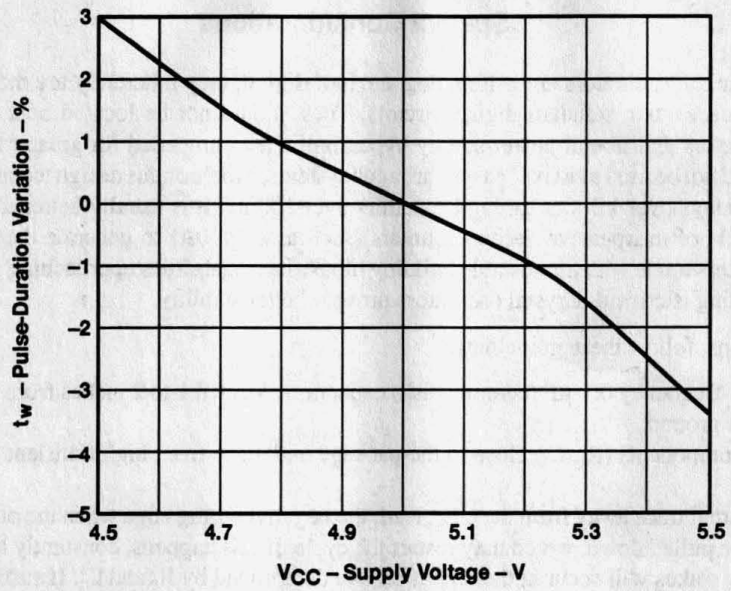


Figure 8. Pulse-Duration Variation Versus Supply Voltage

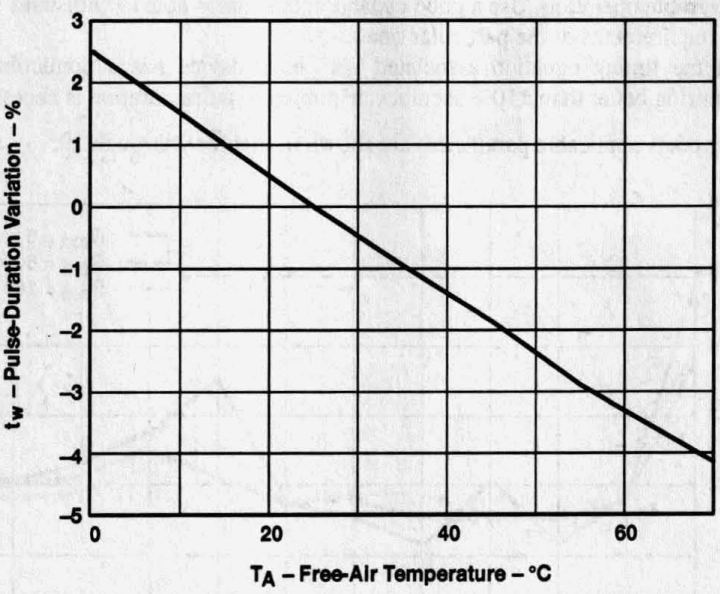


Figure 9. Pulse-Duration Variation Versus Free-Air Temperature

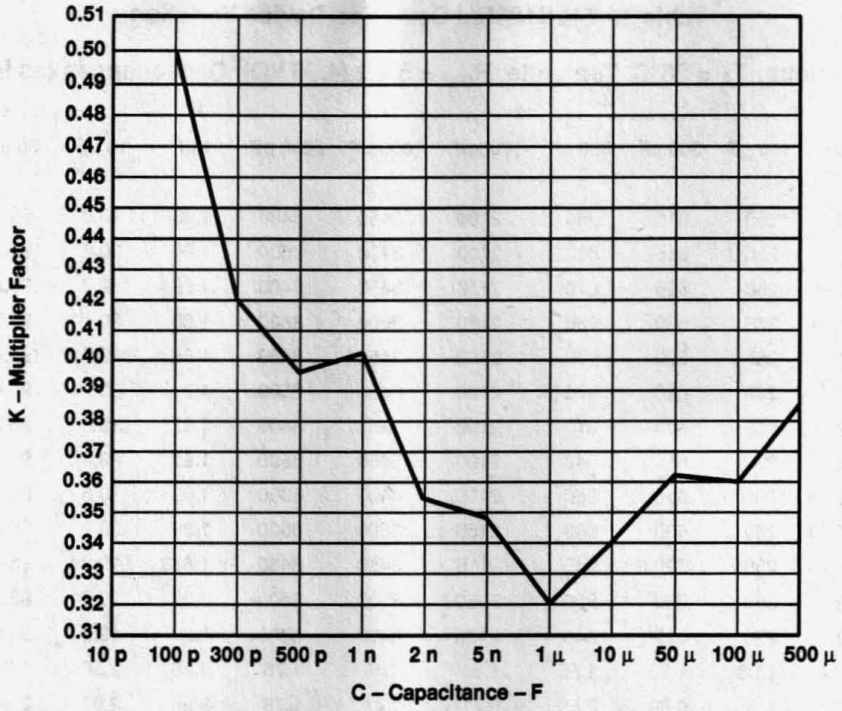


Figure 10. Multiplier Factor Versus Capacitance

Device-to-Device Variation

Device-to-device variation is always a concern with designers when using a part such as the 'LS123. The data in Table 1 were taken in the laboratory using three external-resistor (R_{ext}) values. Ten devices were tested, using three different date codes, and using 12 different external capacitor (C_{ext}) values. Each column was averaged and that number considered a target value, and the high and low values considered the + and – percentage change from that value. These results indicate that the average percentage change from the target value probably should not exceed ±5%. This should not, however, be interpreted as an ensured parameter. This parameter is not tested by TI.

Table 1. 74LS123N/J Device-to-Device Variation

Example 1. Conditions: T_A = 25°C, Ten units, R_{ext} = 5 kΩ (4.96 kΩ), Capacitances (as listed)

	ns							X				ms
C_{ext} UNIT	10 pF	100 pF	300 pF	500 pF	1000 pF	2000 pF	5000 pF	1 µF	10 µF	50 µF	100 µF	500 µF
1.	80	250	615	960	2100	3450	8400	1.88	19.8	95.4	213	851
2.	83	255	615	960	2100	3400	8500	1.94	20.2	97.2	217	866
3.	84	255	625	970	2150	3450	8400	1.86	19.7	95.2	213	848
4.	88	260	630	980	2150	3500	8600	1.88	20	96.6	216	860
5.	88	255	620	970	2100	3450	8400	1.88	19.9	95.8	214	853
6.	86	260	620	970	2100	3450	8500	1.9	20	96.4	215	856
7.	82	255	620	970	2100	3450	8400	1.87	19.6	95.2	213	850
8.	83	260	615	940	2100	3450	8500	1.95	20.4	97.7	218	867
9.	82	250	615	960	2100	3400	8300	1.82	19.3	93.2	209	830
10.	87	260	630	980	2150	3500	8500	1.89	20	96.5	216	859
AVG	83.7	255	620.5	965	2115	3450	8450	1.888	19.89	95.92	214.4	854
MAX	88	260	630	980	2150	3500	8600	1.95	20.4	97.7	218	867
MIN	80	250	615	940	2100	3400	8300	1.82	19.3	93.2	209	830
%CHG+	5.14	1.96	1.53	1.55	1.65	1.45	1.78	3.28	2.56	1.86	1.68	1.52
%CHG–	4.12	1.96	0.89	2.59	0.71	1.45	1.78	3.60	2.97	2.84	2.25	2.81

Example 2. Conditions: T_A = 25°C, Ten units, R_{ext} = 80 kΩ (80.2 kΩ), Capacitances (as listed)

	µs				X			ms		X	s	X
C_{ext} UNIT	10 pF	100 pF	300 pF	500 pF	1000 pF	2000 pF	5000 pF	1 µF	10 µF	50 µF	100 µF	500 µF
1.	0.91	3.9	10	16	33.5	53.5	140	34	325	1.61	3.54	14.7
2.	0.92	3.9	10	16	33.5	58.5	141	35	334	1.64	3.59	14.9
3.	0.9	3.9	10.1	16.2	34	59	141	34	329	1.62	3.56	14.8
4.	0.94	3.95	10.3	16.4	34.5	60	143	34.5	334	1.64	3.61	15
5.	0.89	3.9	10	16.1	34	58.5	141	34.5	331	1.62	3.57	14.8
6.	0.915	3.9	10.1	16.2	34	59	142	34.5	333	1.63	3.59	14.9
7.	0.92	3.9	10.1	16.2	34	58.5	140	34	328	1.61	3.54	14.7
8.	0.91	3.9	10	15.9	33.5	58.5	141	35	328	1.65	3.62	15
9.	0.87	3.8	10	15.9	33.5	58	138	33.5	322	1.58	3.48	14.4
10.	0.91	3.9	10.2	16.3	34.5	59.5	143	34.5	334	1.64	3.61	15
AVG	0.9085	3.895	10.08	16.12	33.9	58.8	141	34.35	331.1	1.624	3.571	14.82
MAX	0.94	3.95	10.3	16.4	34.5	60	143	35	338	1.65	3.62	15
MIN	0.87	3.8	10	15.9	33.5	58	138	33.5	322	1.58	3.48	14.4
%CHG+	3.47	1.41	2.18	1.74	1.77	2.04	1.42	1.89	2.08	1.60	1.37	1.21
%CHG–	4.24	2.44	0.79	1.36	1.18	1.36	2.13	2.47	2.75	2.71	2.55	2.83

Table 1. 74LS123N/J Device-to-Device Variation (Continued)

Example 3. Conditions: T_A = 25°C, Ten units, R_{ext} = 160 kΩ (159.7 kΩ), Capacitances (as listed)

	µs							X ms X			s	X
C_{ext} UNIT	10 pF	100 pF	300 pF	500 pF	1000 pF	2000 pF	5000 pF	1 µF	10 µF	50 µF	100 µF	500 µF
1.	1.79	7.8	20	32	67	117	280	68.9	658	3.23	7.1	29.6
2.	1.8	7.8	20	32	67	118	280	70.5	672	3.29	7.21	30
3.	1.78	7.8	20	32.5	68	119	280	69.5	662	3.25	7.16	29.8
4.	1.85	7.9	20.5	33	69	120	285	70.4	672	3.3	7.26	30.2
5.	1.76	7.75	20	32	67.5	118	285	70	667	3.27	7.17	29.9
6.	1.8	7.8	20	32.5	68	119	285	70.4	670	3.28	7.21	30.1
7.	1.8	7.85	20	32.5	67.5	118	280	68.9	658	3.23	7.12	29.6
8.	1.79	7.8	20	32	66.5	118	285	71.5	678	3.31	7.26	30.2
9.	1.71	7.55	20	32	66.5	116	275	67.9	648	3.19	7	29.2
10.	1.78	7.8	20.5	33	68.5	120	285	70.5	672	3.3	7.26	30.2
AVG	1.786	7.785	20.1	32.35	67.55	118.3	282	69.86	665.7	3.265	7.175	29.88
MAX	1.85	7.9	20.5	33	69	120	285	71.5	678	3.31	7.26	30.2
MIN	1.71	7.55	20	32	66.5	116	275	67.9	648	3.19	7	29.2
%CHG+	3.58	1.48	1.99	2.01	2.15	1.44	1.06	2.35	1.85	1.38	1.18	1.07
%CHG–	4.26	3.02	0.5	1.08	1.55	1.94	2.48	2.81	2.66	2.30	2.44	2.28

Applications

Delayed-Pulse Generator With Override

In Figure 11, the first one-shot (OS_1) determines the delay time by preselected values of $R_{ext}1$ and $C_{ext}1$. The second one-shot (OS_2) determines the output pulse duration by preselected values of R_{ext} and C_{ext}. The output pulse can be terminated at any time by a positive rising pulse into the override input.

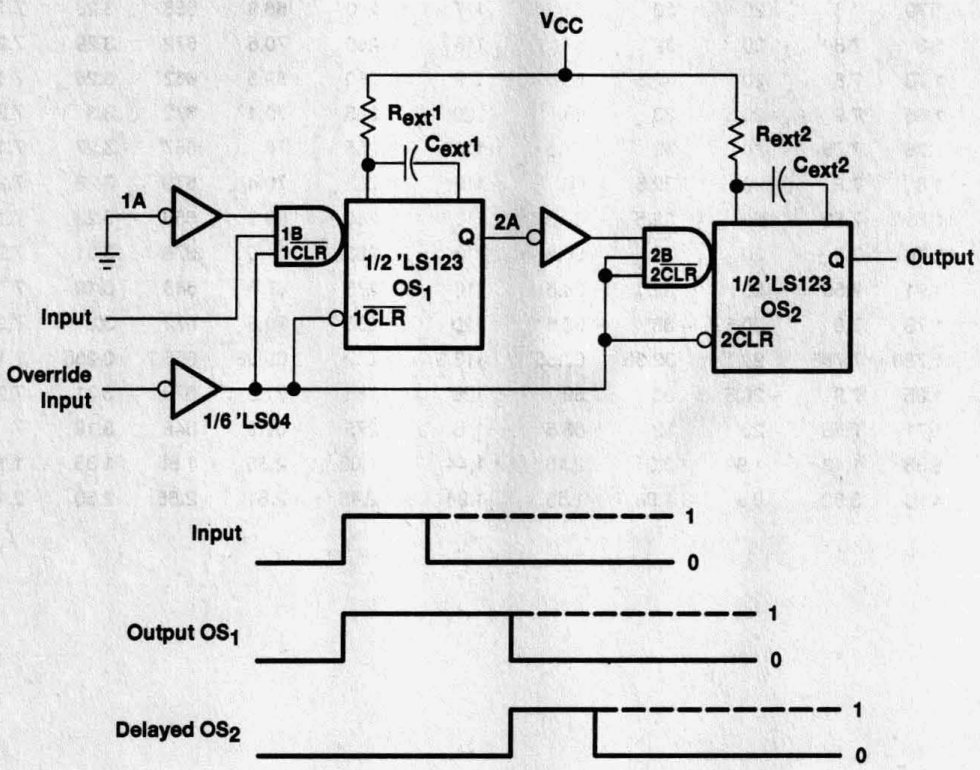


Figure 11. Delayed-Pulse Generator with Override

Missing-Pulse Detector

The pulse duration of OS_1, determined by $C_{ext}1$ and $R_{ext}1$, is set to at least one half the incoming pulse period. The rise of the incoming pulse fires OS_1, producing a high on the Q output. The output of OS_1 remains high as long as there is no missing pulse in the pulse train. Therefore, the one-shot is being retriggered. However, if a pulse is missing from the pulse train, the output of OS_1 falls and OS_2 fires.

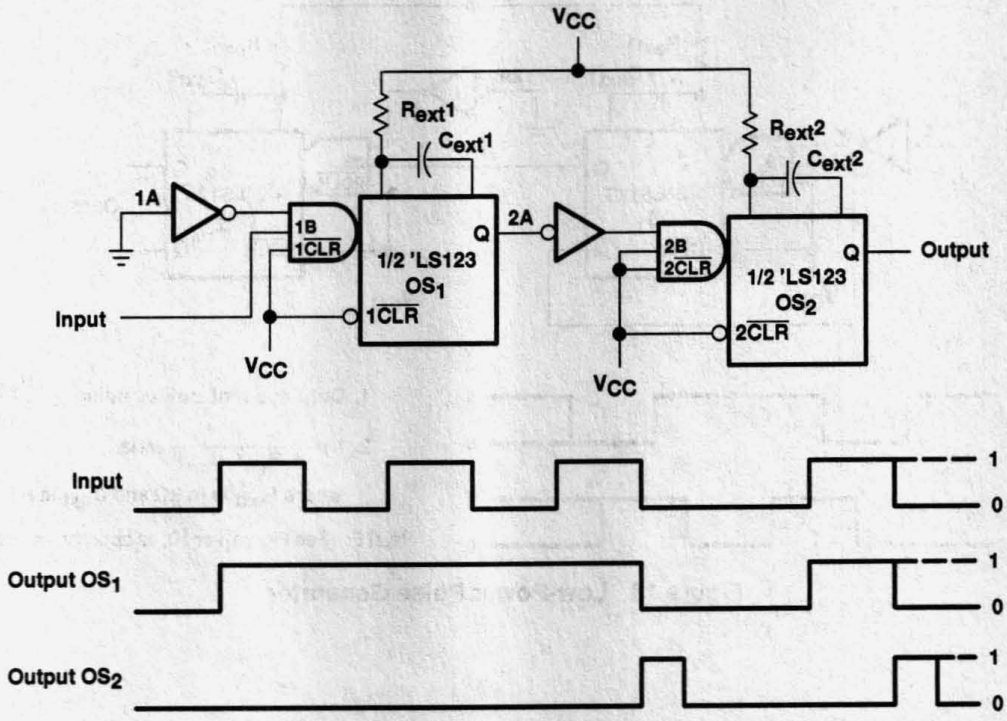
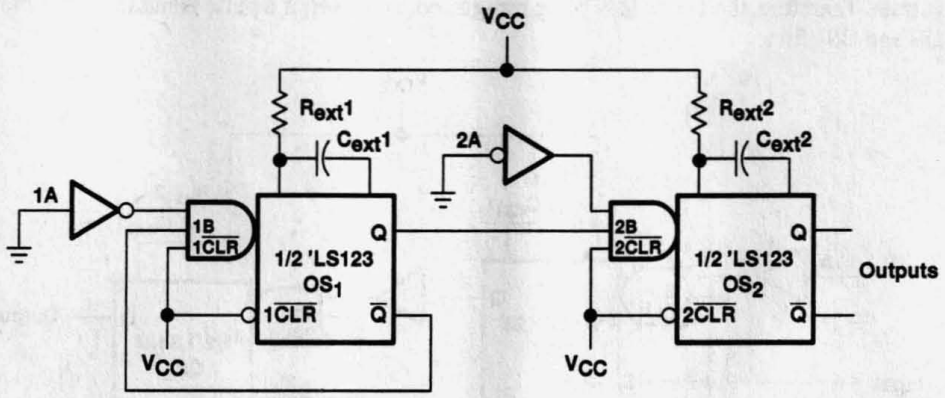
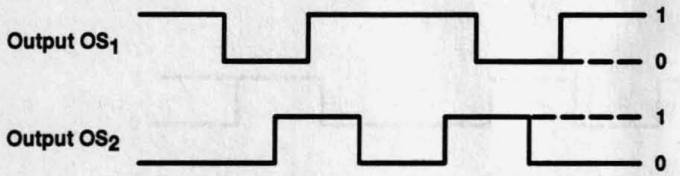


Figure 12. Missing-Pulse Detector

Low-Power Pulse Generator

The output frequency developed by the OS_1 configuration is determined by $R_{ext}1$ and $C_{ext}1$, while the output pulse duration of OS_2 is determined by $R_{ext}2$ and $C_{ext}2$. A low-power pulse generator is shown in Figure 13.





1. Duty cycle of output pulse $= \frac{R_{ext}2\ C_{ext}2}{R_{ext}1\ C_{ext}1}$

2. $f = \frac{1}{K\ R_{ext}1\ C_{ext}1}$ MHz

where R_{ext} is in kΩ and C_{ext} in pF.

NOTE: See Figure 4 or 10, as appropriate, for values of K.

Figure 13. Low-Power Pulse Generator

Negative/Positive Edge-Triggered One-Shot

Monostable multivibrators OS_1 and OS_2 arranged in a circuit such that a negative-going input pulse or a positive-going input pulse causes OS_1 (OS_2 disabled) to change states (see Figure 14). The outputs of OS_1 and OS_2 are connected to an OR gate, which outputs a pulse when OS_1 or OS_2 switches. This circuit can also be utilized as a frequency doubler.

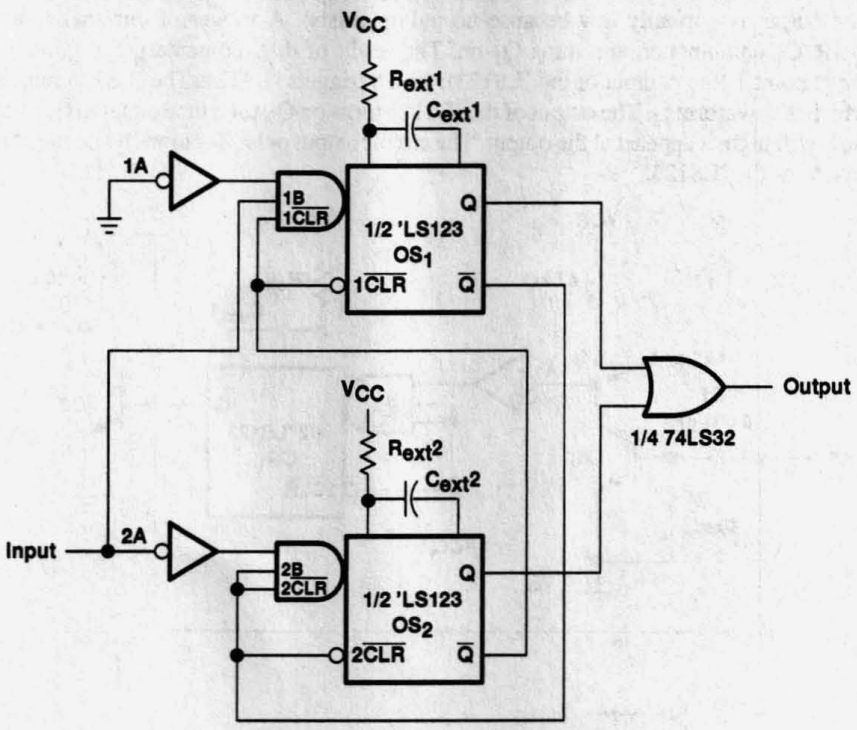


Figure 14. Negative/Positive Edge-Triggered One-Shot

Pulse-Duration Detector

The circuit shown in Figure 15 generates an output pulse (t_3) only if the trigger pulse duration (t_2) is wider than the programmed pulse ($t_w = K \bullet R_{ext} \bullet C_{ext}$) of the 'LS123.

Q_1 is normally off and the A input of the 'LS123 is approximately V_{CC}. The normal Q output of the 'LS123 is low and the Q_2 output is off (the output is normally low because no pullup exists). A trigger of duration t_1 applied at the input is differentiated by the R_1C_1 combination and turns Q_1 on. The result of that momentary condition at the base of Q_1 is a negative-going pulse at point 1 (the A input of the 'LS123), which triggers 'LS123. The 'LS123 remains on for the time $t_w = K \bullet R_{ext} \bullet C_{ext}$, which is waveform t_2. The output of the 'LS123 turns on Q_2 for a time equal to t_2. At the end of t_2, Q_2 turns off. If the input pulse is still high, it appears at the output. The circuit output pulse duration (t_3) equals the input pulse duration minus the pulse duration of the 'LS123.

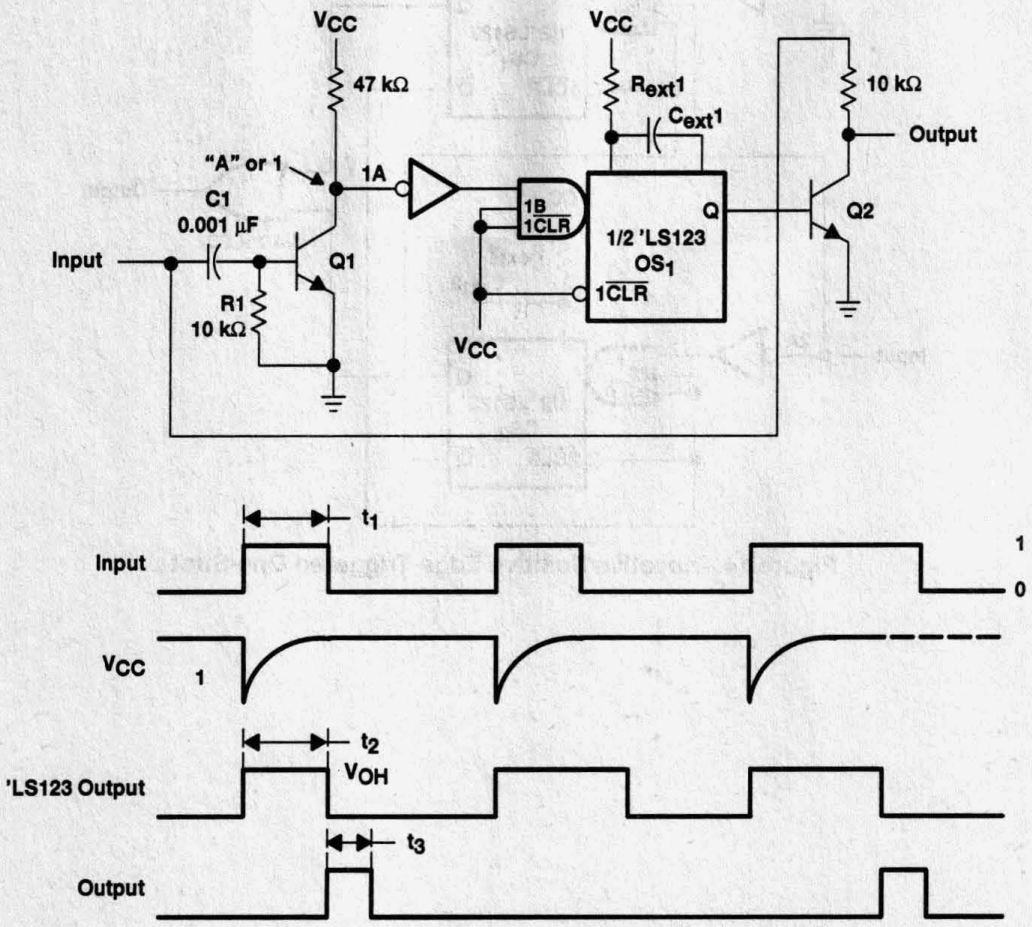


Figure 15. Pulse-Duration Detector

Frequency Discriminator

In Figure 16, R_1 and C_1 form a resistor-capacitor integration network that produces a linear output-voltage curve proportional to frequency over a limited range.

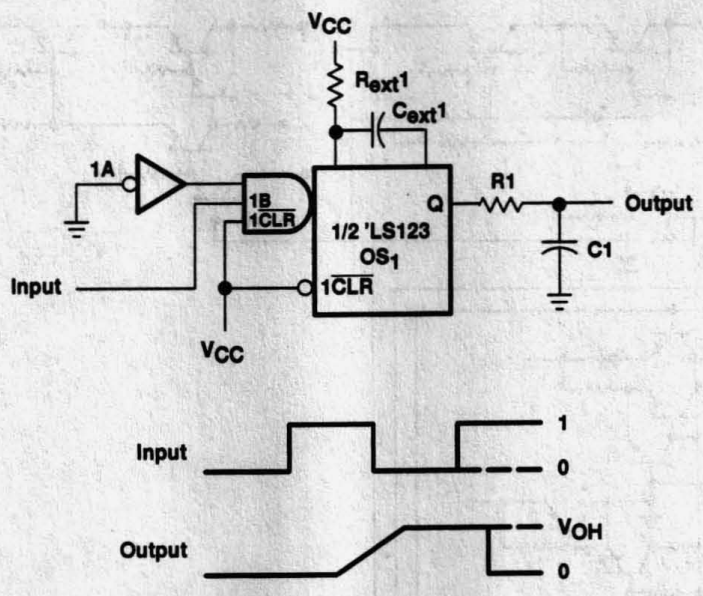
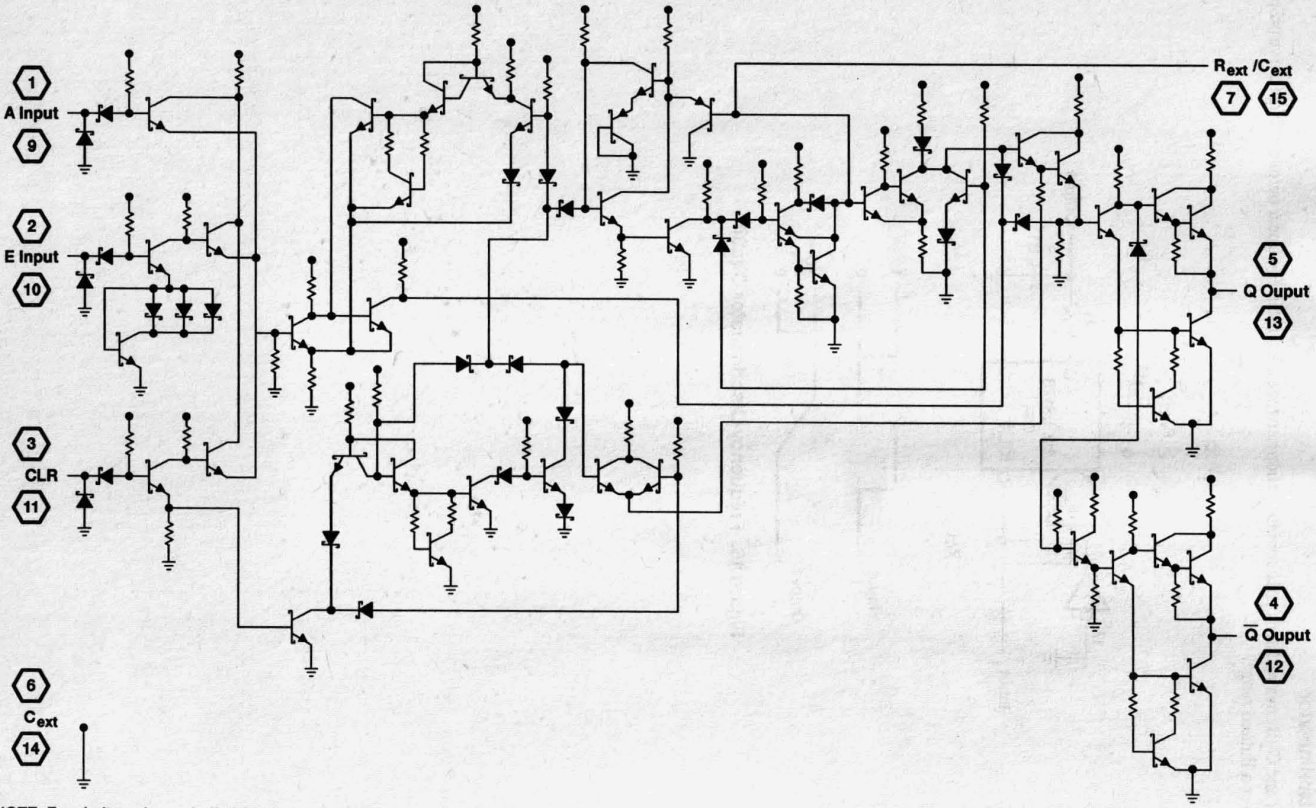


Figure 16. Frequency-Discriminator Circuit



NOTE: For clarity, only one-half of the device is shown.

Figure 17. 'LS123 Schematic

Digital Phase-Locked Loop Design Using SN54/74LS297

SDLA005B
March 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**3–151**
Device Description	**3–151**
First Order DPLL Equations	3–152
Ripple Cancellation	3–153
Loop Transfer Functions and Q-Factor	3–154
DPLL Circuit Implementations and Applications	**3–155**
Lock Detection	3–155
FSK Decoding	3–156
DPLL with Parallel Readout of Phase Data	3–156
DPLL with Real-Time Control of Lock Range and Center Frequency	3–158
Phase Demodulation	3–158
Lock Range Extension	3–159
'LS297 Clock Synchronizer for TMS9909 Floppy Disk Controller	**3–160**
SN54/74LS297 First-Order DPLL Lock Test Data	**3–160**
Design Considerations	**3–163**
Higher Order Digital Phase-Locked Loops	**3–163**
Summary	**3–165**
References	**3–165**

List of Illustrations

Figure	*Title*	*Page*
1	First Order Digital Phase-Locked Loop	3–151
2	Phase Detector Input vs Output with Zero Phase Error	3–152
3	I/D Circuit Waveforms	3–153
4	DPLL Transfer Characteristics	3–153
5	Ripple Cancellation Circuits	3–154
6	Linear Control System Representation of First Order DPLL	3–155
7	Lock Detection Circuit and Waveforms	3–155
8	FSK Decoder and Waveforms	3–156
9	DPLL with Latched Phase Data	3–157
10	DPLL with Microprocessor Control of Bandwidth and Center Frequency	3–158
11	Phase-Shift Demodulator	3–159
12	Lock Range Extension	3–159
13	Floppy Disk Controller Application	3–160
14	Second Order DPLL	3–164

List of Tables

Table	*Title*	*Page*
1	Register Output vs Phase Error	3–156
2	'LS297 Phase Lock Test Data – EXOR Phase Detector DPLL Circuit	3–161
3	'LS297 Phase Lock Test Data – Edge Controlled Phase Detector DPLL Circuit	3–161
4	'LS297 Phase Lock Test Data – EXOR Ripple Cancellation DPLL Circuit	3–162
5	'LS297 Phase Lock Test Data – Edge Controlled Ripple Cancellation	3–162

Digital Phase-Locked Loop Design Using SN54/74LS297

Author
Donald G. Troha

Contributors
James D. Gallia
Low Power Schottky Applications Group

INTRODUCTION

Although the concept of the phase-locked loop (PLL) has been in existence for several decades, until recently the PLL function has been implemented by predominantly analog methods. Recent emphasis on digital methods of signal processing has made it desirable to perform the PLL function digitally. For example, the use of a digital phase-locked loop (DPLL) in place of an analog loop in a digital system would eliminate the need for A-to-D and D-to-A conversion.

The SN54/74LS297 described below performs the first-order phase-locked loop function with a high degree of accuracy and a minimum of external components. Features of the 'LS297 DPLL include:

- Entirely digital design
- Accuracy is not affected by temperature and supply voltage variations
- Bandwidth and center frequency are digitally programmable
- Narrow bandwidth (high Q) loops are feasible
- Ripple cancellation features are provided
- Higher order loops can be constructed by cascading.

The divide-by-N counter required by the DPLL is not provided in the 'LS297 package so that the user may choose a counter to meet his specific needs. For example, a divide-by-N counter with parallel outputs provides a direct digital readout of phase error information, while a programmable divide-by-N allows real-time control of loop center frequency. Both Exclusive-OR and edge-triggered phase detectors are provided in the 'LS297. Either phase detector may be used to construct a loop, or the two may be used together in ripple cancellation schemes. The DPLL phase-detector output provides a second means of extracting phase data from the loop in the form of a pulse-width modulated signal.

Although the DPLL and analog PLL perform the phase-locked function by entirely different methods, linear control system models for the loops are analogous, enabling the DPLL user to take advantage of work that has already been done with analog PLLs.

DEVICE DESCRIPTION

As shown in Figure 1, the basic digital phase-locked loop consists of four elements. a phase detector, a K-counter, an increment/decrement circuit, and a divide-by-N counter. With the exception of the divide-by-N counter, these elements are provided in a single 'LS297 package. Two external clocks must be provided to the 'LS297: a K-clock and an I/D-clock. However, in many DPLL applications, the two clocks may be common.

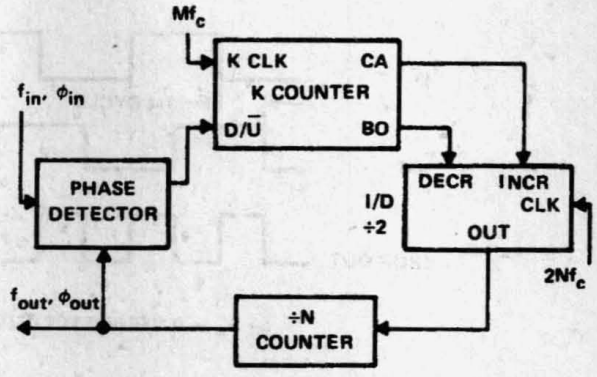


Figure 1. First Order Digital Phase-Locked Loop

As indicated in the data sheet, the phase detector compares the phase of the incoming signal, ϕ_{in}, with the phase of the signal produced by the DPLL, ϕ_{out}, and outputs an error signal, $k_d\phi_e$, where k_d is the gain of the phase detector and ϕ_e is the phase error ($\phi_{in} - \phi_{out}$). Two types of phase detectors are provided with the 'LS297: a conventional Exclusive-OR (EXOR) gate and an edge-

controlled phase detector (ECPD). The ECPD is a flip-flop which functions as follows: A high-to-low transition at ϕ_B will produce a high-level output, while a high-to-low transition at ϕ_{A2} will produce a low-level output. The phase error, ϕ_e, is defined to be zero when the phase detector output has a 50% duty cycle. Figure 2 illustrates that for $\phi_e = 0$, the absolute phase difference between f_{in} and f_{out} is 1/4 cycle for the EXOR case and 1/2 cycle for the ECPD case. The EXOR phase detector has a gain, k_d, of 4 and phase error limit of ±90°. The ECPD has a k_d of 2 and a phase error limit of ±180°.

The K-counter works together with the I/D circuit to produce a signal which is fed back through the divide-by-N counter to the phase detector to be compared with the incoming signal. The K-counter consists of an up-counter, and a down-counter with respective carry and borrow outputs. The D/$\overline{U}$ input to the K-counter controls which half (up or down) of the K-counter is in operation at a particular instant. In a typical DPLL configuration, the output of the phase detector connects to the D/$\overline{U}$ input of the K-counter.

The carry and borrow outputs of the K-counter are internally connected to the increment and decrement inputs of the I/D circuit, respectively, A pulse to the decrement input causes one half-cycle to be deleted from the I/D output, while a pulse to the increment input will result in a half-cycle being added to the I/D output. The I/D circuit produces an output frequency equal to one-half I/D clock when no increment or decrement is in process. This is illustrated in Figure 3.

An example of basic DPLL operation is as follows: If the inputs, f_{in} and f_{out}, to the phase detector are such that the phase detector output is low, then the "up" portion of the K-counter operates, eventually producing a carry pulse. This carry pulse is fed to the increment input of I/D circuit causing one half-cycle to be added to the I/D output. Similarly, a high at the phase detector output enables the "down" portion of the K-counter, eventually producing a borrow pulse to the decrement input which deletes one half-cycle from the I/D output. The DPLL continually adjusts the phase of f_{out} in this fashion so that in the lock condition a definite phase difference will exist between f_{in} and f_{out}.

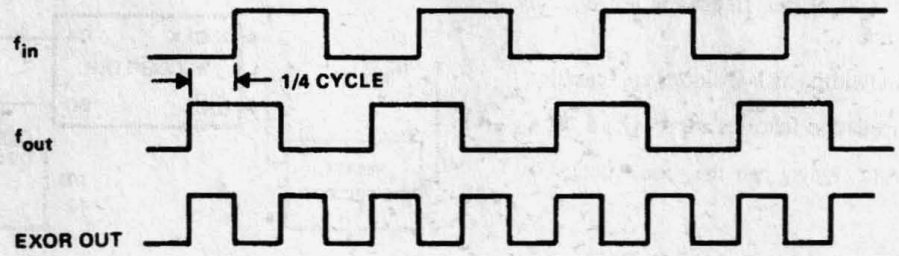
First Order DPLL Equations

The block diagram of a first order digital phase-locked loop is illustrated in Figure 1. The K-clock has a frequency of Mf_c and the I/D-clock has a frequency of $2Nf_c$, where M is a constant, f_c is the loop center frequency, and N is the modulus of the divide-by-N counter. The I/D-clock, frequency and divide-by-N modulus will therefore determine the loop center frequency:

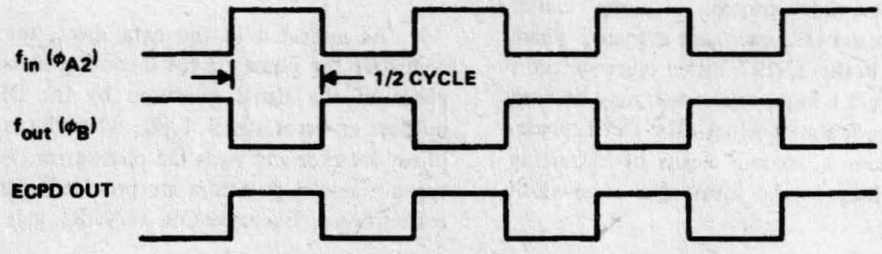
$$f_c = \text{I/D Clock}/2N \quad \text{Hz} \tag{1}$$

From the data sheet, we have expressions for the K-counter and I/D circuit outputs:

$$K_{out} = (k_d \phi_e Mf_c)/K \quad \text{Hz} \tag{2}$$



(a) ϕ_e = 0 USING EXCLUSIVE-OR PHASE DETECTOR



(b) ϕ_e = 0 USING EDGE-TRIGGERED PHASE DETECTOR

Figure 2. Phase Detector Input vs Output with Zero Phase Error

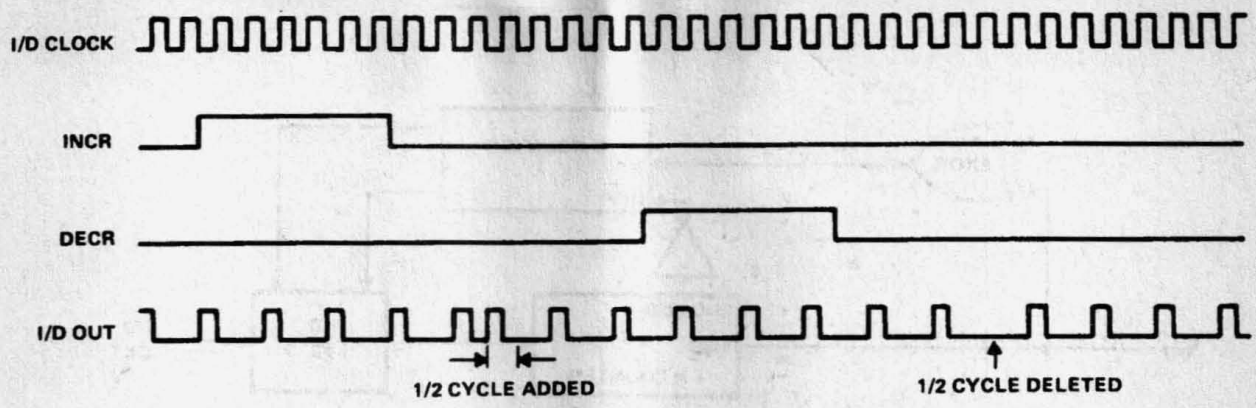


Figure 3. I/D Circuit Waveforms

$$I/D_{out} = Nf_c + (k_d \phi_e Mf_c)/2K \quad Hz \qquad (3)$$

where k_d is the phase detector gain, ϕ_e is the phase error, and K is the modulus of the K-counter.

The loop output is:

$$f_{out} = f_c + (k_d \phi_e Mf_c)/2KN \quad Hz \qquad (4)$$

From this equation we can derive the tracking frequency range Δf_{max}. At the limit of lock range, $k_d \phi_e$ is ±1. Therefore:

$$\Delta f_{max} = (f_{out})_{max} - f_c = Mf_c/2KN \quad Hz \qquad (5)$$

It is evident from the above equation that the lock range of the loop may be adjusted by adjusting K, the modulus of the K-counter.

When the DPLL is in the lock condition, f_{out} equals f_{in}, and a definite phase error, ϕ_e, will exist between the two signals. From equation (4) we obtain:

$$\phi_e = 2KN (f_{in} - f_c)/k_d Mf_c \quad cycles \qquad (6)$$

which is the phase error between f_{in} and f_{out} under lock. This is illustrated in Figure 4. For a phase error of zero, f_{in} must equal the center frequency, f_c.

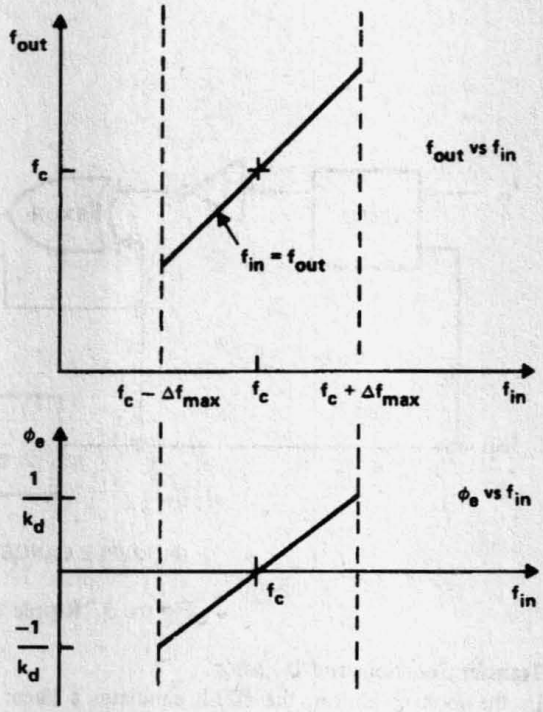


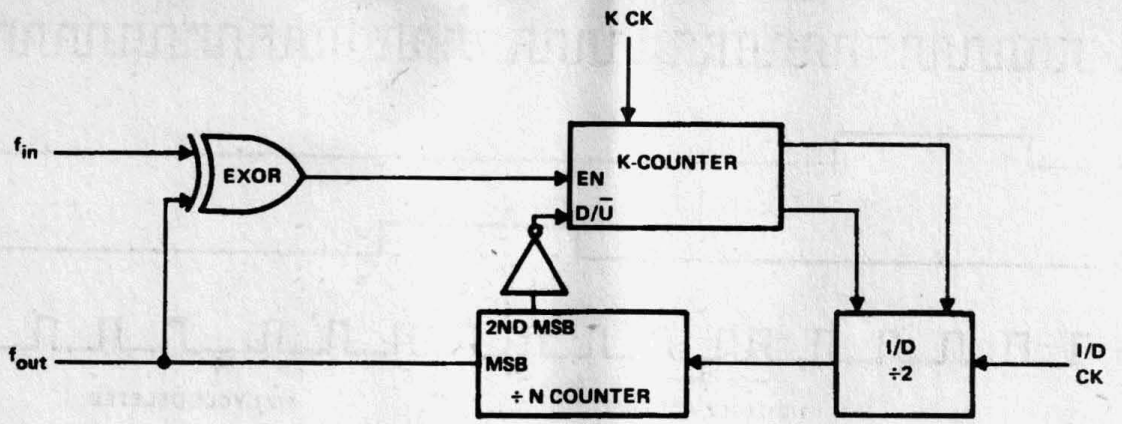
Figure 4. DPLL Transfer Characteristics (in lock)

Ripple Cancellation

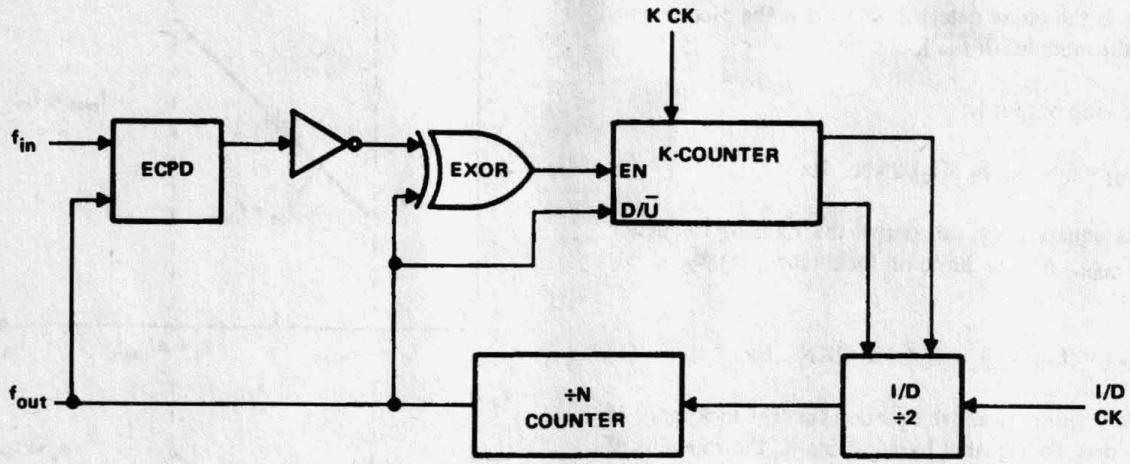
Examining the basic DPLL configuration in Figure 1, we see that the K-counter should continue to function, producing periodic carry and borrow pulses, even if the loop is locked with zero phase error. If K is too small, the K counters will recycle too often, producing repeated carry pulses followed by repeated borrow pulses. This will result in a duty cycle error called ripple in the DPLL output. This ripple may be reduced to a value of 1/N cycles at the divide-by-N counter output by making K sufficiently large, specifically K > M/4 for DPLL circuits utilizing the EXOR phase detector and K > M/2 for ECPD circuits, so that the phase correction pulses will cancel in the lower order bits of the divide-by-N counter.

Alternatively, one of the ripple cancellation circuits shown in Figure 5 may be used to minimize ripple. When either of these schemes is implemented, the K-counter is disabled when the DPLL is in a lock condition with zero phase error. While these circuits act to minimize ripple, they also have the effect of narrowing the lock range of the loop. The loop phase error limit (±90° for EXOR DPLLs and ±180° for ECPD DPLLs) is reduced by a factor of 1/(1 + 1/2K), and the phase detector gain, k_d is reduced by 1/2. This results in an adjusted lock range of:

$$\Delta f_{max} = Mf_c/(1 + 1/2K)\, 4KN \quad Hz \qquad (7)$$



(a) RIPPLE CANCELLATION WITH EXOR PHASE DETECTOR



(b) RIPPLE CANCELLATION WITH ECPD

Figure 5. Ripple Cancellation Circuits

Loop Transfer Functions and Q-Factor

In the lock condition, the DPLL simulates a linear control system analogous to a first order analog phase-locked loop, (Figure 6). The K-counter of the DPLL acts as an integrator in this system. From Figure 6 the open loop transfer function G(s) can be written:

$$G(s) = k_v/s \tag{8}$$

where k_v is the total loop gain:

$$k_v = k_d\, Mf_c/2KN \quad \text{rad/s} \tag{9}$$

The closed loop transfer function is thus:

$$H(s) = k_v/(s + k_v) \tag{10}$$

The 3-dB bandwidth, $\omega_{3\ dB}$, is therefore equal to k_v, the total loop gain.

The digital phase-lock loop may be thought of as a filter because it filters out high frequency phase changes from the input signal. Conventional filters are characterized by a quality factor "Q," which relates filter bandwidth and center frequency. The Q of a DPLL is similarly defined:

$$Q = \omega_c/2\omega_{3\ dB} = 2\pi\, KN/k_d\, M \tag{11}$$

If the K-clock and I/D-clock are common (M = 2N), the expression for Q simplifies to:

$$Q = \pi\, K/k_d \tag{12}$$

Since K can be programmed to a value of 2^3 to 2^{17}, a common clock, first order, DPLL can have a Q ranging from 6 to over 205,000.

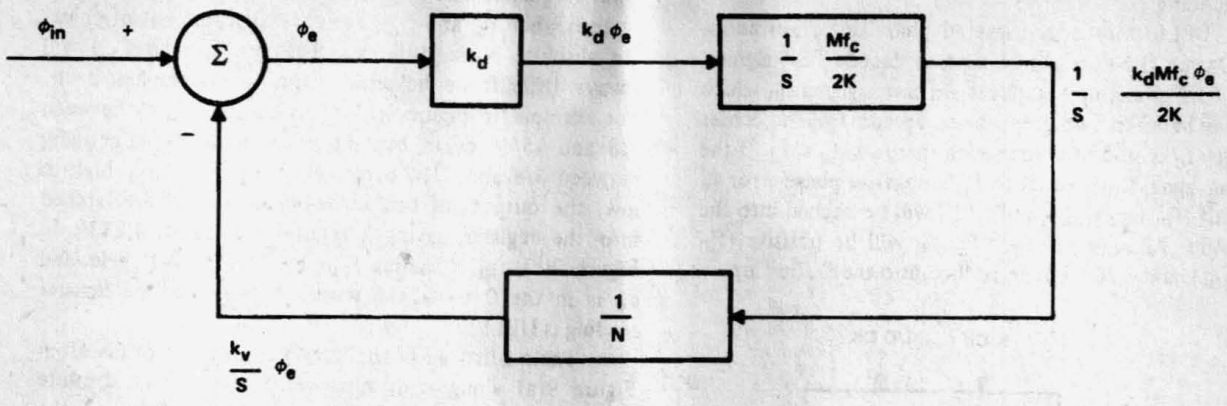


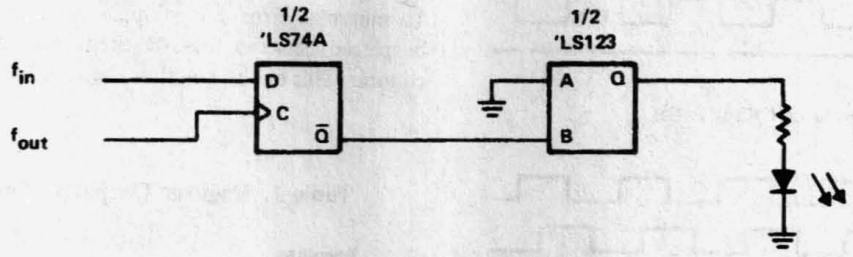
Figure 6. Linear Control System Representation of First Order DPLL

DPLL CIRCUIT IMPLEMENTATIONS AND APPLICATIONS

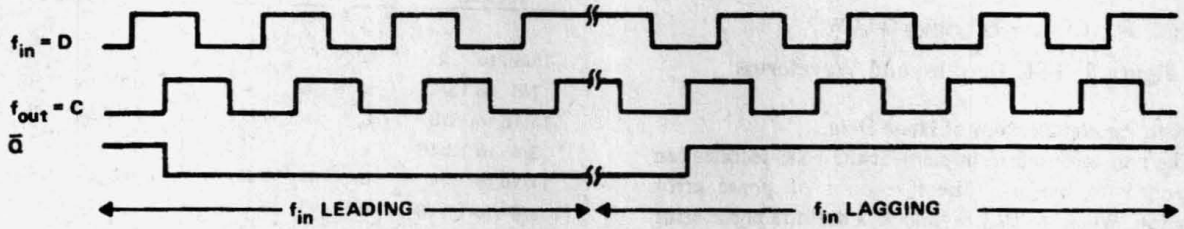
Lock Detection

Figure 7(a) illustrates a simple lock detection circuit which can be built with a D-type flip-flop and a monostable multivibrator. Waveforms in Figure 7(b) illustrate that if the DPLL is in lock, $\overline{Q}$ from the D flip-flop will be either high or low, depending on the phase difference between f_{in} and f_{out}. The result is that the monostable does not fire, and the LED does not light up. An out-of-lock condition is illustrated in Figure 7(c). In this condition, the D flip-flop will output a series of pulses which will repeatedly fire the monostable and light the LED.

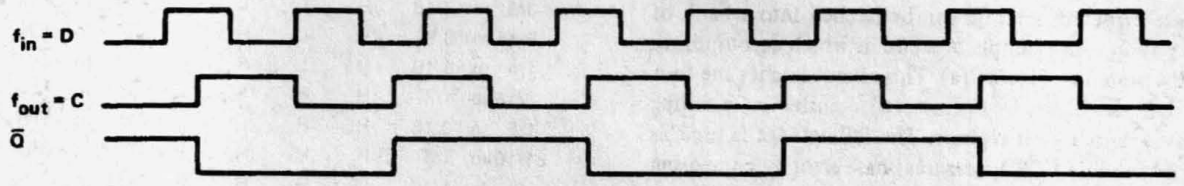
In ECPD DPLL circuits, this lock detection circuit works well for all frequencies within the lock range except at $f_{in} = f_c$. If f_{in} varies around f_c, a false out-of-lock indication will result. This circuit works at all frequencies within the lock range of EXOR phase detector loops.



(a) LOCK DETECTION CIRCUIT



(b) LOCK CONDITION WAVEFORMS

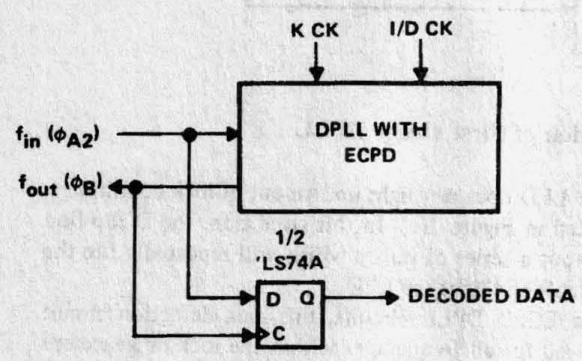


(c) OUT-OF-LOCK WAVEFORMS

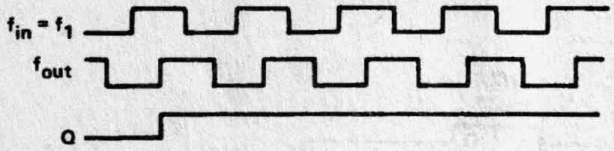
Figure 7. Lock Detection Circuit and Waveforms

FSK Decoding

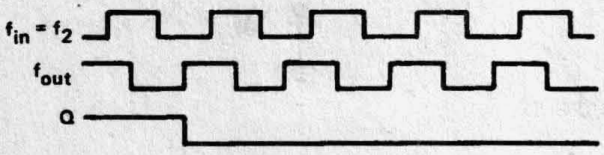
A DPLL with edge-triggered phase detection and a single D-type flip-flop can be used to decode FSK signals, (Figure 8). For example, suppose we have a signal f_{in} which alternates between two frequencies f_1 and f_2. The center frequency f_c should be chosen such that $f_1 < f_c < f_2$. If the incoming signal f_{in} is equal to f_1, a negative phase error ϕ_e will result (f_{in} lags f_{out}), and a "1" will be latched into the D flip-flop. Likewise, if $f_{in} = f_2$, ϕ_e will be positive (f_{in} leads f_{out}), and a "0" will be latched into the D flip-flop.



(a) FSK DECODER CIRCUIT



(b) $f_{in} = f_1$ LOCKS Q HIGH



(c) $f_{in} = f_2$ LOCKS Q LOW

Figure 8. FSK Decoder and Waveforms

DPLL with Parallel Readout of Phase Data

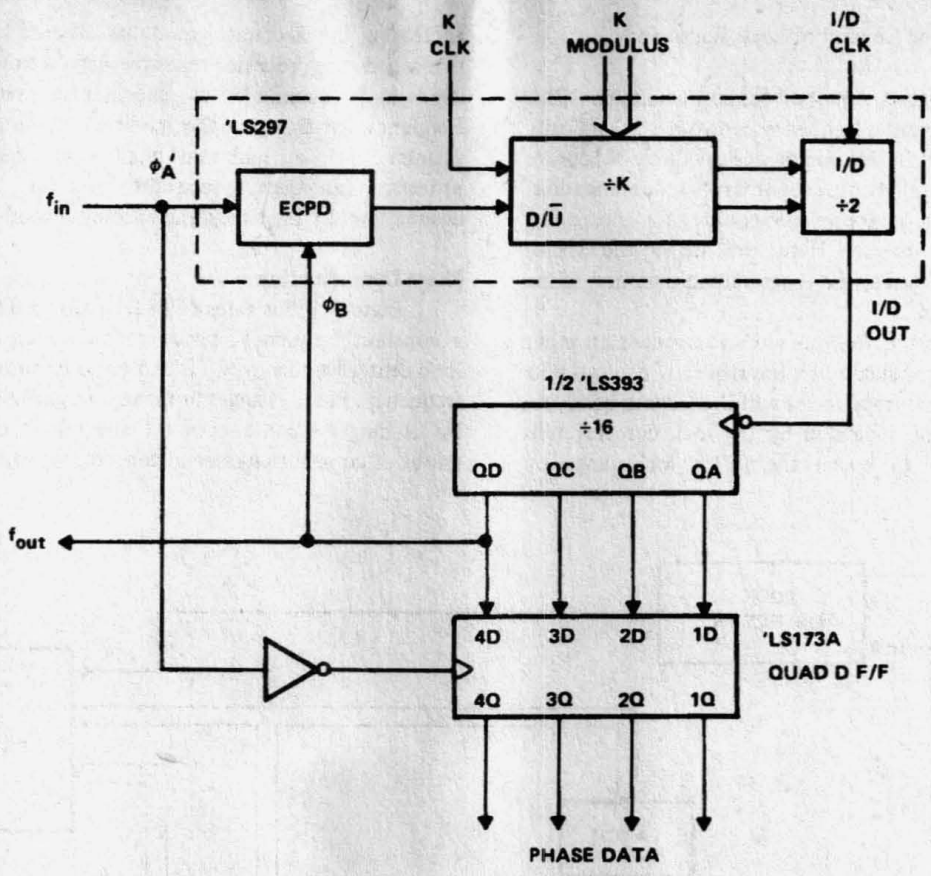
The concept used to implement the FSK decoder can be extended to perform direct readout of phase error information. When a DPLL is in lock, a definite phase error will exist between f_{in} and f_{out} and any intermediate stage of the divide-by- N counter. If a divide-by-N counter with parallel outputs is incorporated into the phase-locked loop, the phase error information can be latched into a bank of registers by f_{in}. An example of a circuit which accomplishes this is illustrated in Figure 9(a). This circuit latches the four outputs of the divide-by-N (n = 16) counter on a falling edge of f_{in} into a 4-bit register. The falling edge is used as the strobe because ECPD measures phase error by comparing falling edges of f_{in} and f_{out}. The output of the register can then be decoded to give the phase error, ϕ_e, from which the input frequency can be calculated. Because ϕ_e is defined to be zero when f_{in} and f_{out} are one-half cycle out of phase, the absolute phase difference between f_{in} and f_{out} will always differ from the phase error, ϕ_e, by one-half cycle. For example, in Figure 9(b), f_{in} is leading f_{out} by between 7/8 and 15/16 cycle, but the phase error, ϕ_e, is actually between 3/8 and 7/16 cycle. When f_{in} goes from high to low, the outputs of the divide-by-16 counter are latched into the register, giving a register reading of LLLH. In Figure 9(c), f_{in} is leading f_{out} by 7/16 to 1/2 cycle, and ϕ_e is in the 0 to −1/16 range. In this case, the register reading is HLLL.

Table I lists all possible register readings for circuit in Figure 9(a) along with phase error values and absolute phase difference values. The absolute phase difference is the fraction of a cycle by which f_{in} leads f_{out}, and the phase error, ϕ_e, is the absolute phase difference minus one-half cycle. The register output may be related to the absolute difference between f_{in} and f_{out} by considering the register output to be an inverted data binary fraction expression for the absolute phase difference. The phase error, ϕ_e, may thus be computed by inverting the bits of the output register to obtain a binary fraction reading of the absolute phase difference, then subtracting a binary one-half. The computed phase error could then be used in Eq. (6) to compute the input frequency f_{in}.

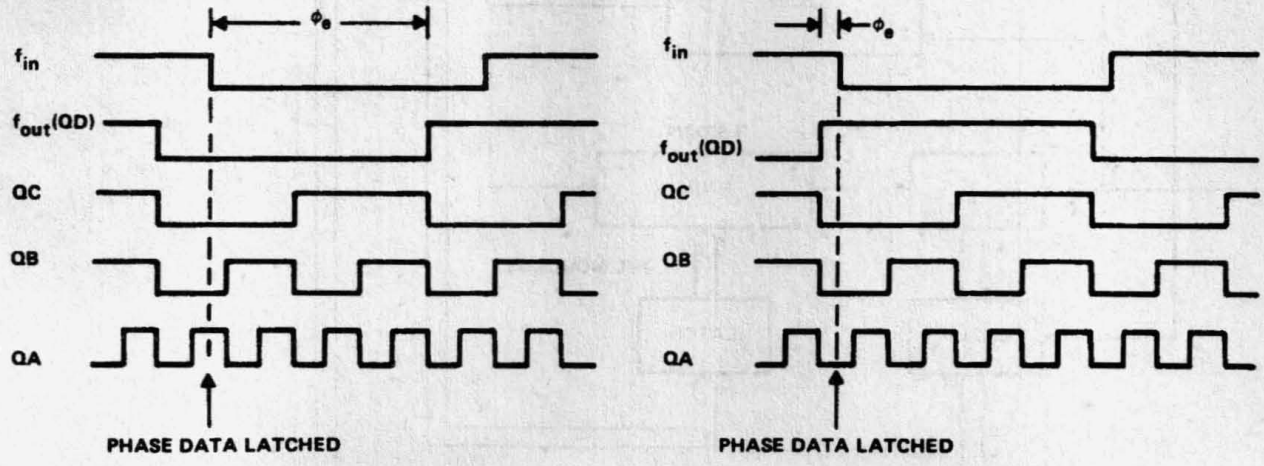
A higher degree of accuracy may be attained by adding more stages to the divide-by-N counter and register. To minimize error due to ripple, more counter stages could be placed between the I/D circuit and the parallel output counter. This circuit could be used for FM demodulation.

Table 1. Register Output vs Phase Error

Absolute Phase Difference (Cycles)	Register Output 4Q	3Q	2Q	1Q	ϕ_e (Cycles)
15/16 to 1	L	L	L	L	7/16 to 1/2
7/8 to 15/16	L	L	L	H	3/8 to 7/16
13/16 to 7/8	L	L	H	L	5/16 to 3/8
3/4 to 13/16	L	L	H	H	1/4 to 5/16
11/16 to 3/4	L	H	L	L	3/16 to 1/4
5/8 to 11/16	L	H	L	H	1/8 to 3/16
9/16 to 5/8	L	H	H	L	1/16 to 1/8
1/2 to 9/16	L	H	H	H	0 to 1/16
7/16 to 1/2	H	L	L	L	−1/16 to 0
3/8 to 7/16	H	L	L	H	−1/8 to −1/16
5/16 to 3/8	H	L	H	L	−3/16 to −1/8
1/4 to 5/16	H	L	H	H	−1/4 to −3/16
3/16 to 1/4	H	H	L	L	−5/16 to −1/4
1/8 to 3/16	H	H	L	H	−3/8 to −5/16
1/16 to 1/8	H	H	H	L	−7/16 to −3/8
0 to 1/16	H	H	H	H	−1/2 to −7/16



(a) CIRCUIT DIAGRAM



(b) A PHASE ERROR OF BETWEEN 3/8 AND 7/16 CYCLE LATCHES LLLH INTO THE D FLIP-FLOPS

(c) A PHASE ERROR OF 0 to −1/16 CYCLE LATCHES HLLL INTO THE D FLIP-FLOPS

Figure 9. DPLL with Latched Phase Data

DPLL with Real-Time Control of Lock Range and Center Frequency

Figure 10 suggests a method for constructing a DPLL with lock range and center frequency controlled dynamically by a microprocessor. In this circuit, the divide-by-N counter is split between a parallel output counter with direct readout of phase data and a programmable counter for controlling the loop center frequency. Here, the use of the SN54/74LS292/4 is suggested as the programmable portion of the divide-by-N counter.

As an application for this circuit, consider an input signal, f_{in}, to be demodulated by the DPLL, which can take on any one of several frequencies within a certain band. An out-of-lock condition indicated by the lock detector tells the microprocessor to widen the DPLL lock range by decreasing the K-counter modulus. When a lock condition is reached, the processor reads the phase error, ϕ_e, from the divide-by-N counter latch and adjusts the loop center frequency by changing the modulus of the programmable counter until a minimum phase error is reached. The processor can then reduce the loop lock range to the desired level by increasing the K-counter modulus.

Phase Demodulation

Figure 11 illustrates a DPLL circuit used to demodulate a constant frequency, phase-modulated input signal. The loop center frequency, f_c, is chosen to be equal to incoming frequency. Phase changes in the input signal may be detected by latching the contents of the divide-by-N counter with a strobe of constant phase, and constant frequency, f_c. For an

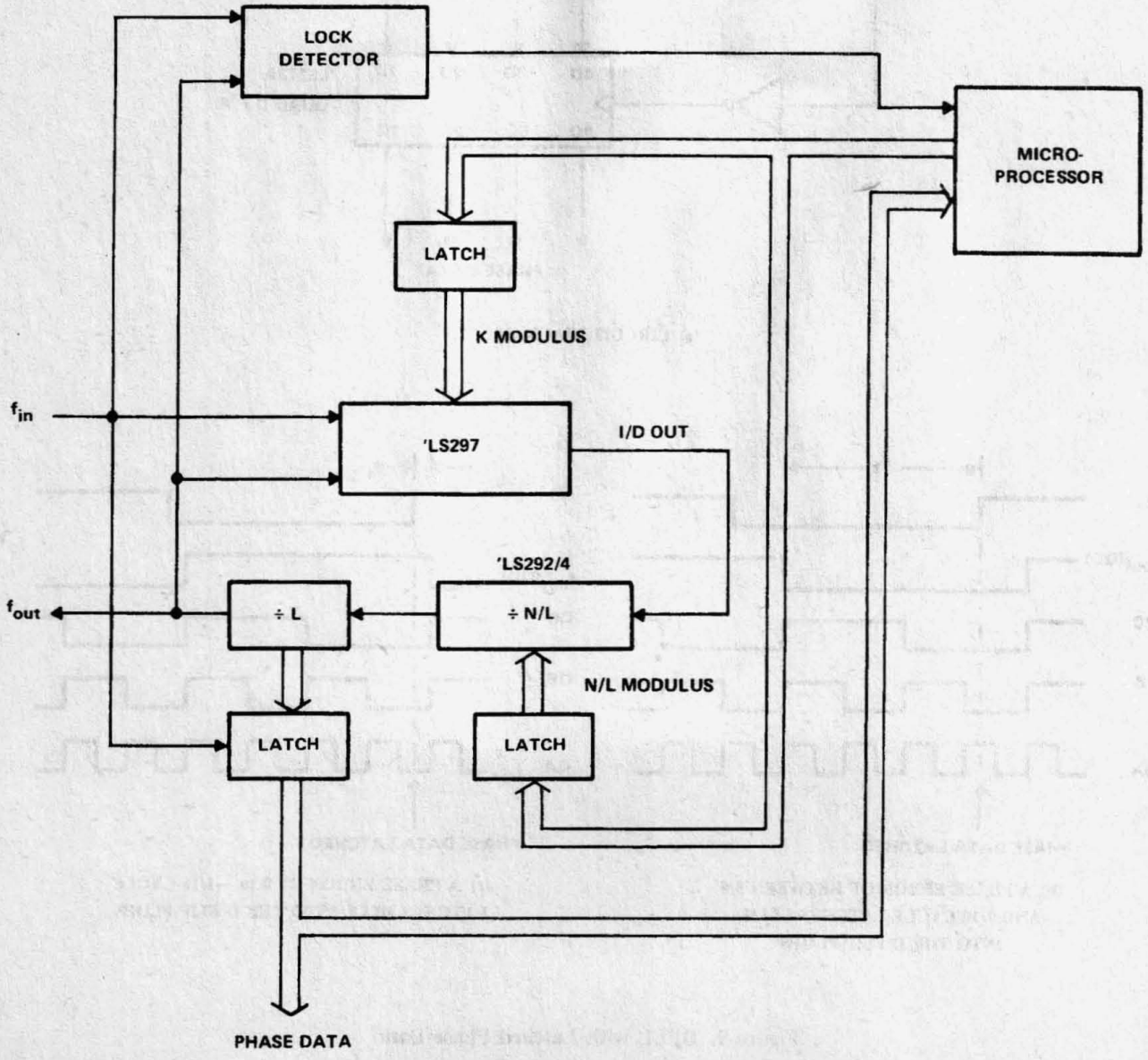


Figure 10. DPLL with Microprocessor Control of Bandwidth and Center Frequency

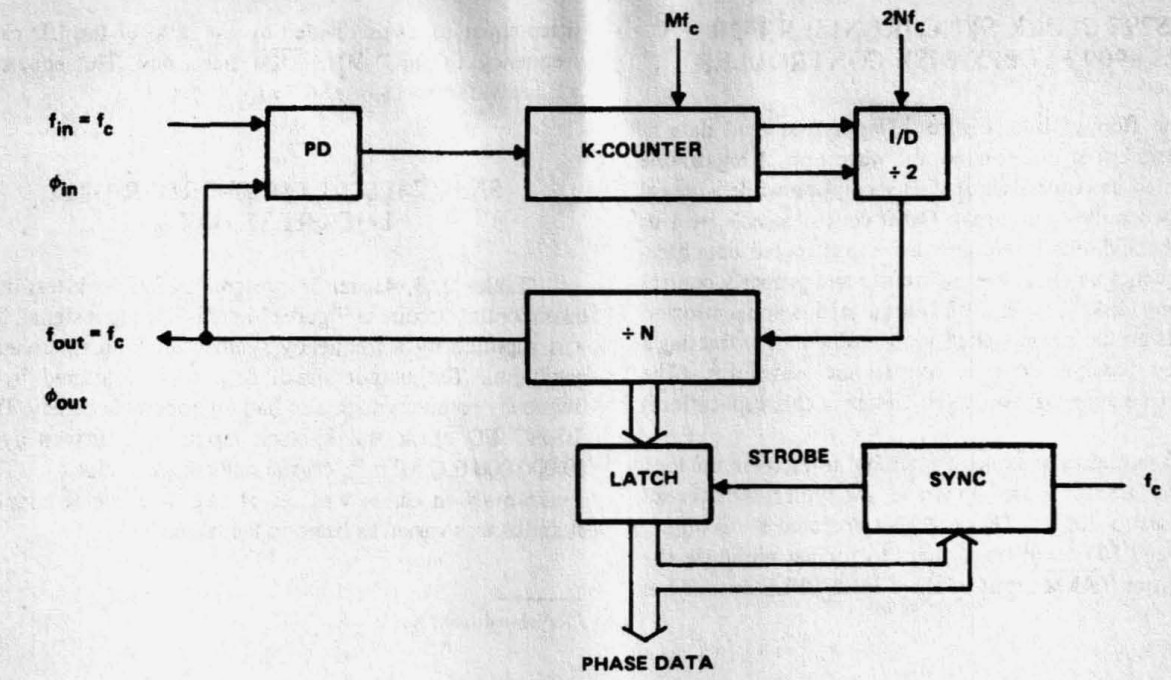


Figure 11. Phase-Shift Demodulator

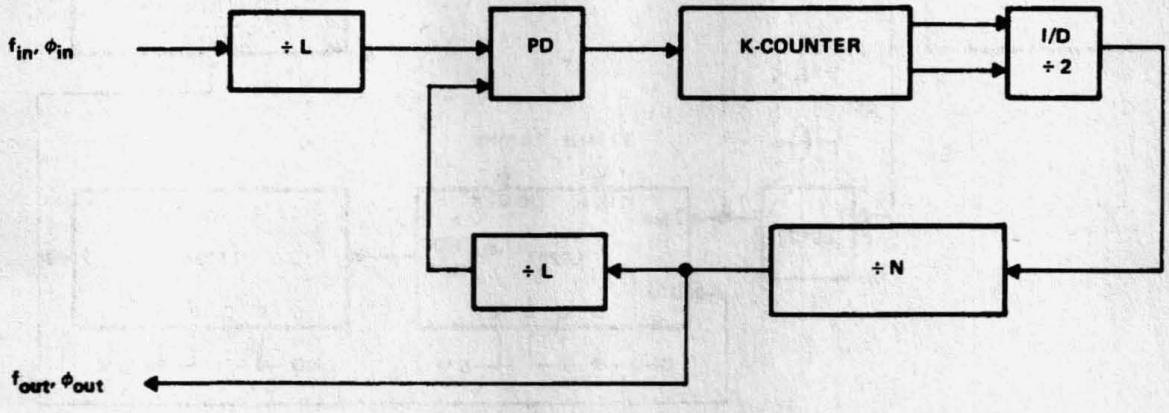


Figure 12. Lock Range Extension

accurate digital readout of phase data, some synchronizing circuitry will be required to synchronize the phase of the latch strobe with the phase of the incoming signal. Reference 4 elaborates on the use of this method of phase demodulation in Omega receivers.

Lock Range Extension

By placing counters of equal modulo (L) on each of the two phase detector inputs as shown in Figure 12, the DPLL 3-dB bandwidth as given by Eq. (9) is decreased by the factor L. In order to obtain the same 3-dB bandwidth as a loop without the divide-by-L counters, the K-counter modulus must be decreased by a factor of L. This has the effect of widening the loop lock range as given by Eq. (5).

'LS297 CLOCK SYNCHRONIZER FOR TMS 9909 FLOPPY DISK CONTROLLER

The floppy disk (Figure 13) puts out read data at 250 kbits/s but it is a nonperiodic waveform. A logical one is presented as two pulses at 2-μs separation while a logical zero is two pulses 4 μs apart. Other control signals are 1 μs apart. The TMS 9909 requires the reconstructed data baseline frequency in order to synchronize and properly control the floppy disk. The 'LS297 is used in this application to solve this classic phase-locked loop problem of extracting a frequency baseline from a nonperiodic waveform. (The baseline frequency happens to be 1 MHz in this application.)

To minimize phase-lock jitter and to increase the lock range, the 'LS122 is used to stretch the typical 200 ns read data pulses to 500 ns. The 'LS297 is operated at maximum K-clock and I/D clock frequencies to further minimize the output jitter. ($\overline{RKM}$ input or the 1 MHz DPLL output has jitter equal to ± 1 μs divided by the ratio of the I/D clock frequency to the 1 MHz $\overline{RKM}$ frequency. This equals to ± 1 μs divided by 15 or ± 66.7 ns.)

SN54/74LS297 FIRST-ORDER DPLL LOCK TEST DATA

Tables 2, 3, 4, and 5* present 'LS297 lock test data taken for the circuits in Figures 1 and 5. The input signal, f_{in}, was supplied by a frequency synthesizer with microhertz resolution. The output signal f_{out}, was monitored by a frequency counter which also had microhertz accuracy. The 'LS297 I/D clock and K-clock inputs were driven by a 10.000 000 000 MHz crystal-controlled clock. The divide-by-N modulus was set at 256, and the K-counter modulus was varied as listed in the tables.

*Reprinted from Ref. 5.

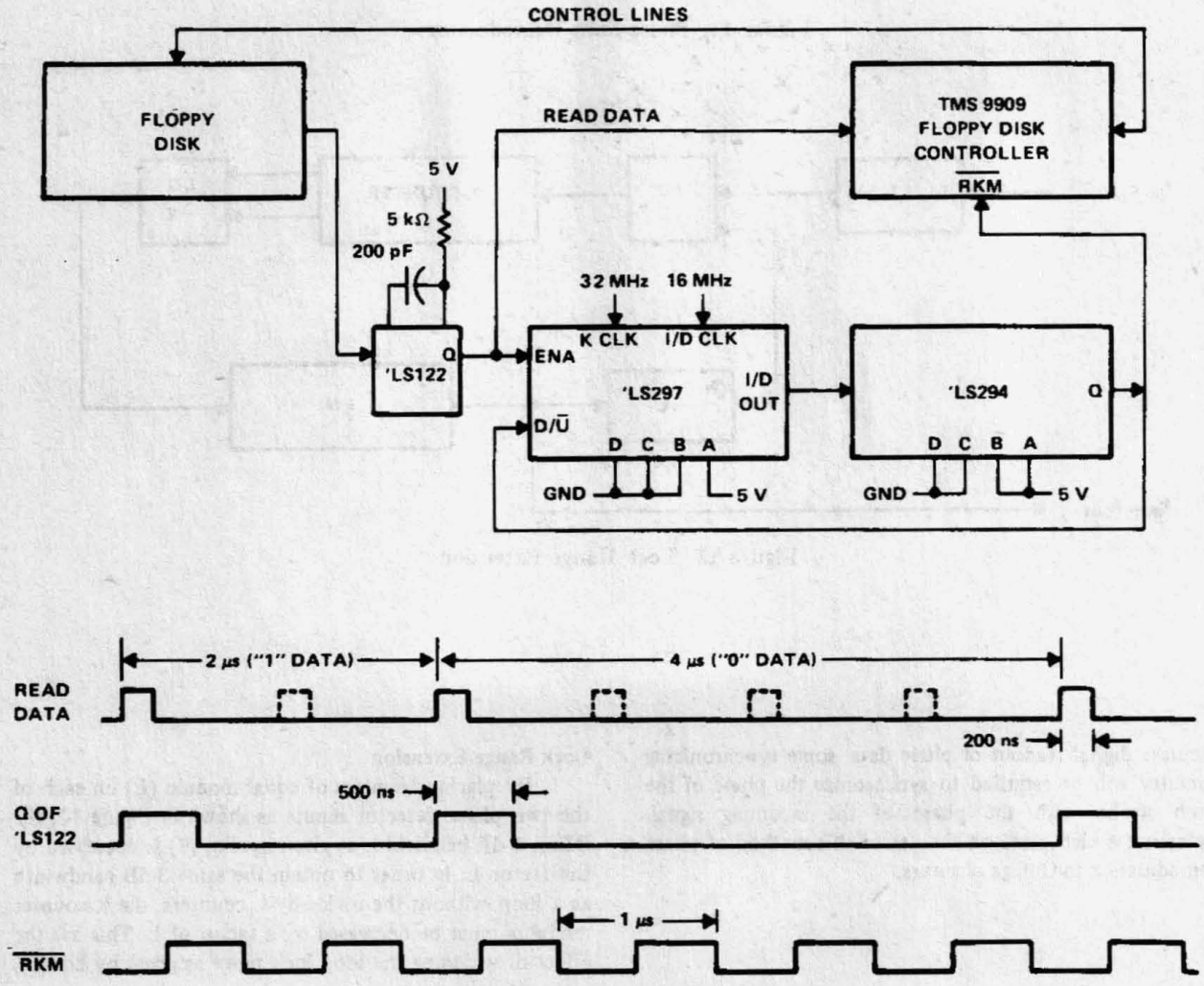


Figure 13. Floppy Disk Controller Application

Table 2. 'LS297 Phase Lock Test Data — EXOR Phase Detector DPLL Circuit [Figure 1] (M = 2N = 512; f_C = 19531.25 Hz; K Clock = I/D Clock = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	$\phi_{E\,max}$ Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_C$ Frequency Lock Range (Hz)	$f_{OUT\,max}$ Maximum Lock Frequency (Hz)	$f_{OUT\,min}$ Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_C$ (cycles)
2^3	6.3	±0.70	19.07	90 ± 89.3	2422.33276	21953.58276	17108.91724	8/N
2^5	25.1	±0.70	4.76	90 ± 89.3	605.58319	20136.83319	18925.66681	2/N
2^7	100.5	±0.70	1.19	90 ± 89.3	151.39579	19682.64580	19379.85420	1/N
2^9	402.1	±0.70	2.98×10^{-1}	90 ± 89.3	37.84894	19569.09895	19493.40105	1/N
2^{11}	1608.5	±0.70	7.45×10^{-2}	90 ± 89.3	9.46223	19540.71224	19521.78776	1/N
2^{13}	6434	±0.70	1.86×10^{-2}	90 ± 89.3	2.36555	19533.61556	19528.88444	1/N
2^{15}	25736	±0.70	4.65×10^{-3}	90 ± 89.3	0.59138	19531.84139	19530.65861	1/N
2^{17}	102944	±0.70	1.16×10^{-3}	90 ± 89.3	0.14784	19531.39785	19531.10215	1/N

Table 3. 'LS297 Phase Lock Test Data — Edge Controlled Phase Detector DPLL Circuit [Figure 1] (M = 2N = 512; f_C = 19531.25 Hz; K Clock = I/D Clock = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	$\phi_{E\,max}$ Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_C$ Frequency Lock Range (Hz)	$f_{OUT\,max}$ Maximum Lock Frequency (Hz)	$f_{OUT\,min}$ Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_C$ (cycles)
2^3	12.6	±0.70	9.53	180 ± 177.9	2412.79602	21953.58276	17118.45398	16/N
2^5	50.3	±0.70	2.38	180 ± 177.9	603.19900	20136.83319	18928.05099	4/N
2^7	201.1	±0.70	5.96×10^{-1}	180 ± 177.9	150.79975	19682.64580	19380.45025	1/N
2^9	804.2	±0.70	1.49×10^{-1}	180 ± 177.9	37.69993	19569.09895	19493.55006	1/N
2^{11}	3217	±0.70	3.72×10^{-2}	180 ± 177.9	9.42498	19540.71224	19521.82502	1/N
2^{13}	12868	±0.70	9.31×10^{-3}	180 ± 177.9	2.35624	19533.61556	19528.89375	1/N
2^{15}	51472	±0.70	2.32×10^{-3}	180 ± 177.9	0.58906	19531.84139	19530.66094	1/N
2^{17}	205887	±0.70	5.82×10^{-3}	180 ± 177.9	0.14726	19531.39785	19531.10273	1/N

Table 4. 'LS297 Phase Lock Test Data — EXOR Ripple Cancellation DPLL Circuit [Figure 5(a)] (M = 2N = 512; f_C = 19531.25 Hz; K Clock = I/D Clock = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	ϕ_E max Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_C$ Frequency Lock Range (Hz)	f_{OUT} max Maximum Lock Frequency (Hz)	f_{OUT} min Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_C$ (cycles)
2^3	12.6	±0.70	9.53	0 ± 84.0	1139.36031	20670.61032	18320.08362	1/N
2^5	50.3	±0.70	2.38	0 ± 87.9	298.09658	19829.34658	19228.45840	1/N
2^7	201.1	±0.70	5.96×10^{-1}	0 ± 88.9	75.40103	19606.65110	19455.55210	1/N
2^9	804.2	±0.70	1.49×10^{-1}	0 ± 89.3	18.92447	19550.17447	19512.32553	1/N
2^{11}	3217	±0.70	3.72×10^{-2}	0 ± 89.3	4.73111	19535.98112	19526.51888	1/N
2^{13}	12868	±0.70	9.31×10^{-3}	0 ± 89.3	1.18277	19532.43278	19530.06722	1/N
2^{15}	51472	±0.70	2.32×10^{-3}	0 ± 89.3	0.29569	19531.54569	19530.95431	1/N
2^{17}	205887	±0.70	5.82×10^{-3}	0 ± 89.3	0.07923	19531.32392	19531.17608	1/N

Table 5. 'LS297 Phase Lock Test Data — Edge Controlled Ripple Cancellation DPLL Circuit [Figure 5(b)] (M = 2N = 512; f_C = 19531.25 Hz; K Clock = I/D Clock = 10 MHz)

K	Q $\left(\frac{\pi K}{K_D}\right)$	ϕ_E Phase Error Resolution (1/2N) (degrees)	Δf Frequency Resolution (Hz)	ϕ_E max Phase Error Lock Range (degrees)	Δf_{max} $f_{IN} - f_C$ Frequency Lock Range (Hz)	f_{OUT} max Maximum Lock Frequency (Hz)	f_{OUT} min Minimum Lock Frequency (Hz)	Ripple (Phase Error in ÷N Counter) $f_{IN} = f_C$ (cycles)
2^3	25.1	±0.70	4.76	180 ± 168.0	1139.36031	20670.61032	18320.08362	1/N
2^5	100.5	±0.70	1.19	180 ± 175.9	298.09658	19829.34658	19228.45840	1/N
2^7	402.1	±0.70	2.9×10^{-1}	180 ± 177.9	75.40103	19606.65110	19455.55210	1/N
2^9	1608.5	±0.70	7.4×10^{-2}	180 ± 178.6	18.92447	19550.17447	19512.32553	1/N
2^{11}	6434	±0.70	1.8×10^{-2}	180 ± 178.6	4.73111	19535.98112	19526.51888	1/N
2^{13}	25736	±0.70	4.6×10^{-3}	180 ± 178.6	1.18277	19532.43278	19530.06722	1/N
2^{15}	102944	±0.70	1.2×10^{-3}	180 ± 178.6	0.29569	19531.54569	19530.95431	1/N
2^{17}	411774	±0.70	2.9×10^{-4}	180 ± 178.6	0.07923	19531.32392	19531.17608	1/N

Calculated values for Q are listed in the tables along with measured values of phase error resolution; frequency resolution, Δf; phase error range; frequency lock range; maximum and minimum lock frequencies; and ripple. Phase error resolution, and frequency resolution can be best understood by recalling that the phase of the I/D circuit output is adjusted by half-cycles. This means that the phase of the output signal, f_{out}, will have an uncertainty or resolution of $\pm 1/2N$ cycles. For the data presented, N was set at 256, giving a phase resolution, $\Delta\phi$, of ±0.70 degrees. For a $\pm 1/2N$ phase resolution, Eq. (4) implies that the output frequency will have an uncertainty Δf of

$$\Delta f = \Delta\phi\, k_d\, Mf_c/2KN \quad Hz$$
$$= k_d\, Mf_c/4KN^2 \quad Hz \tag{13}$$

For common clock circuits (M = 2N), the expression simplifies to:

$$\Delta f = k_d\, f_c/2KN \quad Hz \tag{14}$$

The phase error lock range data in Tables 2, 3, 4, and 5 indicate that the lock ranges were reduced from the theoretical limits by the phase resolution factor 1/2N and loop propagation delays along with the factor of 1/(1 + 1/2K) mentioned earlier for ripple cancellation circuits. The lock frequency range, and minimum and maximum lock frequency data from the tables can be compared to theoretical limits expressed by Eq. (5) and Eq. (7).

DESIGN CONSIDERATIONS

The design of a first-order DPLL can be simplified by considering a few points. Having a common clock for the K-counter and I/D circuits simplifies calculations. However, making the K-clock higher in frequency than the I/D clock has the effect of widening the loop lock range, and vice versa. The phase detector should be chosen according to the input signal characteristics. The EXOR phase detector requires square wave inputs but is less sensitive to noise than the ECPD. The ECPD, while being more sensitive to the effects of noise, has a wider phase-error range, and has no duty cycle requirements. Recalling that the DPLL output frequency has a phase resolution of $\pm 1/2N$ cycles, the modulus (N) of the divide-by-N counter should be chosen such that phase resolution requirements are met.

Once the center frequency, lock range, phase detector, and divide-by-N modulus have been chosen, Eq. (1) yields the required clock frequency, and Eq. (5) yields the required K-counter modulus. Note that the loop lock range may have to be altered in order to set K equal to a power of two. Also note that setting the clocks equal (M = 2N) constrains the lock range to a maximum value of $\pm f_c/8$. If the chosen settings for M and K do not satisfy the ripple inequalities presented earlier ($K > M/4$ for EXOR, and $K > M/2$ for ECPD), the output signal will exhibit ripple. If such is the case, the user may elect to adjust M or K, or use a ripple cancellation circuit.

HIGHER ORDER DIGITAL PHASE-LOCKED LOOPS

A higher order analog PLL is typically constructed by inserting a filter in the PLL feedback loop. Higher order DPLLs can be constructed by cascading 'LS297 devices. An example of a second-order DPLL circuit configuration is illustrated in Figure 14, along with its associated control system representation.

The circuit shown in Figure 14(a) is composed of two first-order DPLLs which have been labeled Loop 1 and Loop 2. The overall DPLL center frequency and the Loop 2 center frequency are determined by the Loop 2 I/D clock. Since the Loop 1 I/D clock is connected to the I/D output of Loop 2, the Loop 1 center frequency will be determined by the frequency of the Loop 2 I/D output. A close inspection of Figure 14(a) reveals that if both loops are locked, the Loop 1 center frequency will be equal to the incoming frequency, f_{in}. This means the second-order DPLL will track its incoming signal with zero phase error within its lock range. The second-order DPLL lock range is determined by Loop 2:

$$\Delta f_{max} = \frac{Mf_c}{4K_2N} \quad Hz \tag{15}$$

The phase error ϕ_e, in Loop 2 is proportional to the difference in frequency between f_{in} and f_c:

$$(f_{in} - f_c) = \frac{k_{d2}\, Mf_c}{4K_2N}\ \phi_e \quad Hz \tag{16}$$

Frequency offset data may therefore be obtained by latching the contents of the Loop 2 feedback counter as described earlier for first-order DPLLs.

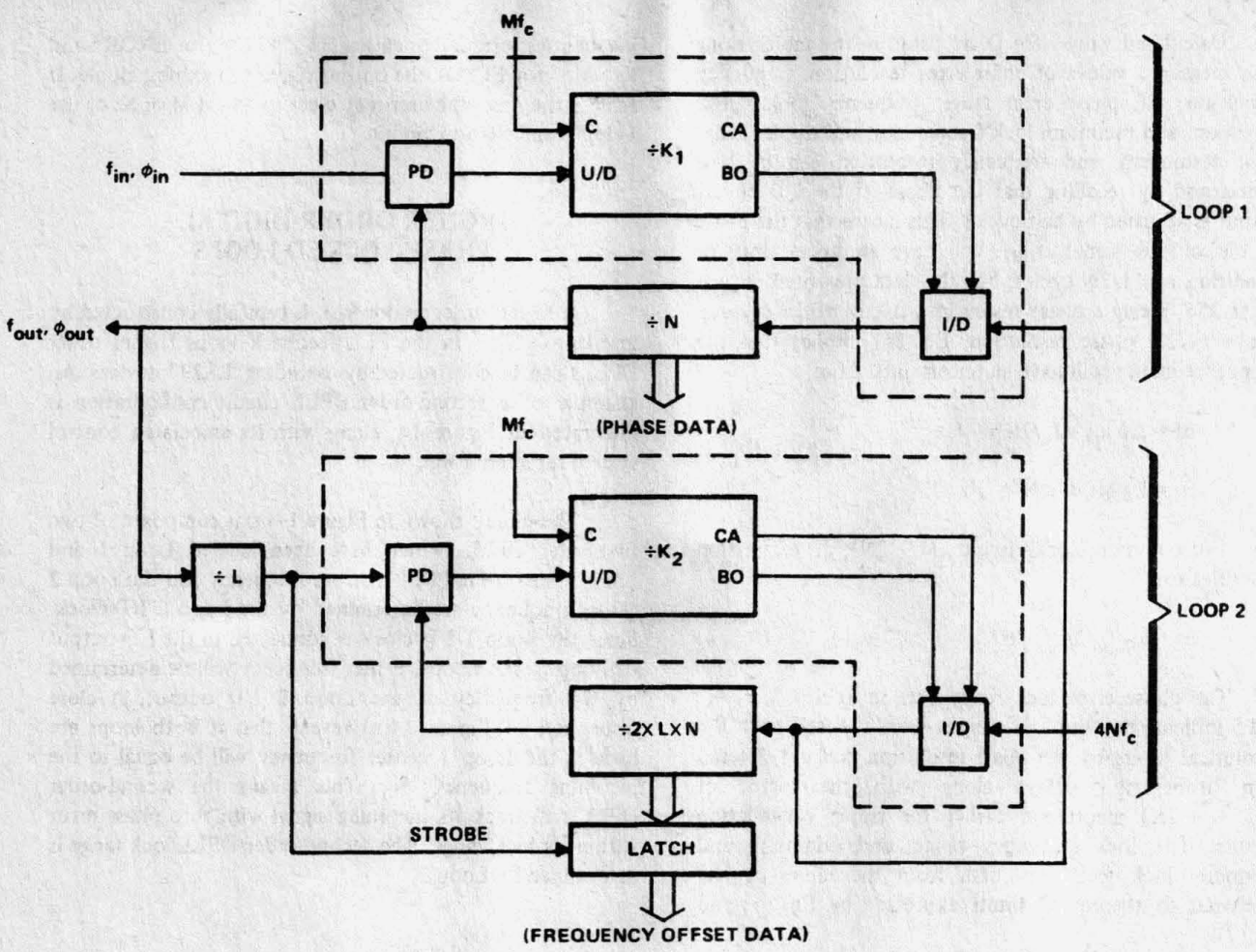
The transfer function for this loop can be shown to be:

$$H(S) = \frac{\phi_{out}(S)}{\phi_{in}(S)} = \frac{\omega_1 S + \omega_1\omega_2}{S^2 + \omega_1 S + \omega_1\omega_2} \tag{17}$$

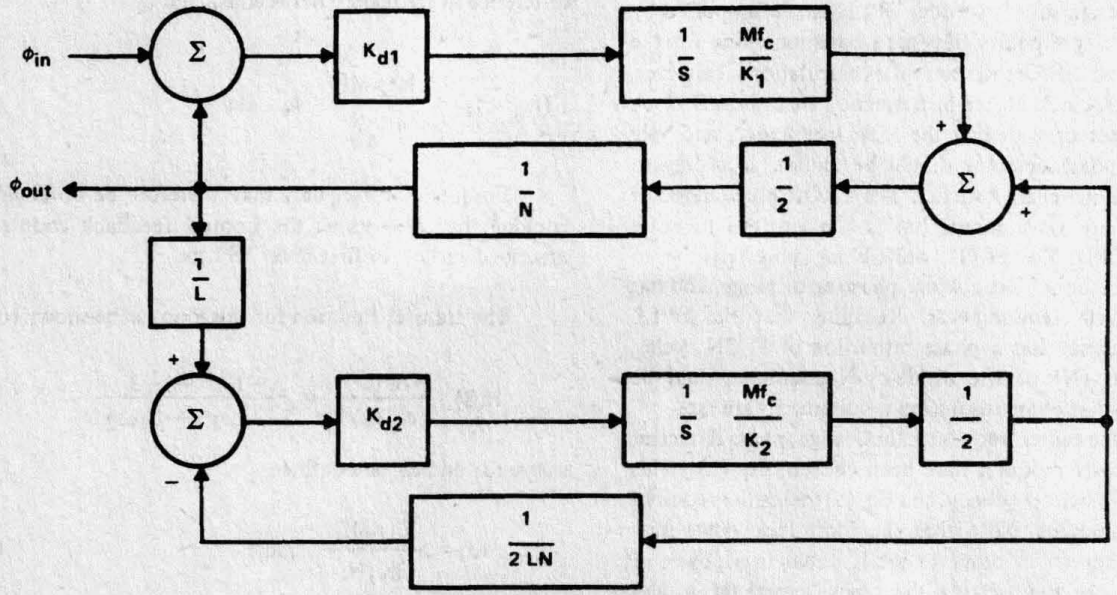
where ω_1 and ω_2 are defined:

$$\omega_1 = \frac{k_{d1}\, Mf_c}{2K_1N} \quad rad/s \tag{18}$$

$$\omega_2 = \frac{k_{d2}\, Mf_c}{4K_2LN} \quad rad/s \tag{19}$$



(a) BLOCK DIAGRAM



(b) CONTROL SYSTEM REPRESENTATION

Figure 14. Second Order DPLL

This can be compared to the general equation for a second-order, active filter analog PLL:

$$H(S) = \frac{\phi_{out}}{\phi_{in}} = \frac{2\zeta\omega_n S + \omega_n^2}{S^2 + 2\zeta\omega_n S + \omega_n^2} \quad (20)$$

where ω_n is the loop natural frequency and ζ is the damping factor. By equating (17) and (20), expressions for the natural frequency and damping factor of a second-order DPLL can be obtained:

$$\omega_n = (\omega_1\omega_2)^{1/2} \text{ rad/s} \quad (21)$$

$$\zeta = \frac{1}{2}(\omega_1/\omega_2)^{1/2} \quad (22)$$

Some of the effects of natural frequency and damping factor on loop performance have been presented in Reference 3.

Higher order DPLLs may be constructed in a similar manner by cascading.

SUMMARY

The operation of the 'LS297 has been presented as a basic building block in a digital phase-locked loop along with some ideas of how to extract phase data from the DPLL. A first-order DPLL may be constructed with one 'LS297 device, an external feedback counter, and an external clock. The accuracy of the DPLL is dependent upon the accuracy of the loop clocks, and loop center frequency and lock range are digitally programmable. A direct digital readout of phase information can be made available by latching the contents of the DPLL divide-by-N counter with a strobe of appropriate phase and frequency. Possible applications for the 'LS297 include motor speed control, noise filtering, tone recognition, data synchronization, frequency synchronization and multiplication, and position indicators, along with frequency and phase demodulation suggested earlier. The versatility of the DPLL can be greatly enhanced by the use of microprocessor control of lock range and center frequency.

REFERENCES

1. W. W. Lee, V. Harrington, Jr., and D. B. Cox, Jr., *A New Integrated-Circuit Digital Phase Locked-Loop,* Charles Stark Draper Laboratory Report P-148 (March 1975); reprinted in *IEEE Proc. National Aerospace and Electron. Conf.,* 377-383 (June 1975).

2. G. Gaugler, *Digital Phase Lock Loop Application Note,* Air Force Avionics Laboratory Internal Report, WPAFB (February 1977)

3. F. M. Gardner, *Phaselock Techniques, Second Edition,* (New York. John Wiley and Sons, 1979).

4. D. B. Cox, Jr., E. V. Harrington, Jr., W. H. Lee, and W. M. Stonestreet, "Digital Phase Processing for Low-Cost Omega Receivers," *J. Inst. of Nav.,* Vol. 22, No. 3 (1975).

5. J. D. Gallia, *Design of a Low-Power Schottky TTL High-Speed Digital Phase-Locked Loop Integrated Circuit,* Air Force Avionics Laboratory Technical Report, AFWAL-TR-80-1152;[(Dallas, Texas: Texas Instruments) Report 03-80-30] (October 1980).

General Design Considerations 1
Backplane Design 2
Device-Specific Design Aspects 3
5-V Logic Design 4
3.3-V Logic Design 5
Clock-Distribution Circuits (CDC) 6
Boundary-Scan IEEE Std 1149.1 (JTAG) Logic 7
Packaging 8
Index 9

Contents

	Page
ABT Enables Optimal System Design	4–3
Advanced High-Speed CMOS (AHC) Logic Family	4–21
Advanced Schottky Load Management	4–43
SN74CBTS3384 Bus Switches Provide Fast Connection and Ensure Isolation	4–83
Texas Instruments Crossbar Switches	4–91

ABT Enables Optimal System Design

SCBA001A
March 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**4–7**
Trends Important for Today's System Designer	**4–7**
Advanced Bus-Interface Logic (ABIL) as the System Bus Interface	**4–7**
Enablers to Continuous New-Product Development	**4–9**
What Is Advanced BiCMOS Technology (ABT)?	**4–9**
Fine-Pitch Packaging Shrinks ABT Device Size	**4–13**
ABT Products Provide End-Equipment-Specific Solutions	**4–15**
Summary	**4–19**

List of Illustrations

Figure	*Title*	*Page*
1	ABT Assumes Optimal Position	4–8
2	ABT Input/Output Circuit Structure	4–10
3	ABT Process Provides Consistency	4–11
4	Bus-Hold Circuit and Benefits	4–12
5	Fine-Pitch Package Options for ABT	4–14
6	ABT Products and Features	4–16
7	UBT™ Portfolio	4–17
8	LVT Provides Optimized 3.3-V I/O	4–18
9	Bus-Interface Evolution	4–19

EPIC-IIB, SCOPE, UBT, Widebus, Widebus+, and Shrink Widebus are trademarks of Texas Instruments Incorporated.
SuperSPARC is a trademark of SPARC International, Inc.

Introduction

As operating frequencies of microprocessors increase, the time allotted for memory access, arithmetic computation, or similar operations decreases. With this in mind, a new series of Advanced Bus-Interface Logic (ABIL) products developed with Texas Instruments (TI) submicron Advanced BiCMOS Technology (ABT) process assumes a prominent role as the key high-performance logic needed in today's workstation, personal and portable computer, and telecom systems. The goal of this family of products is to provide system designers a bus-interface solution combining high-drive capability, low power consumption, signal integrity, and propagation delays small enough to appear transparent with respect to overall system performance. Fine-pitch package options simplify layout, reduce required board space, and decrease overall system costs. Novel circuit-design techniques add value over competitive solutions.

Trends Important for Today's System Designer

Modern system designers face many complex challenges in meeting their design goals. The trends toward (need for) faster cycle times, lower power consumption, smaller footprints, greater reliability, and lower total system cost combine to put ever-increasing pressure on today's system designer.

The need for faster cycle time traditionally has been addressed by the microprocessor manufacturer. Clock and microprocessor frequencies have increased steadily with each succeeding product generation. The most advanced RISC processors in development are touting frequencies of about 200 MHz. For production systems, it is not unusual for processors to run on the order of 50 MHz and above. Increasing clock and microprocessor frequencies are now beginning to put pressure on surrounding memory and logic to make greater contributions in reducing overall system cycle times and improving overall system performance.

Higher-performance systems require the designer to focus on total system power requirements. Faster systems traditionally require more power, which often means more costly solutions. Power costs money to supply, and heat buildup due to this power costs money to remove. Also, excess power consumption adversely affects reliability due to the increase in the junction temperature of the silicon components. Lower-power devices reduce requirements for larger power supplies and high-cost cooling techniques, and could lead to smaller system packaging.

Occurring in parallel with demands for increased system performance and reduced system power consumption is demand to house systems in smaller cases, boxes, chassis, and cabinets. This miniaturization requires that each system component be optimally laid out in silicon, packaged, and mounted on the printed-circuit board (PCB).

Speed, power, size, cost, and reliability are all parameters by which system and end-equipment success are measured. Semiconductor manufacturers must be sensitive to these parameters and be able to provide well-defined and well-designed products to meet these needs.

Advanced Bus-Interface Logic (ABIL) as the System Bus Interface

Semiconductor vendors are required by system design houses to provide new products that are faster, consume less power, exist in smaller packages, and present a lower relative cost than their predecessors. Since the early 1970s, many different logic-product technologies have attempted to meet these demands.

Early logic-product technologies often forced the system designer to make tradeoffs. As shown in Figure 1, speed and power were the most typical design goals traded off. Solutions such as Schottky or HCMOS, respectively, offered high speed at the expense of low power or low power at the expense of high speed. In a typical system application, this logic technology is used between only a few system blocks, such as a simple 8-MHz processor, a slow 256K DRAM, and a local TTL bus. Their functional role was little more than small-scale integration (SSI) or medium-scale integration (MSI). Despite these shortcomings, early logic technologies thrived because they were inexpensive and readily available.

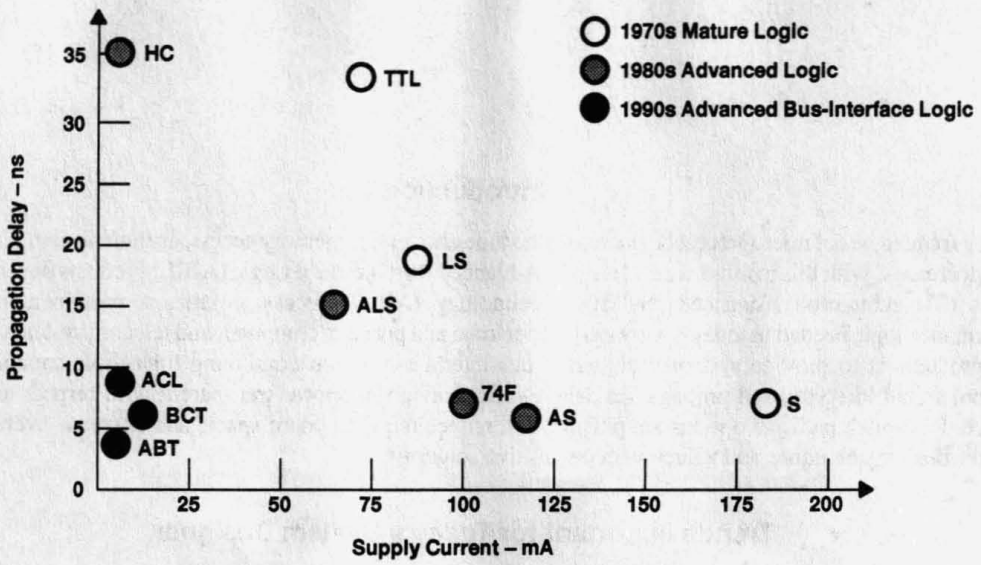


Figure 1. ABT Assumes Optimal Position

Cycle-time requirements for interface logic vary as a function of microprocessor and clock speed. In an 8-MHz system, the total system cycle available for completion of all operations is 250 ns. This can be roughly budgeted into 160 ns for the memory access, 45 ns for processor setup, and 45 ns for the interface logic (including signal propagation across PCB traces). With 45 ns available for interface, a forgiving, low-performance technology such as low-power Schottky or HCMOS can be utilized.

The situation changes dramatically when system speeds increase to 45 or 50 MHz. At 45 MHz, only 44 ns of total cycle time is available to complete all operations. Now, more expensive memories are needed with access times in the 20-ns range. Microprocessor setups can only be 8 ns. This leaves only 16 ns for interface and signal-trace propagation delay. The interface cycle time is a much higher percentage of the total system cycle time at 45 MHz than at 8 MHz.

As cycle-time requirements shrink, each nanosecond becomes critical in meeting the total system budget. The system designer has the option of using higher-performance memories, processors, or interface logic in squeezing additional nanoseconds out of the system delay. There is great demand for using interfacing logic to meet these budget needs because typically it is much less expensive for the designer to use than higher-performance memories or processors.

In light of decreasing total system cycle-time requirements, early logic technologies gave way to faster technologies. Significant gains made since the Schottky and HCMOS days result in products that no longer force the system designer into a tradeoff box. New-product development in the area of complex memories, processors, and ASICs has led the way for an equal, if not greater, acceleration in new-product development for advanced digital-logic products.

This development has propelled logic up from the ranks of *glue* status, used to fill in design gaps around the other major system blocks, to its new position as the system bus interface. ABIL products are now responsible for controlling the signals between the backplane buses and the other major system design blocks. They have become a major system design block in their own right, exerting significant influence over the performance of the final design.

In a modern-day system, ABIL products are likely to connect many major system design blocks, including application-specific parallel processors, 4M DRAMs, fast-cache SRAMs, and complex ASIC gate arrays/standard cells. The task of this new breed of advanced logic is to effectively transceive the address, data, and control signals of these integrated-circuit elements to and from heavily loaded TTL/CMOS/BTL system backplanes.

A wide variety of industry-standard and proprietary backplane specifications add to the difficulty of the task. At the low end of the scale, exhibiting data-transfer rates in the range of 10 to 20 Mbytes/s, are the PC-, AT-, and EISA-type buses. For midrange server and graphics-workstation applications, the 50- to 100-Mbytes/s data-transfer-rate range of Multibus II and microchannel-type buses is typical. High-end server and mainframe computer applications require the ≥ 100-Mbytes/s data-transfer rates of Futurebus+-type buses. Transceivers connecting to each of these backplanes must provide very high-drive current capability to effectively and reliably migrate signals across. ABIL products from TI uniquely address this need.

Enablers to Continuous New-Product Development

Reduction in minimum process dimension, enhanced value-added circuit design techniques, utilization of fine-pitch packaging, and incorporation of lower-power supply voltages are the most important enablers to continuous new development for logic products.

The minimum process dimension represents the width of the transistor-gate region and gives an indication of the switching speed of the transistor. In general, the smaller the minimum process dimension, the faster the transistors switch. An added advantage of reducing the minimum process dimension is the gain in gate density that can be achieved. A gain in gate density results in increased device functionality without a corresponding increase in silicon die area. Currently, state-of-the-art high-volume-production logic processes consider a 0.8-μm minimum process dimension. However, work is ongoing to prototype more advanced processes characterized by 0.6-, 0.5-, and 0.35-μm minimum process dimensions.

Enhanced value-added circuit-design techniques greatly increase the functionality of a logic device as well as improve its performance. These techniques often eliminate the need for the designer to utilize discrete components such as resistors, capacitors, and diodes because these are built into the silicon device itself. Additionally, optimizations in I/O or core circuitry can positively affect speed and power performance.

An aggressive drive exists to convert classic through-hole package approaches to totally above-board surface-mount approaches. Occurring in parallel is a drive to upgrade existing surface-mount packages with finer pin-to-pin pitches so as to minimize total package area. However, with smaller packages comes increased reliance on thermal-management techniques. The increased difficulty in removing heat from the smaller packages can preclude the use of inexpensive plastic packages. The need for ceramic or other alternatives would act to drive up design costs.

Finally, system designers are beginning to drive the semiconductor industry to move below 5 V as the baseline for power supplies. The migration to lower voltages, such as 3.3 V, enhances the reliability of advanced process technologies exhibiting minimum process dimensions of 0.6 μm or lower. The need for low-voltage memory and processor product interface, lower device-generated noise levels, lower power consumption, and increased battery life for unregulated portable systems accelerate the demand for 3.3-V logic. New 3.3-V logic opportunities will emerge as system designers continue to rely on advanced process technologies.

What Is Advanced BiCMOS Technology (ABT)?

Advanced BiCMOS Technology (ABT) is available today in products from TI to aid designers doing high-performance bus management. It is currently available in many different product options, including 8-bit octal, 16-, 18-, and 20-bit Widebus™, and 32- and 36-bit Widebus+™ versions.

At TI, ABT evolved from an earlier 1.5-μm BiCMOS process. It was designed to provide speeds equivalent to existing advanced bipolar solutions but with 90% less device power. This standard BiCMOS process introduced high-performance, lower-power, bus-interface products to the marketplace two years ahead of the nearest competitor. Since its bus-interface introduction in 1987, TI has utilized BiCMOS and advanced BiCMOS in products such as mixed-signal integrated circuits, high-performance gate arrays, high-speed cache tags, and application-specific processors such as the SuperSPARC™.

ABT employs a submicron 0.8-μm minimum process dimension. It combines elements of both bipolar and CMOS circuit/process technologies onto a single silicon chip. ABT offers the system designer the best combination of high speed, high drive, and low power consumption in the industry. As shown in Figure 1, ABT provides a performance point closer to the origin of the speed/power graph than any other logic technology available. Specifically, ABT is based on a CMOS core-circuit structure with an NPN bipolar output transistor module added. This means adding about four additional masks to the CMOS process. The current single NPN transistor output structure of ABT has been optimized for 5-V operation.

Simplified input and output stages of an ABT transceiver are shown in Figure 2. The inputs are designed to offer TTL-compatible levels with guaranteed switching between a V_{IH} minimum of 2 V and a V_{IL} maximum of 0.8 V. These inputs are implemented with CMOS circuitry; therefore, they offer characteristic high impedance for low leakage and low capacitance for minimal bus loading. The CMOS supply voltage of the input stage is dropped by diode D1 and transistor Q1, centering the threshold around 1.5 V. When inputs are in the low state, Q_r raises the voltage of source Q_p up to the rail, ensuring proper operation of the feedback stage. This stage provides about 100 mV of input hysteresis, increasing noise margins and reducing oscillations.

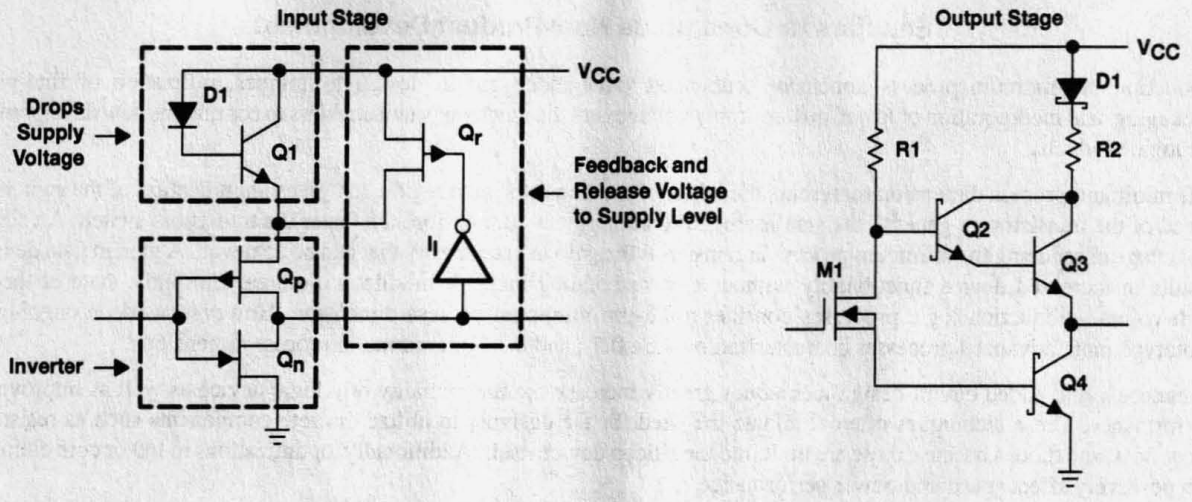


Figure 2. ABT Input/Output Circuit Structure

ABT outputs utilize bipolar circuitry to provide the high speed and drive necessary for a bus interface. A major advantage of using bipolar circuitry in the output stage is the reduced voltage swing, which lowers ground noise, improves signal integrity, and reduces dynamic power consumption. In Figure 2, M1 acts as a current switch that drives the outputs low when conducting current from R1 through to the base of Q4. The base of Q2 is pulled low, turning off the upper output. For a low-to-high output transition, M1 turns off and current through R1 charges the base of Q2. As Q2 goes high, the Darlington pair, Q2 and Q3, turns on. With its supply of base current now cut off, Q4 turns off and the output transition switches low to high. R2 limits output current in the high state and D1 is a blocking diode preventing current flow in power-down applications.

By virtue of its small minimum process geometry, tight metal pitch, and shallow junctions, ABT can provide strong output drive currents (sink currents specified at 64 mA and source currents specified at 32 mA) and low parasitic capacitances. As a result of these enhancements, internal propagation delays are very fast and very well behaved. Figure 3 shows that typical propagation delays are on the order of 2–3 ns across the operating temperature range. This excellent consistency allows ABT to be specified over the industrial temperature range of –40°C to 85°C. Figure 3 also shows that ABT performance is very well behaved across capacitive load and multiple-output switching conditions.

Maximum propagation delays for ABT are as low as 4–5 ns, depending on the device type and propagation path. Table 1 compares the data sheet maximums of several ABT 16-bit Widebus™ transceiver devices with competing FCTB/C CMOS and 74F/ALS bipolar solutions. It is clear from both Figure 3 and Table 1 that ABT is the system designer's best choice for bus-interface applications that require consistent speed performance for many different conditions.

From a power (current) consumption standpoint, the use of bipolar in the output stage is advantageous for two reasons. First, the voltage swing is less than that of a CMOS output. The power consumed when charging or discharging internal circuit capacitances and the external load capacitance is reduced. Second, the bipolar transistors are capable of turning off more efficiently than CMOS transistors. The wasteful flow of current from V_{CC} to GND is reduced. Although bipolar does tend to have a high static power consumption, its lower dynamic power consumption allows for better overall power performance at high frequencies than either pure bipolar or CMOS. This is because the dynamic power component makes up the majority of a device's overall power consumption.

The ABT maximum high-impedance supply currents (I_{CCZ}) range from about 50 μA for 8-bit octals to about 2–3 mA for 16-bit Widebus™ products. Maximum dynamic supply currents (I_{CCL}) range from about 30 mA for 8-bit octals to about 34 mA for 16-bit Widebus™ products. Power on demand, an enhanced circuit design improvement to the bipolar output stage on new ABT product families, reduces dynamic current consumption levels by up to 50%. High-impedance and dynamic supply-current goals for the new 32-/36-bit Widebus+™ family are 500 μA and 60 mA, respectively.

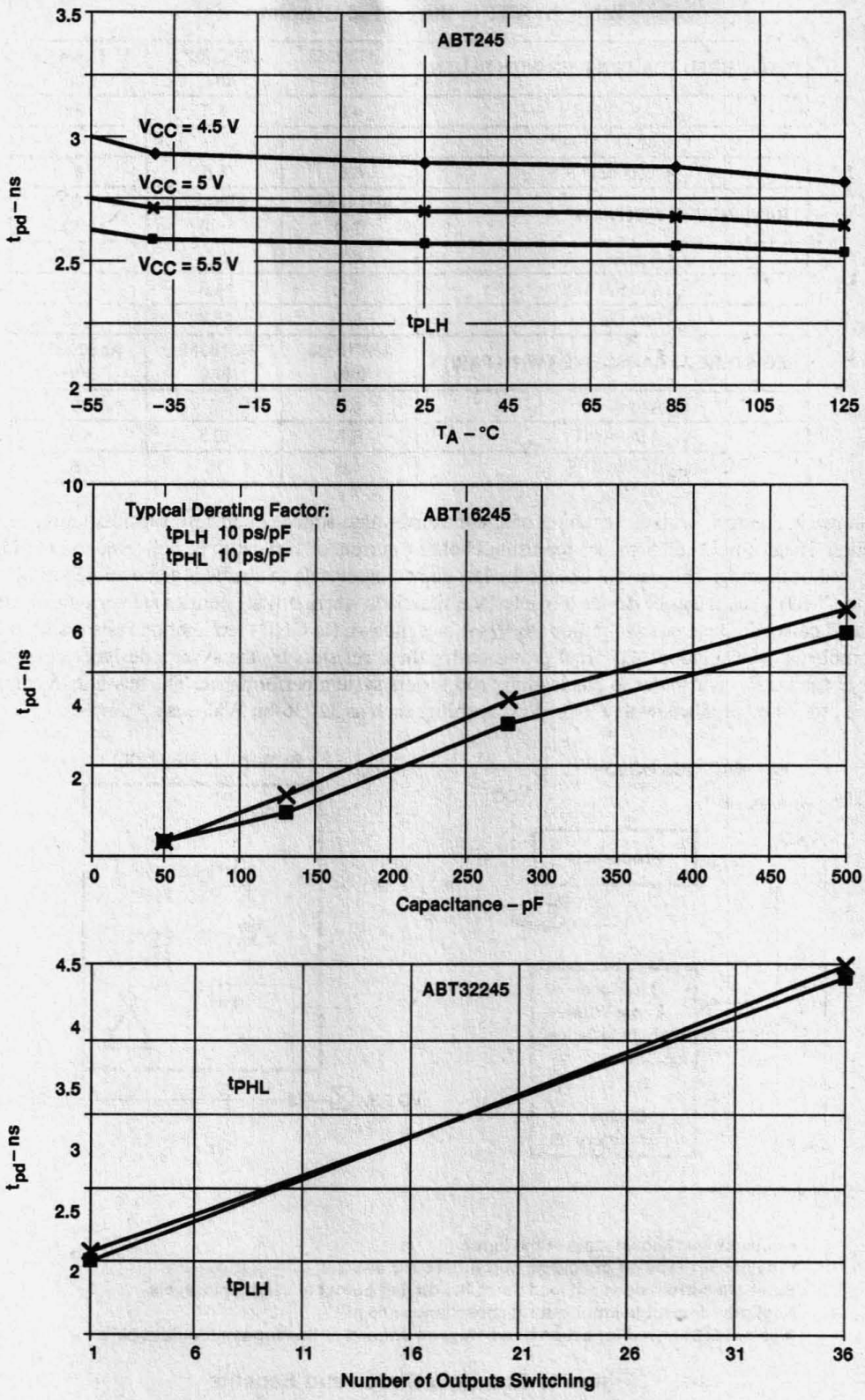
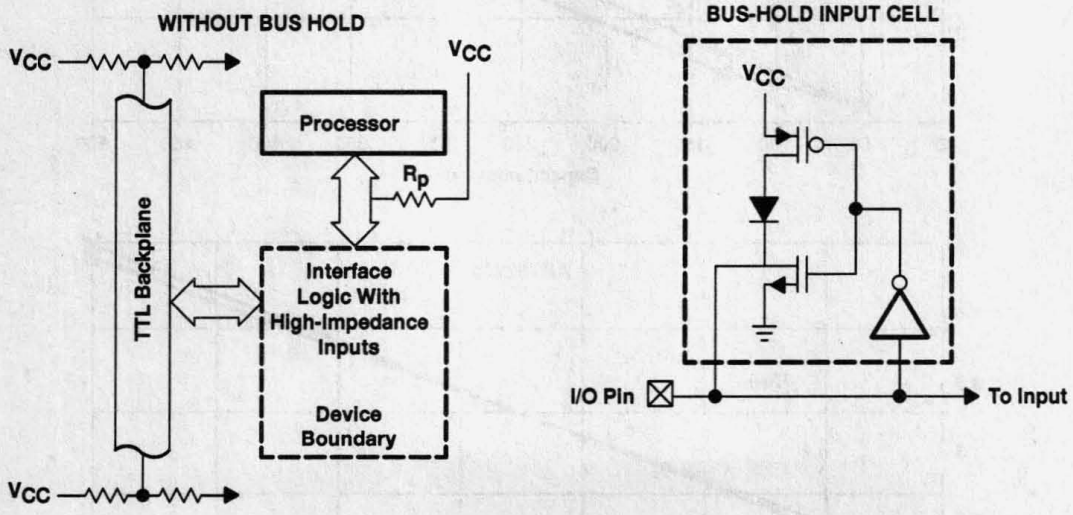


Figure 3. ABT Process Provides Consistency

Table 1. ABT Is the Speed Benchmark

REGISTERED TRANSCEIVER WITH CLKEN	ABT16952 (ns)	29FCT52C (ns)	F2952 (ns)
t_{pd} CLK to A/B	4.5	6.3	9
$t_{pd(en)}$ $\overline{OE}$ to A/B	6	7	10
$t_{pd(dis)}$ $\overline{OE}$ to A/B	5.5	6.5	9
TRANSCEIVER WITH PARITY	**ABT16657 (ns)**	**ABT657 (ns)**	**F657 (ns)**
t_{pd} A to B	4.3	5.5	8
t_{pd} A to PARITY	6.7	11.3	16
t_{pd} B to $\overline{ERR}$	6.7	15.7	22.5
REGISTERED TRANSCEIVER WITH PARITY	**ABT16833 (ns)**	**FCT833B (ns)**	**ALS29833 (ns)**
t_{pd} A to B	4.3	7	10
t_{pd} A to PARITY	6.7	10.5	15
t_{pd} CLK to $\overline{ERR}$	4.6	15	16

Bus hold, as shown in Figure 4, is another example of an enhanced, value-added circuit design technique available on new ABT product families. The bus-hold cell provides for a small holding current of 100 µA to be delivered to I/O pins configured as inputs left unused or floating. This current latches the last known input state to a valid logic level. Floating input conditions are common to CMOS backplanes or device bus-interface situations where driving entities are periodically required to be in 3 state. Bus-hold cells eliminate passive pullup (to V_{CC}) or pulldown (to GND) termination resistors necessary to prevent application problems or oscillations. External provision for these resistors by the system designer consumes board area, increases bus capacitance, contributes to bus loading, and lowers system performance. The bus-hold feature is particularly effective when offered on products with a lot of I/O capability such as 32-/36-bit Widebus+™ devices.



- **Holds the last known state of the input**
- **Provides for ±100 µA of holding current at 0.8 V and 2 V**
- **Bus-hold current does not load down the driving output at valid logic levels**
- **Negligible impact to input/output capacitance (0.5 pF)**
- **Eliminates the need for external resistors on unused or floating input/output pins**

Figure 4. Bus-Hold Circuit and Benefits

Fine-Pitch Packaging Shrinks ABT Device Size

As the push for smaller system sizes becomes intense, the system designer will require the logic manufacturer to house high-performance silicon in increasingly smaller packages. Most notably, the system designer has been leveraging the advantages of plastic-leaded chip carriers (PLCCs) and small-outline integrated circuits (SOICs).

Both PLCC and SOIC packages provide a gull-wing lead profile. Both utilize 1.27-mm pin-to-pin pitch spacing. The reduced pitch offers a major space improvement over bulky plastic dual-in-line (PDIP) through-hole packages. The major difference between PLCC and SOIC is philosophical. The PLCC has pins on all four sides (arranged either in square or rectangular configuration) while the SOIC has pins on only two sides (arranged in flow-through configuration).

In spite of the advantages of PLCC and SOIC, system designers are beginning to specify surface-mount packages with finer pitch values to keep their end equipments competitive in the marketplace or to avoid falling behind more aggressive rivals. Such fine-pitch versions available in volume today offer improvements in the pin-to-pin pitch down to 0.635 mm. More advanced fine-pitch alternatives exhibiting characteristic pitches of 0.5, 0.4, and 0.3 mm are on the horizon.

The plastic quad flat package (PQFP) is a fine-pitch version of the PLCC package. It offers a 0.635-mm pitch and is widely used for microprocessors, ASICs, or other custom devices. The 44-pin PQFP is the smallest used in volume, while the largest versions provide over 200-pin capability. However, for the system designer using ABIL products, it is advantageous to combine the fine-pitch capability of the PQFP with the two-sided dual-in-line design of the SOIC.

SOICs have evolved in two distinct paths to meet this need. The first path considers reducing the surface area and pin pitch of the package while keeping the pin count and bit density constant. The second path considers increasing the bit density of the package by increasing pin count and reducing pin pitch. Figure 5 clearly shows both of these migratory paths starting from the standard octal SOIC package in the upper left corner.

Package size reductions are shown from top to bottom in Figure 5, with each succeeding reduction occupying a new row at constant bit density and pin count. Bit-density and pin-count increases are shown horizontally across Figure 5.

There are five new fine-pitch packages represented in Figure 5. Four of these offer a density-upgrade path for the SOIC. The fifth is a new package offering a density upgrade for the PQFP. All of these packages were developed and standardized exclusively for high-performance ABIL ABT products by TI.

The shrink small-outline package (SSOP) is available in two worldwide standard form factors. The first, approved by the Joint Electronic Device Engineering Council (JEDEC), allows for 16-, 18-, or 20-bit I/O functions in a package roughly the same size as the octal SOIC. The pin pitch for the JEDEC SSOP is 0.635 mm. The JEDEC SSOP is available in a 48-pin version for the basic 16-bit driver and transceiver functions and in a 56-pin version for complex 16- to 20-bit transceiver functions. The very popular ABT Widebus™ family uses the JEDEC-approved SSOP.

The second form factor, approved by the Electronics Industry Association of Japan (EIAJ), allows for 8- and 9-bit I/O functions in a package about 40% of the size of the octal SOIC. The pin pitch for the EIAJ SSOP is 0.65 mm. The EIAJ SSOP is available in a 20-pin version for basic ABT 8-bit driver and transceiver functions and in a 24-pin version for complex ABT 8- and 9-bit transceiver functions.

The bottom row of Figure 5 represents the third form-factor upgrade to the SOIC available from TI. The thin shrink small-outline package (TSSOP) is EIAJ approved and offers a reduced thickness (height) specification of 1.1 mm. The pin pitch of the EIAJ TSSOP is 0.65 mm (the body width is 4.4 mm). The TSSOP is compatible with Type I and Type II card physical requirements of the Personal Computer Memory Card International Association (PCMCIA). TSSOP offers the smallest package size available for 20- and 24-pin drivers and transceivers. For denser memory arrays, TSSOP facilitates front and back side mount in under 3.3-mm thickness specified by PCMCIA if card thicknesses are kept under 1 mm.

For wide-word applications with extreme space and height restrictions, TI offers Widebus™ devices in a new package called the Shrink Widebus™. Available in 48- and 56-pin versions, this new package has a 1.1-mm maximum height, a 6.1-mm body width, and a 0.5-mm lead pitch. The Shrink Widebus™ package, developed by TI, is registered with the EIAJ, meets the requirements of the PCMCIA, and occupies 40% less board area than the standard JEDEC SSOP.

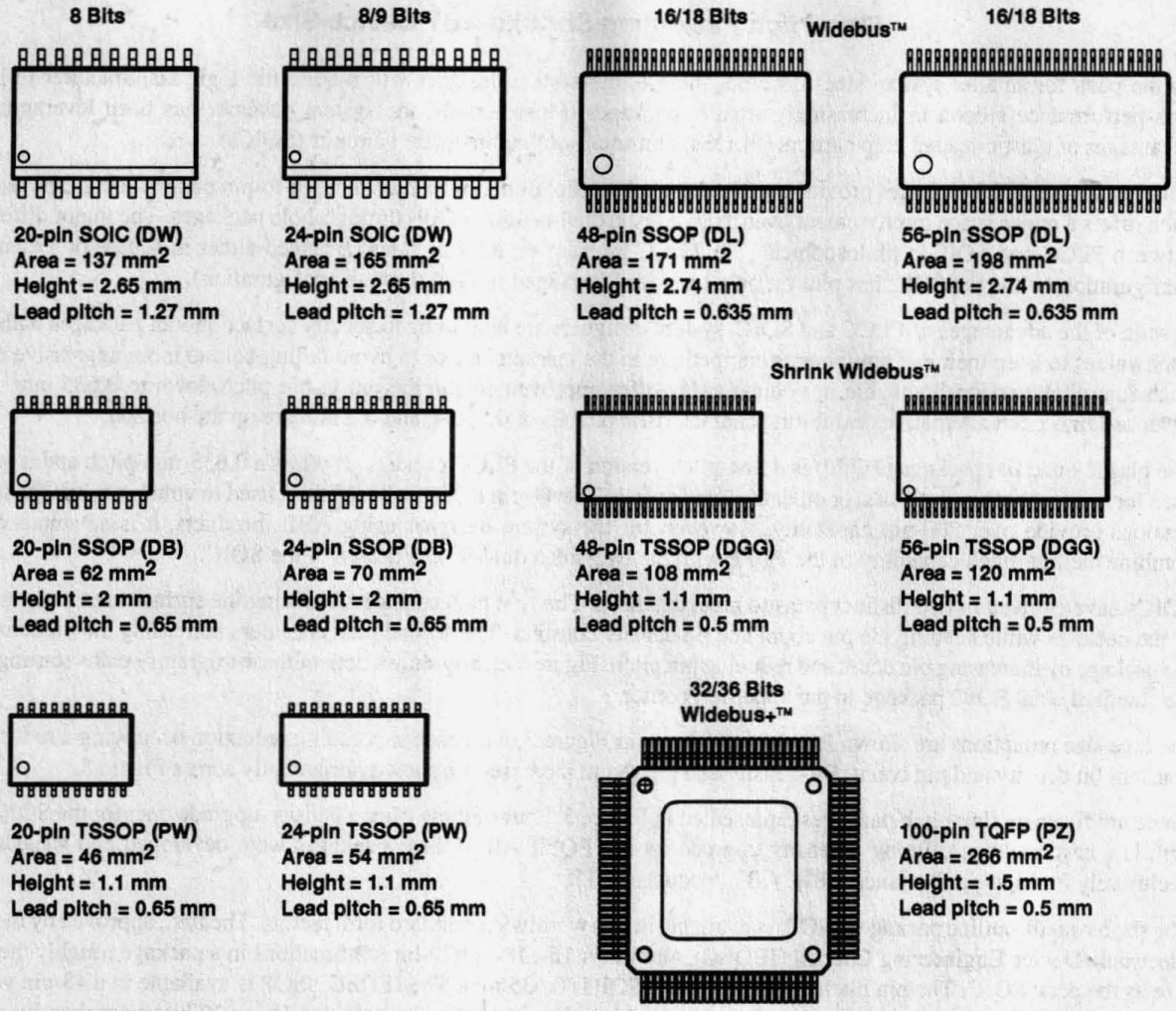


Figure 5. Fine-Pitch Package Options for ABT

The EIAJ thin quad flat package (TQFP) provides the density upgrade path for the PQFP. This 100-pin package allows single-chip 32- and 36-bit I/O solutions in over 50% less area than with octal SOIC connections. The pin pitch for the EIAJ TQFP is 0.5 mm, which is the smallest in production today. The reduced pitch of the TQFP offers a 35% area reduction over 100-pin PQFP solutions. The new 32- and 36-bit ABT Widebus+™ family, announced at the BUSCON '92 West trade show in Long Beach, California, uses the 100-pin TQFP.

All of the fine-pitch package options are superior for space-saving applications. The JEDEC SSOP and EIAJ TQFP are superior in several other areas as well. The JEDEC SSOP incorporates a flow-through architecture where input and output pins each have their own dedicated side of the package. Flow-through pinouts offer the system designer a very easy route path for signal traces.

A standard SOIC octal package can afford only one GND pin for every eight I/Os. This ratio improves to 2:1 and 3:1 for JEDEC SSOP and EIAJ TQFP, respectively. Both the JEDEC SSOP and the EIAJ TQFP provide multiple V_{CC} and GND pins distributed along the sides. The larger number of GND pins and distribution of these pins results in less noise and allows for less propagation delay than octal functions. As a result, ABT octals, ABT Widebus™, and ABT Widebus+™, all typically exhibit less than 1 V of noise, even though the maximum number of switched outputs increases from 8 bits to 18 bits to 36 bits with each respective family.

As package area decreases, the thermal impedance of the package to the ambient environment increases. Thermal impedance represents the ability of a package to dissipate heat. The higher the thermal impedance, the more difficulty the package has in dissipating heat. The higher thermal impedances of fine-pitch packages require additional attention and care from the system designer. Proper thermal management techniques as well as proper power dissipation guidelines must be used to ensure operation. Fortunately, the low power of ABIL ABT products is more conducive to a fine-pitch packaging approach than competitive CMOS solutions.

ABT Products Provide End-Equipment-Specific Solutions

Combining previously discussed state-of-the-art elements of the ABT process with its numerous advanced fine-pitch package options and enhanced circuit-design features yields a very impressive portfolio of new products. These new products effectively serve the distinct needs of the workstation, personal and portable computer, and telecom end-equipment markets.

Table 2 categorizes the entire ABIL product spectrum built with the ABT process technology. These families offer features and benefits dedicated to specific markets and industry standards. Figure 6 shows the relationships of these features and benefits.

Table 2. ABT Products and Features

NAME	EXAMPLE PART NUMBER	KEY FEATURES	NO. OF BITS	PACKAGES	MAX PROP DELAY (ns)	I_{CCZ} (mA)	I_{OL} (mA)	I_{OH} (mA)	TARGET APPLICATIONS
ABT	SN74ABT245A	0.8-µm process, –40°C/85°C	8, 9, 10	DIP, SOIC, SSOP (EIAJ), TSSOP	3.6	0.25	64	32	High-speed bus interface, PC, EWS, telecom
ABT Widebus™	SN74ABT16245A	Flow-through pinouts, low noise	16, 18, 20	SSOP (JEDEC), TSSOP	4.0	0.19	64	32	Higher performance, space-conscious applications
ABT Widebus+™	SN74ABT32245	Bus-hold cell, power on demand	32, 36	TQFP (EIAJ)	5.2	2	64	32	Single-chip 32-bit interface
IWS Drivers	SN74ABT25245	Enhanced output drivers	8	DIP, SOIC	4.3	0.5	188	96	25-Ω incident-wave switching
Memory Drivers	SN74ABT2245	Series output-damping resistors	8, 10, 11, 12, 16	DIP, SOIC, SSOP (EIAJ), SSOP (JEDEC)	4.5	0.25	12	12	Low noise, high-reliability driving, memory interface
Futurebus+	SN74FB2031	BTL port, 2-ns minimum edge rate	8, 9, 18	PQFP, SSOP (JEDEC), TQFP (EIAJ)	7.6	10	100	3	IEEE 896.1 backplane interface
BTL Drivers	SN74FB2033A	BTL-TTL-level translation	8, 9	PQFP, SSOP (JEDEC)	6.1	10	100	3	IEEE 1194.1 backplane interface
SCOPE™	SN74ABT8245	Testability, built-in self-test	8, 16, 18	DIP, SOIC, SSOP (EIAJ), SSOP (JEDEC), TQFP (EIAJ)	4.7	0.05	64	32	IEEE 1149.1 backplane interface
LVT	SN74LVT245B	3.3-V V_{CC}, mixed mode, bus hold	8	SOIC, SSOP, TSSOP	4	0.19	64	32	Battery portables, notebook computers, POS terminals
LVT Widebus™	SN74LVT16245A	3.3-V V_{CC}, mixed mode, bus hold, power on demand	16, 18	SSOP (JEDEC), TSSOP	4.1	0.19	64	32	Workstations, portable computers

For high-performance engineering workstation and server markets, the ABT Widebus™ and Widebus+™ families provide the highest integration and performance. They are necessary to connect the most demanding CISC/RISC microprocessors to the most heavily loaded, high-frequency backplanes.

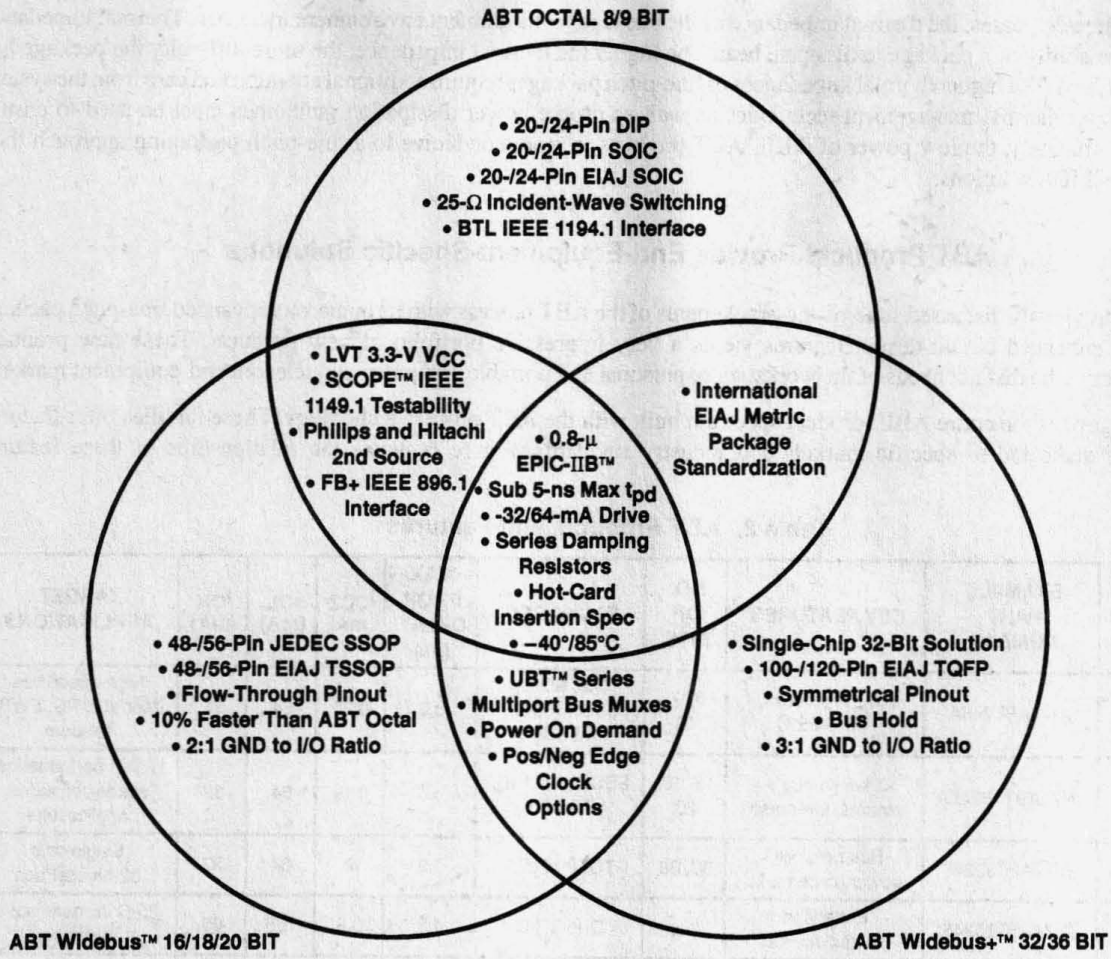


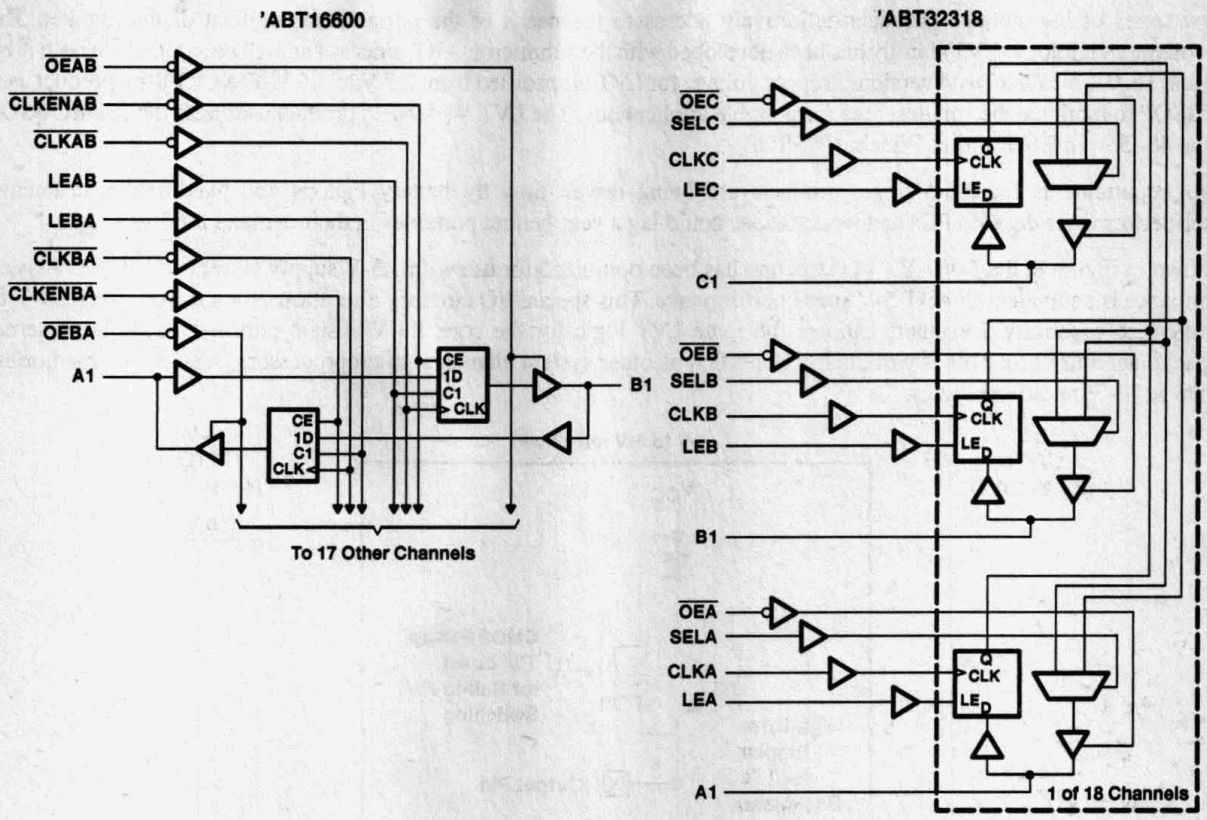
Figure 6. ABT Products and Features

The Universal Bus Transceiver (UBT™) is unique in the industry because it can be operated in several distinct bus-interface modes. Each package contains D-type latches and flip-flops. Flexible control-logic options provide for output-enable, latch-enable, clock, and clock-enable combinations.

UBT™s can be configured as transparent, data-flow-through transceivers (like the dedicated '245 function), latch-enabled transceivers (like the dedicated '543 function), clocked registered transceivers (like the dedicated '646 function), and clock-enabled registered transceivers (like the dedicated '952 function). Workstation designers can minimize inventory and procurement requirements, costs, and overhead with UBT™ flexibility. Designed specifically for workstation bus-interface applications, the UBT™ is perfect as an interface to the many different microprocessor architectures and system backplane specifications available.

Figure 7 details the current UBT™ portfolio from TI and includes block diagrams for two devices in the series. The 'ABT16600 is an 18-bit UBT™ packaged in the 56-pin SSOP package. It can be configured in each of four different data-flow modes between its A port and B port.

The 'ABT32318 is an 18-bit multiplexed UBT™ that can be configured in each of three different data-flow modes between its A port, B port, and C port. This UBT™ allows the system designer multiple combinations for real-time and stored data exchanges between the three ports. It is particularly useful for multibus communication, multiway interleaving memory applications, and high-performance, multiplexed-address and data-bus interface.



SERIES	NO. OF BITS	NO. OF PORTS	PACKAGE	NO. OF PINS	PARTITIONING	CONTROL LOGIC			
						OE	LE	CLK	CLKEN
16500/1	18	2	SSOP, TSSOP	56	× 18	Yes	Yes	Yes	No
16600/1	18	2	SSOP, TSSOP	56	× 18	Yes	Yes	Yes	Yes
32316	16	3	TQFP	80	× 16	Yes	Yes	Yes	Yes
32318	18	3	TQFP	80	× 18	Yes	Yes	Yes	No
32501	36	2	TQFP	100	× 18	Yes	Yes	Yes	No

Figure 7. UBT™ Portfolio

Several ABT product families directly address upper-end workstation and server equipment. A series of transceivers compliant with the IEEE 896.1 Futurebus+ backplane-interface standard are available. The special Futurebus+ protocols dictate special electrical requirements of the transceivers to ensure proper connection to Futurebus+ backplanes. Each of seven transceivers in the series utilize backplane transceiver logic (BTL) switching levels in accordance with the Futurebus+ standard. Complementing these Futurebus+ transceivers is a series of BTL transceivers compliant with the IEEE 1194.1 standard. Both transceiver series contain a TTL A port along with the BTL B port and can perform TTL-to-BTL and BTL-to-TTL-level translation.

SCOPE™ transceivers and drivers are available in ABT, which are compliant with the IEEE 1149.1 testability standard. For high reliability and fault-tolerant system needs, these devices provide their own internal self-test capabilities. A complete line of SCOPE™ hardware and software system products have been developed by TI.

The personal-computer market is characterized by very short design cycle times and intense pressure to lower costs. The major driving force is the need for workstation-type performance in machines designed for desktop, home, and portable applications. ABT in fine-pitch package options meets these needs nicely.

A new series of low-voltage products definitively addresses the needs of the portable subsegment of this market. The low-voltage technology (LVT) family has been developed with the submicron ABT process and will be available in both 8-bit octal and 16-/18-bit Widebus™ versions. Supply voltage for LVT is specified from 2.7 V to 3.6 V. The LVT 8-bit product uses the TSSOP to facilitate the smallest area for portable applications. The LVT Widebus™ product uses both the JEDEC SSOP and the 48-/56-pin EIAJ Shrink Widebus™ SSOP.

Market requirements for 3.3-V logic products are being driven now by battery laptops and hand-held instruments. Higher-performance desktop PCs and workstations could lag a year behind portables in their demand for 3.3-V logic.

As shown in Figure 8, the 5-V ABT I/O structure has been optimized for use with 3.3-V supply currents. LVT 3.3-V speed performance is equivalent to ABT 5-V speed performance. This special I/O circuitry also allows for a *mixed-mode* 3.3-V to 5-V interface capability. Designers can use the same LVT logic for the core 3.3-V system partition as for the external 5-V backplane interface. This is particularly important as other system elements (microprocessors, ASICs, and memories) migrate to 3.3 V at different rates.

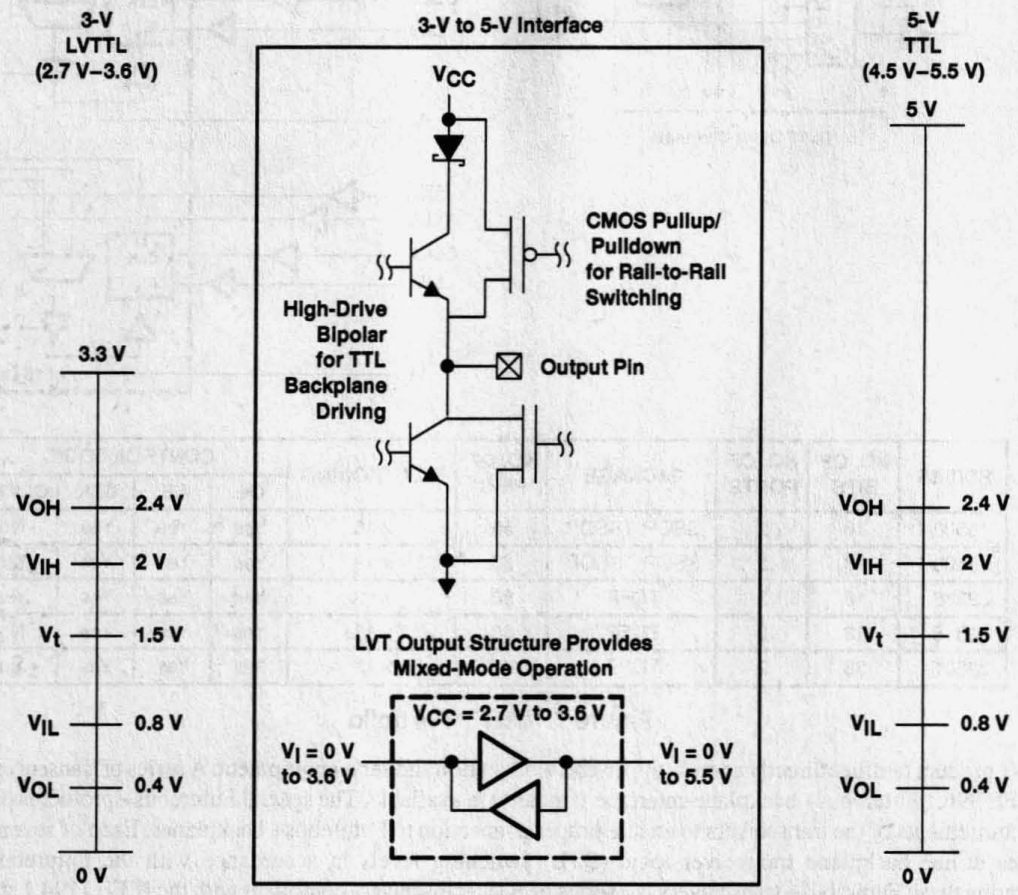


Figure 8. LVT Provides Optimized 3.3-V I/O

LVT I/O circuitry provides multiple output-current ratings for multiple system requirements. LVT devices are specified to drive at rail-to-rail low-voltage CMOS levels and standard 5-V TTL levels. LVT employs bus-hold and power-on-demand circuits increasing reliability, decreasing discrete component count, and minimizing enabled and disabled static power consumption. Maximum I_{CCL}, I_{CCH}, and I_{CCZ} current specifications are 5 mA, 0.1 mA, and 0.1 mA, respectively.

The majority of traditional telecom end equipments can be divided into switching and transmission categories. Switching equipment, such as central offices, cross connects, and branch exchanges, are analogous to large mainframes or supercomputers. ABT octal and Widebus™ product families are targeted for these telecom equipments.

For transmission equipment, such as line cards, bridgers, and routers, products with enhanced data-sheet specifications covering hot-card insertion and power up/down are required. In these applications, a board (card) typically is removed (inserted) from an active (hot) system for upgrade, maintenance, or repair. The additional specifications characterize the device's performance when supply currents change (ramp) rapidly.

It is necessary to know how the device behaves when V_{CC} is 0 V, when V_{CC} is at the rail (5.5 V), and when V_{CC} ramps between these voltages. To address this requirement specifically for telecom transmission applications, ABT transceiver data sheets take into account I_I, I_{OZH}, I_{OZL}, and I_{OZ} current conditions for various V_{CC} ramp rates. Transmission-system designers can then profile ABT device performance in hot-card insertion and power up/down conditions.

Summary

TI provides the system designer with the most advanced products to date, aiding the solution of complex design challenges. Advanced bus-interface logic (ABIL) products processed in submicron advanced BiCMOS technologies (ABT) address specific end-equipment demands of the workstation, personal and portable computer, and telecom markets. Advanced fine-pitch package options, such as SSOP, TSSOP, and TQFP, offer space-saving form factors. Circuit design techniques, such as bus hold and power on demand, add value over competitive solutions.

The evolutionary development of process and package technologies is illustrated in Figure 9. Solid lines indicate process-technology migration for CMOS and BiCMOS. The minimum process dimension is represented on the ordinate in units of microns. The dashed line indicates package-technology migration from PDIP to SOIC to SSOP to TQFP. For the dashed line, the ordinate represents minimum lead pitch in millimeters.

Figure 9 shows some interesting trends. BiCMOS solutions, initially well behind their CMOS cousins in terms of performance, have closed the gap almost completely during the past six years. For 5-V logic applications, ABT offers significant advantages over an equivalent CMOS version, particularly with the advent of thermally enhanced fine-pitch packages like the TQFP.

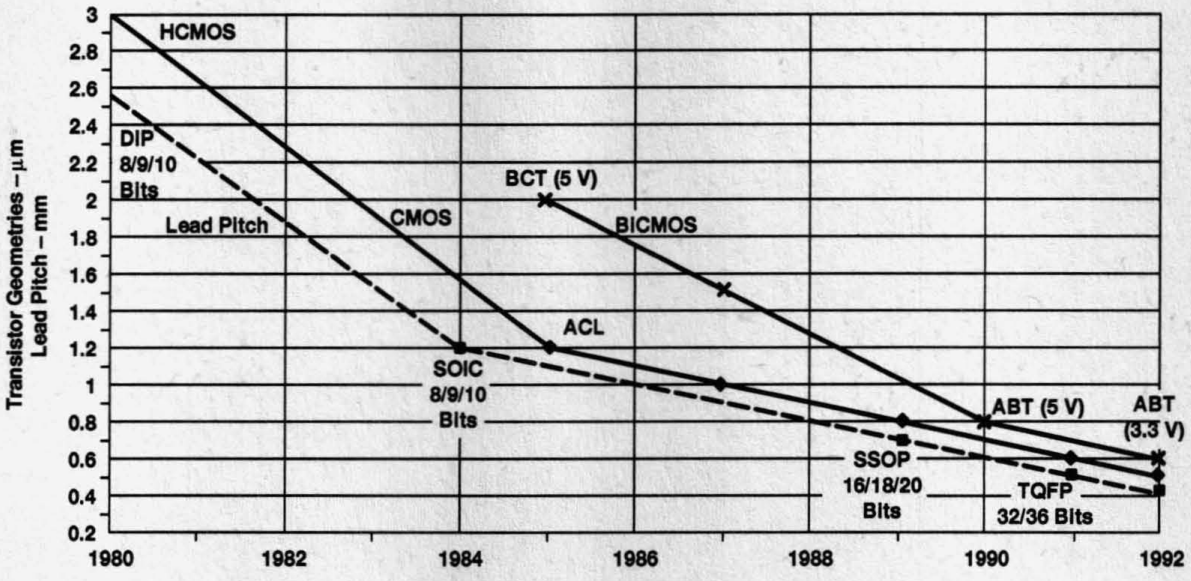


Figure 9. Bus-Interface Evolution

The advanced BiCMOS opportunity is to provide more processing capability and overall throughput at a time when the next-generation CMOS technologies are not quite ready, or where a mixed-technology approach provides a more practical solution. For ABIL products, the high performance and drive capability of ABT are necessary for rack-mount supercomputers, workstations, and telecom switching equipment. However, the low power consumption of ABT is necessary if these end equipments are to migrate to the desktop.

As process geometries drop to 0.6 µm and below, advanced BiCMOS and advanced CMOS will continue to compete in the pursuit of the best low-voltage solutions. Future enhancements to advanced BiCMOS might include extensions to a complementary structure of NPN and PNP transistors to better cope with reduction in power-supply voltages. As supply voltages drop to 2.6 V and below, it appears likely that advanced BiCMOS and advanced CMOS will coexist as viable product technologies, each supporting a dedicated group of customers. Time will tell.

Advanced High-Speed CMOS (AHC) Logic Family

SCAA034
January 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**4–25**
High-Speed CMOS (HC)	**4–25**
Advanced High-Speed CMOS	**4–26**
Protection Circuitry	**4–26**
Electrostatic Discharge	4–26
Latchup Protection	4–27
AC Performance	**4–28**
Power Consideration	**4–28**
Power Dissipation	**4–29**
Input Characteristics	**4–30**
AHC Input Circuitry	**4–30**
Input Current Loading	4–32
Supply Current Change (ΔI_{CC})	4–32
DC Characteristics	**4–33**
AHC/AHCT Output Circuitry	**4–33**
Output Drive	4–34
Partial Power Down	4–34
Proper Termination of Outputs	**4–35**
Common Termination Techniques	**4–35**
Shunt	4–35
AC	4–36
Thevenin	4–36
Diode	4–36
Series (Source Terminated)	4–36
Signal Integrity	**4–37**
Simultaneous Switching	4–37
Ground-Bounce Measurement	4–39
AHC Versus HC	**4–40**
Advanced Packaging	**4–41**
MicroGate	**4–42**
Acknowledgment	**4–42**

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

List of Illustrations

Figure	*Title*	*Page*
1	ESD Input Protection Circuitry	4–26
2	ESD Output Protection Circuitry	4–27
3	Parasitic Bipolar Transistors in CMOS	4–27
4	Schematic of Parasitic SCR Showing P-Gate and N-Gate Electrodes Connected	4–28
5	I_{CC} Versus Frequency	4–29
6	Supply Current Versus Input Voltage	4–30
7	Simplified Input Stage of an AHC Circuit	4–30
8	Output Voltage Versus Input Voltage (AHC04)	4–31
9	Output Voltage Versus Input Voltage (AHCT04)	4–31
10	Input Current Versus Input Voltage (AHC245)	4–32
11	Simplified Output Stage of an AHC Circuit	4–33
12	AHC Output Characteristics	4–34
13	Termination Techniques	4–35
14	Output Buffer With External Parasitics	4–38
15	Simultaneous-Switching-Noise Waveform	4–39
16	Ground-Bounce Test Circuit	4–39
17	AHC/AHCT and HC Family Positioning	4–40
18	AHC Packages	4–41
19	SN74AHC245 Pinout	4–42
20	5-Pin MicroGate Pinout	4–42

List of Tables

Table	*Title*	*Page*
1	HC and AHC Performance Comparison (Typical Values)	4–28
2	Input-Current Specification	4–32
3	ΔI_{CC}-Current Specification	4–32
4	AHC DC Specifications	4–33
5	Termination Techniques Summary	4–37
6	AHC and HC Features (Typical Values)	4–40

Introduction

The Texas Instruments (TI) Advanced High-Speed CMOS (AHC) logic family provides a natural migration for HCMOS users who need more speed for low-power, and low-drive applications. Unlike many other advanced logic families, it does not have any of the drawbacks that come with higher speed, e.g., higher signal noise and power consumption. The AHC logic family consists of gates, medium-scale integrated circuits, and octal functions fabricated using the EPIC process that features higher performance than the High-Speed CMOS (HC) product family at comparable cost.

This application report introduces the Advanced High-Speed CMOS (AHC) logic family characterization information to supplement the AHC data book. The additional information will aid design engineers in more accurately designing their digital logic systems. The focus is on the family's features and benefits, product characteristics, and design guidelines. This application note is divided into sections, each dealing with a specific characteristic of the family. This application report focuses on the AHC family and compares it to the HC product family.

The main topics discussed are:

- High-Speed CMOS (HC)
- Advanced High-Speed CMOS (AHC)
- Protection Circuitry
- AC Performance
- Power Considerations
- Input Characteristics
- Output Characteristics
- Signal Integrity
- AHC Versus HC
- Advanced Packaging
- MicroGate

For more information on TI's AHC logic products, please contact your local TI field sales office or an authorized distributor, or call TI at 1-800-336-5236.

High-Speed CMOS (HC)

High-Speed CMOS has the following characteristics:

- HC family covers a wide range of applications: low power drain for low-speed systems, and a slightly higher drain for higher-speed systems.
- The HC family has ac parameters ensured at supply voltages of 2 V, 4.5 V and 6 V over the full operating temperature range into a 50-pF load. The TTL compatible version, HCT, is specified for a 4.5-V to 5.5-V V_{CC} range.
- In HC, only the gates that are switching contribute to the dynamic system power. This reduces the size of the power supply required, thus providing lower system cost and higher reliability through lower heat dissipation.
- HC devices are ideal for battery-operated systems, or systems requiring battery back-up because there is virtually no static power dissipation.
- Improved noise immunity is due to the rail-to-rail (V_{CC} to ground) output voltage swings.
- HC devices are warranted for operation over an extended temperature range of –40°C to 85°C.

Advanced High-Speed CMOS

Advanced High-Speed CMOS (AHC) can be used for higher speed applications. Some advantages of using AHC over HC are:

- The AHC is almost three times faster than the HC. The AHC has a typical propagation delay of about 5.2 ns.
- The AHC family allows designers to combine the low-noise characteristics of HCMOS devices with today's performance levels without the overshoot/undershoot problems typical of higher drive devices.
- The AHC family has lower power consumption than the HC family.
- The output drive is ±8mA at 5-V V_{CC} and ±4mA at 3.3-V V_{CC}.
- AHC devices are available in D and DW (SOIC), DB (SSOP), N (PDIP), PW (TSSOP), and DGV (TVSOP) packages. Selected AHC devices are available in military versions (SN54AHCxx).
- MicroGate (single gate) versions that simplify routing are also available.

Protection Circuitry

Electrostatic discharge (ESD) and latchup are two traditional causes of CMOS device failure. To protect AHC devices from ESD and latchup, additional circuitry has been implemented at the inputs and outputs of each device.

Electrostatic Discharge

ESD occurs when a buildup of static charges on one surface arcs through a dielectric to another surface that has the opposite charge. The end effect is the ESD causes a short between the two surfaces. These damaged devices may still pass normal data sheet tests, but will eventually fail. The input and output protection circuitry designed by TI provides immunity to over 2000 V in the human-body-model test, over 200 V in the machine-model test, and over 1000 V in the charged-device model test.

Figure 1 shows the circuitry implemented to provide protection for the input gates against ESD. The primary protection device is a low-voltage-triggered silicon-controlled rectifier (LVTSCR). During an ESD event, most of the current is diverted through the LVTSCR. Additional protection is provided by the resistor and secondary clamp transistors, which break down during an ESD event and protect the gate oxides.

Figure 2 shows how the LVTSCR is used to protect an output.

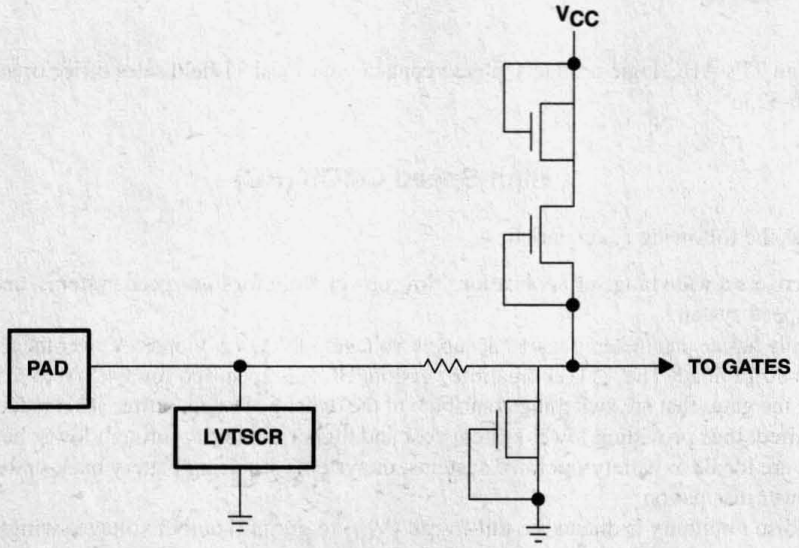


Figure 1. ESD Input Protection Circuitry

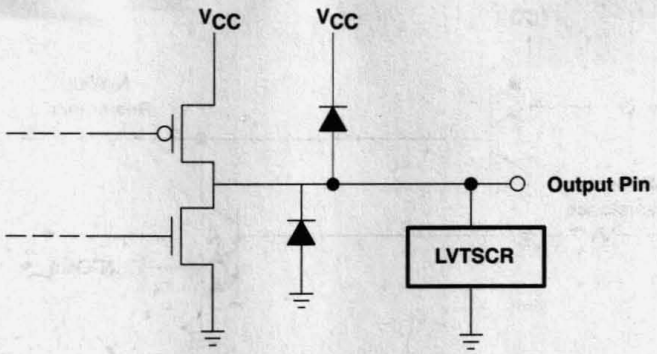


Figure 2. ESD Output Protection Circuitry

Latchup Protection

Internal to almost all CMOS devices are two parasitic bipolar transistors; one p-n-p and one n-p-n. Figure 3 shows the cross section of a typical CMOS inverter with the parasitic bipolar transistors. Note that, as shown in Figure 4, these parasitic bipolar transistors are naturally configured as a thyristor or a silicon-controlled rectifier (SCR). These transistors conduct when one or more of the p-n junctions become forward biased. When this happens, each parasitic transistor supplies the necessary base current for the other to remain in saturation. This is known as the "latchup" condition and can possibly destroy the device if the supply current is not limited.

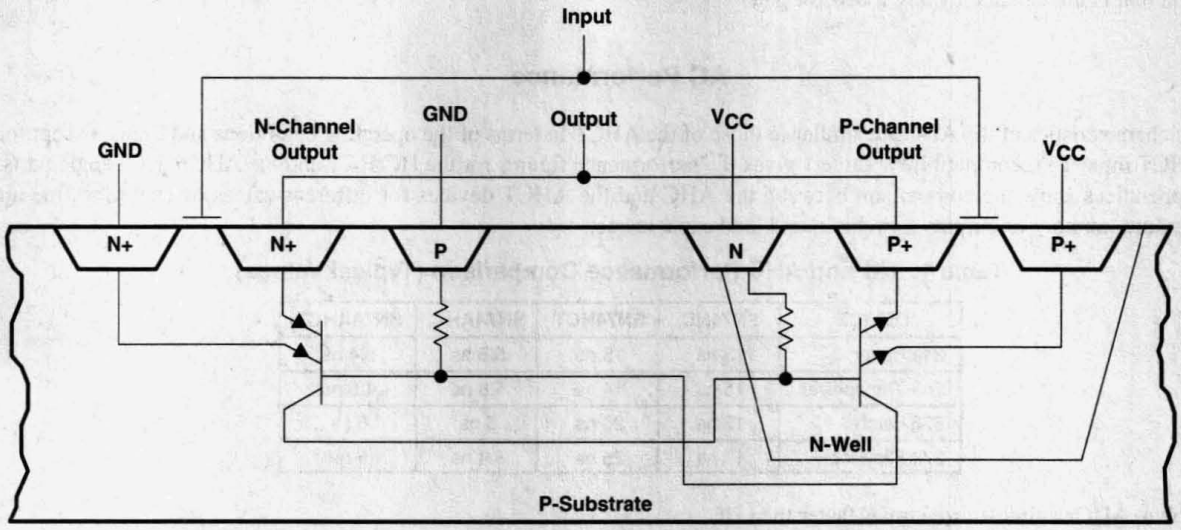


Figure 3. Parasitic Bipolar Transistors in CMOS

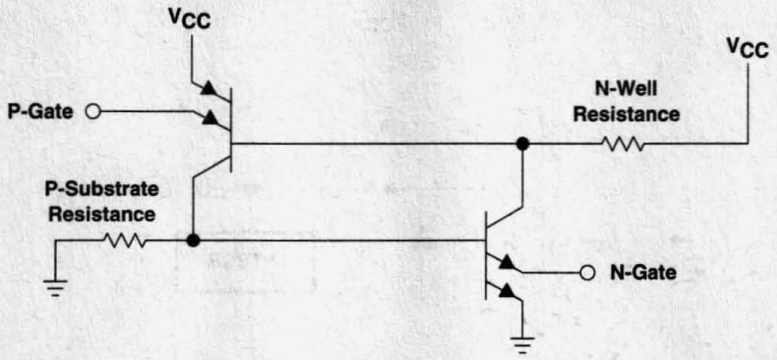


Figure 4. Schematic of Parasitic SCR Showing P-Gate and N-Gate Electrodes Connected

A conventional thyristor is fired (turned on) by applying a voltage to the base of the n-p-n transistor, but the parasitic CMOS thyristor is fired by applying a voltage to the emitter of either transistor. One emitter of the p-n-p transistor is connected to an emitter of the n-p-n transistor, which is also the output of the CMOS gate. The other two emitters of the p-n-p and the n-p-n transistors are connected to V_{CC} and ground, respectively. Therefore, to trigger the thyristor there must be a voltage greater than V_{CC} + 0.5 V or less than –0.5 V and there has to be sufficient current to cause the latchup condition.

Latchup cannot be completely eliminated. The alternative is to prevent the thyristor from triggering. TI has improved the circuit design by adding an additional diffusion or guard ring. The guard ring provides isolation between the device pins and any p-n junction that is not isolated by any transistor gate.

AC Performance

The ac characteristics of the AHC are similar to those of the AHCT in terms of the operating conditions and limits, except for the AHCT input TTL compatibility. Table 1 gives the performance figures for the HC/HCT and the AHC/AHCT logic parts. The appendices show the comparison between the AHC and the AHCT devices for different values of operating free-air temperature, number of outputs switching, and load capacitance.

Table 1. HC and AHC Performance Comparison (Typical Values)

DEVICE	SN74HC	SN74HCT	SN74AHC	SN74AHCT
244 Buffer	13 ns	15 ns	5.8 ns	5.4 ns
245 Transceiver	15 ns	14 ns	5.8 ns	4.5 ns
373 Latch	15 ns	20 ns	5 ns	5 ns
374 Flip Flop	17 ns	25 ns	5.4 ns	5 ns

As shown, AHC is almost three times faster than HC.

Power Considerations

The power dissipation of CMOS devices can be divided into three components:

- Quiescent power dissipation, P_q
- Transient power dissipation, P_t
- Capacitive power dissipation, P_c

The quiescent power is the product of V_{CC} and the quiescent current, I_{CC}. The quiescent current is the reverse current through the diodes that are reverse biased. This reverse current is generally very small (on the order of a few nA), which makes the quiescent power insignificant. However, for circuits that are in static condition for long periods, the quiescent power becomes a factor to be considered.

The transient power is due to the current that flows only during the time the transistors are switching from one logic level to the other. During this time, both of the transistors are partially on, which produces a low-impedance path between V_{CC} and ground that results in a current spike. The rise (or fall) time of the input signal has a direct effect on the duration of the current spike. This is because the faster the input signal passes through the transition region, the less time both transistors are partially on. The transient power is dependent on the characteristics of the transistors, the switching frequency, and the rise and fall times of the input signal. The component can be calculated using the following equation:

$$P_t = C_{pd} \times V_{CC}^2 \times f_I \quad (1)$$

Where:

V_{CC} = Supply voltage (V)
f_I = Input frequency (Hz)
C_{pd} = power dissipation capacitance (F)

Additional capacitive power dissipation is caused by the charging and discharging of external load capacitance and is dependent on the switching frequency. To calculate the power, the following equation can be used:

$$P_C = C_L \times V_{CC}^2 \times f_O \quad (2)$$

Where:

V_{CC} = Supply voltage (V)
f_O = Output frequency (Hz)
C_L = External load capacitance (F)

Power Dissipation

AHCT devices are used primarily to interface TTL output signals to CMOS inputs. To make the inputs of the AHCT devices TTL-voltage compatible, the input transistor geometries were changed. This increased the power consumption, as compared to the equivalent AHC device if the input is kept at a level other than GND or V_{CC}. The increase in power consumption occurs because TTL input levels cause both transistors in the transistor pair to be partially turned on. Included in the tables for the AHCT devices is a parameter, ΔI_{CC}, which enables the designer to compute how much additional current the AHCT device draws per input when at a TTL-voltage level.

Figure 5 shows the relation between the supply current and the frequency of operation for the AHC245 and the AHCT245. As shown, the increase in power consumption for the AHCT is relatively insignificant.

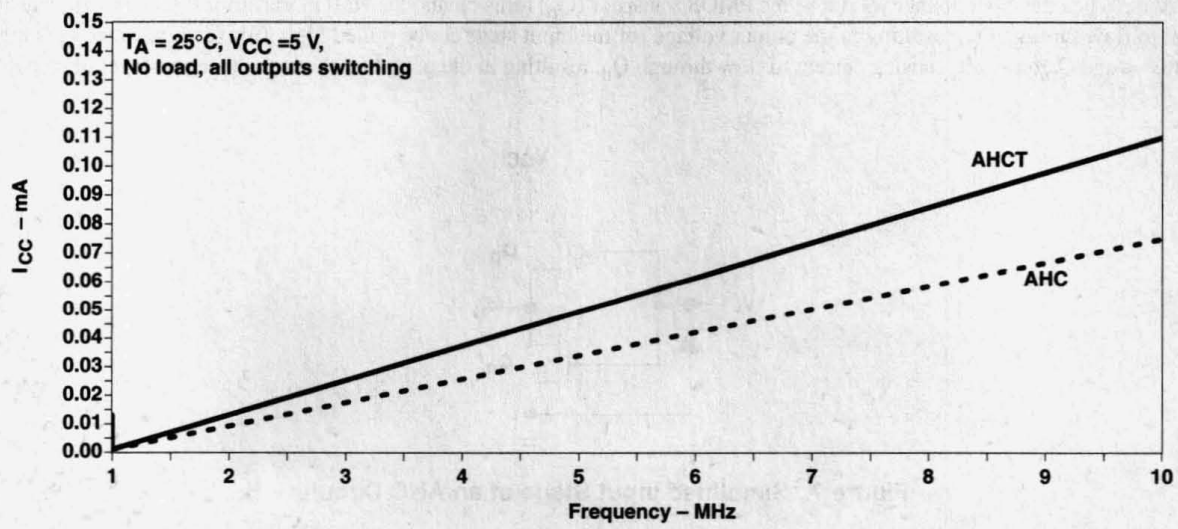


Figure 5. I_{CC} Versus Frequency

Input Characteristics

The AHC family input structure is such that the 5-V CMOS dc V_{IL} and V_{IH} fixed levels of 1.5 V and 3.5 V are ensured, meaning that, while the threshold voltage of 2.5 V is typically where the transition from a recognized low input to a recognized high input occurs, it is at 1.5 V and 3.5 V that the corresponding output levels are specified. For AHCT, V_{IL} and V_{IH} fixed levels of 0.8 V and 2 V are ensured, and the threshold voltage is 1.5 V. Figure 6 shows the characteristics for the AHC245 and the AHCT245.

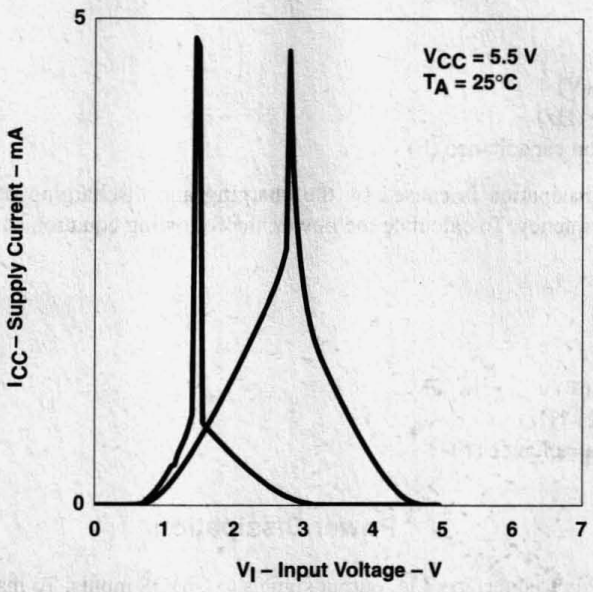


Figure 6. Supply Current Versus Input Voltage

AHC Input Circuitry

The simplified AHC input circuit shown in Figure 7 consists of two transistors, sized to achieve a threshold voltage of 2.5 V. Since V_{CC} is 5 V and the threshold voltage is commonly set to be centered around one-half of V_{CC} in a pure CMOS input, additional circuitry to reduce the voltage level is not required and the resulting simplified input structure consists of two transistors. When the input voltage V_I is low, the PMOS transistor (Q_p) turns on and the NMOS transistor (Q_n) turns off, causing current to flow through Q_p, resulting in the output voltage (of the input stage) to be pulled high. Conversely, when V_I is high, Q_n turns on and Q_p turns off, causing current to flow through Q_n, resulting in the output voltage (on the input stage) to be pulled low.

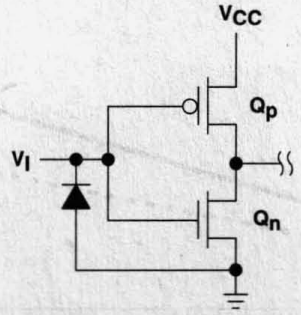
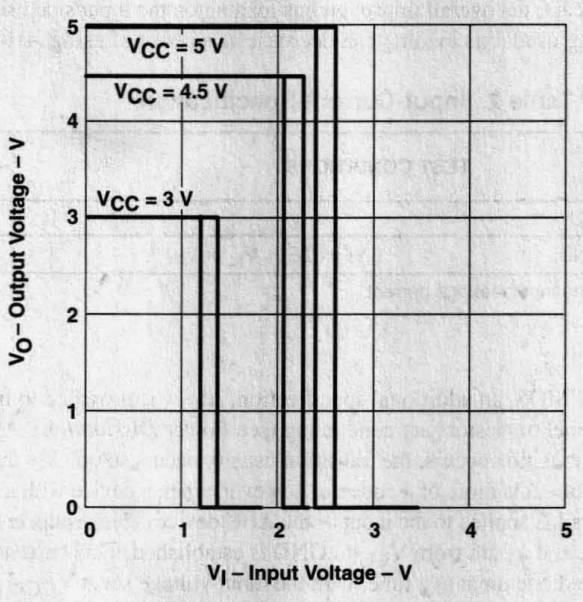


Figure 7. Simplified Input Stage of an AHC Circuit

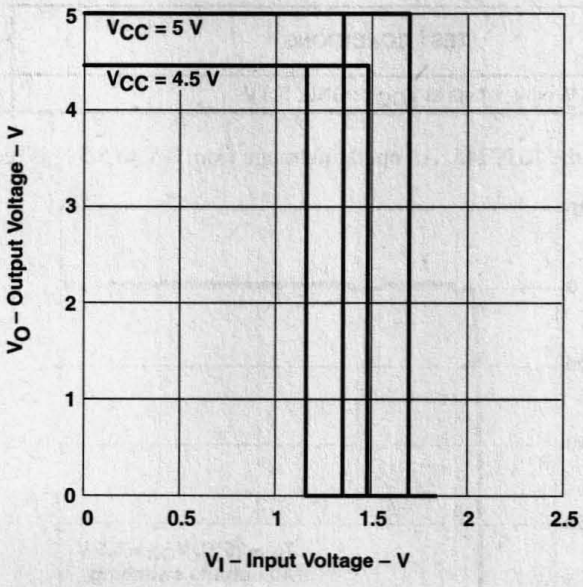
Figures 8 and 9 show the graphs of V_O versus V_I for the AHC04 and the AHCT04. The recommended operating range for the AHC family is from 2 V to 5.5 V. For the AHCT the recommended range is from 4.5 V to 5.5 V. Input hysteresis of typically 150 mV is included in AHC devices (300 mV in AHCT devices), which ensures the devices are free from oscillations by increasing the noise margin around the threshold voltage during low-input transitions.



$T_A = 25°C$

V_{CC}	V_IHL	V_ILH
5.0 V	2.38 V	2.49 V
4.5 V	2.13 V	2.22 V
3.0 V	1.35 V	1.42 V

Figure 8. Output Voltage Versus Input Voltage (AHC04)



$T_A = 25°C$

V_{CC}	V_IHL	V_ILH
5.0 V	1.37 V	1.55 V
4.5 V	1.28 V	1.46 V

Figure 9. Output Voltage Versus Input Voltage (AHCT04)

Input Current Loading

Minimal loading of the system bus occurs when using the AHC family due to the EPIC™ process CMOS input structure; the only loading that occurs is caused by leakage current and capacitance. Input current is low, typically less than 1 μA, as shown in Table 2. Capacitance for transceivers can be as low as 2.5 pF for C_i and 4 pF for C_{io}. Since both of the variables that can affect bus loading are relatively insignificant, the overall impact on bus loading on the input side using AHC devices is minimal and, depending on the logic family being used, bus loading can decrease as a result of using AHC parts.

Table 2. Input-Current Specification

PARAMETER	TEST CONDITIONS	SN74AHC245		UNIT
		MIN	MAX	
I_I	$V_I = V_{CC}$ or GND		±1	μA
I_{OZ}†	$V_O = V_{CC}$ or GND, $V_I = (\overline{OE}) = V_{IL}$ or V_{IH}		±2.5	μA

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

Supply Current Change (ΔI_{CC})

Because the input circuitry for AHC is CMOS, an additional specification, ΔI_{CC}, is provided to indicate the amount of input current present when both p- and n-channel transistors are conducting (see *Power Dissipation*). Although this situation exists whenever a low-to-high or high-to-low transition occurs, the transition usually occurs so quickly that the current flowing while both transistors are conducting is negligible. It is more of a concern, however, when a device with a TTL output drives the AHC part. Here, a dc voltage that is not at the rail is applied to the input of the AHC device. This results in both the n-channel transistor and the p-channel transistor conducting, and a path from V_{CC} to GND is established. This current is specified as ΔI_{CC} in the data sheet for each device and is measured one input at a time, with the input voltage set at $V_{CC} - 0.6$ V, while all other inputs are at V_{CC} or GND. Table 3 provides the ΔI_{CC} specification, which is contained in the data sheet for the SN74AHCT245.

Table 3. ΔI_{CC}-Current Specification

PARAMETER	TEST CONDITIONS	SN74AHCT245		UNIT
		MIN	MAX	
ΔI_{CC}	One input at 3.4 V, other inputs at V_{CC} or GND, 5.5 V		1.5	mA

Figure 10 is a graph of I_I versus V_I for the AHC245. An operating range from 0 V to 5.5 V is recommended.

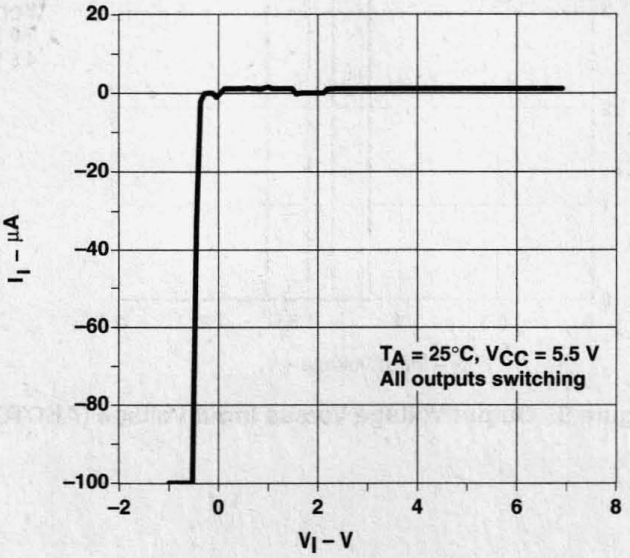


Figure 10. Input Current Versus Input Voltage (AHC245)

DC Characteristics

The AHC family uses a pure CMOS output structure. The AHC family has the dc characteristics shown in Table 4. The values are measured at $T_A = 25°C$.

Table 4. AHC DC Specifications

PARAMETER	TEST CONDITIONS		V_{CC}	SN74AHC245			UNIT
				MIN	TYP	MAX	
V_{OH}	$I_{OH} = -50\ \mu A$		2 V	1.9	2		V
			3 V	2.9	3		
			4.5 V	4.4	4.5		
	$I_{OH} = -4$ mA		3 V	2.58			V
	$I_{OH} = -8$ mA		4.5 V	3.94			V
V_{OL}	$I_{OL} = 50\ \mu A$		2 V				V
			3 V			0.1	
			4.5 V				
	$I_{OL} = 4$ mA,		3 V			0.36	V
	$I_{OL} = 8$ mA,		4.5 V			0.36	V
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1	μA
I_{OZ}†	$V_O = V_{CC}$ or GND,	V_I (OE) = V_{IL} or V_{IH}	5.5 V			±0.25	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			4	μA
C_i	$V_I = V_{CC}$ or GND		5 V		2.5		pF
C_{io}	$V_I = V_{CC}$ or GND		5 V		4		pF

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

AHC/AHCT Output Circuitry

Figure 11 shows a simplified output stage of an AHC/AHCT circuit. When the NMOS transistor (Q_n) turns off and the PMOS transistor (Q_p) turns on and begins to conduct, the output voltage (V_O) is pulled high. Conversely, when Q_p turns off, Q_n begins to conduct and V_O is pulled low. The AHC/AHCT devices have a rail-to-rail output swing to make it compatible with the HC/HCT families.

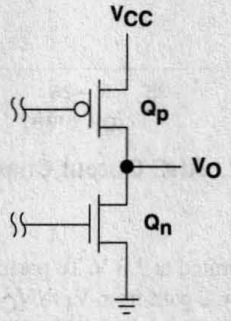


Figure 11. Simplified Output Stage of an AHC Circuit

Output Drive

Figure 12 shows values for V_{OL} vs I_{OL}, and I_{OH} vs V_{OH} for the AHC/AHCT245.

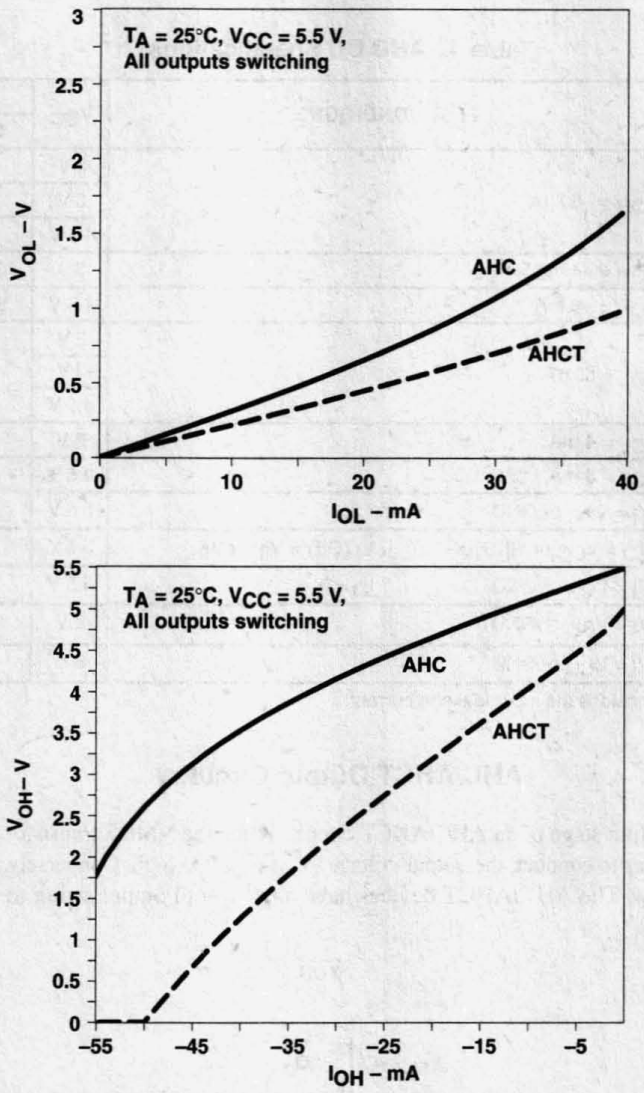


Figure 12. AHC Output Characteristics

Partial Power Down

All AHC devices are 5-V input tolerant when operated at 3.3 V. To partially power down a device, no paths from V_I to V_{CC} or from V_O to V_{CC} can exist. With the AHC family, a path from V_I to V_{CC} has never been an issue. However, as noted earlier, AHC devices are not 5-V output tolerant and do have a path from V_O to V_{CC}. For these devices, when V_{CC} begins to diminish, a diode from V_O to V_{CC} begins to conduct and current flows, resulting in damage to the power supply and/or to the device. The 5-V tolerant AHCT devices are designed so that this path from V_O to V_{CC} is eliminated. As such, AHC devices that are not 5-V tolerant are not capable of being partially powered down, whereas AHCT devices that are 5-V tolerant are capable of being partially powered down.

Proper Termination of Outputs

Depending on the trace length, special consideration may need to be given to the termination of the outputs. As a general rule, if the trace length is less than four inches, no additional components are necessary to achieve proper termination. If the trace length is greater than four inches, reflections begin to appear on the line and the system may appear noisy and generate unreliable data. The solution to this is to terminate the outputs in an appropriate manner to minimize the reflections.

Common Termination Techniques

Most transmission-line termination techniques rely on impedance matching at either the source or receiver to reduce reflections and line noise (see Figure 13). Series, thevenin, and ac techniques are commonly used and are effective methods of line termination for high-speed logic. Shunt is educational, but has implementation problems. Diodes can be used as a solution, but, generally, this is not a good termination technique by itself.

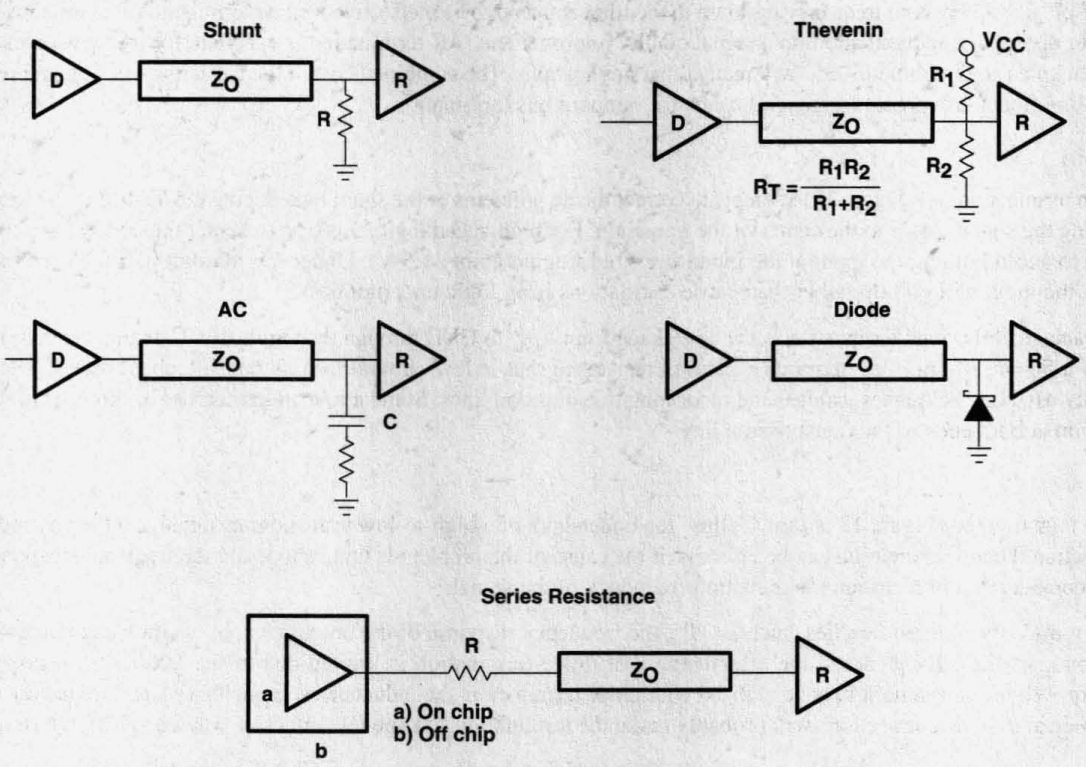


Figure 13. Termination Techniques

Shunt

Shunt termination (see Figure 13) is one of the simplest termination techniques to implement. The value of the termination resistor should match the line impedance for best performance. As the transmitted signal reaches the receiver, the shunt termination drains off the current with an impedance matching the transmission line. There is no reflection, thus, no noise is retransmitted down the transmission line.

There are several disadvantages to shunt termination. Usually the line impedance is fairly low (50 to 70 Ω), which requires a resistor of similar value. This causes a heavy dc current drain on the source when in the logic high state and requires a strong line driver to source the current. With the low-impedance resistor pulling to GND, the V_{OH} of the transmission line will be lower, reducing the noise immunity at the receiver. Additionally, having a strong pull down on the transmission line may unbalance the rising and falling edges of the signal, causing the falling edge to be faster than the rising edge, resulting in duty-cycle distortion of the signal.

AC

AC termination utilizes the same line-impedance-matching resistor as shunt termination, except it is ac coupled with a capacitor, making a simple high-pass filter. The capacitor appears to be a short circuit during signal transitions when termination is needed, but eliminates the dc component of the current drain.

AC termination (see Figure 13) has the precise termination advantages of shunt termination, but reduces the disadvantages of dc current drain and waveform distortion. At each transition of the signal, the capacitor will charge up to the voltage level necessary to maintain zero volts across the resistor. During the arrival of the next input transition, the signal will be driving the full value of the resistor until the capacitor can again recharge.

It is recommended that the resistor value be equivalent to the line impedance. The ideal capacitor value will vary with line impedance, edge rate, and desired signal quality. The values are not critical, but tests have shown that with TI logic, a value of 50 pF for the capacitor is a good compromise. Increasing the capacitance value to 200 pF will improve signal quality, but sacrifice power dissipation. Reducing the value to 47 pF lowers the power dissipation, but sacrifices signal quality. Values below 47 pF give a very high frequency response to the filter and tend to be ineffective for line termination. Values above 200 pF add power dissipation without additional signal quality improvement. AC termination is excellent for use with clock drivers, cables, backplanes, distributed loads, and many other applications. The combined cost of the capacitor, resistor, and real estate for each line frequently precludes general usage for onboard bus termination.

Thevenin

Thevenin termination (see Figure 13) attempts to correct the dc problems of the shunt by reducing the dc load of the termination and pulling the signal closer to the center of the transition. For high-speed logic, it is best to center the dc level at a logic high (>2.0 V) to avoid holding the input at the input threshold (toggle point »1.5 V). Under this condition, if the driver shuts off (high Z), the input will pull up rather than cause oscillations from logic uncertainties.

A disadvantage of thevenin termination is the dc leakage from V_{CC} to GND through the terminator. Using thevenin termination to match a 50- or 70-ohm line requires a parallel resistance that is low enough to pass considerable current. Thevenin is commonly used on backplanes, cables, and other long transmission lines. Some applications such as backplanes may require termination at both ends of the transmission line.

Diode

Diode termination (see Figure 13) simply "clips" the undershoot of a high-to-low transitioning signal and thereby reduces the line reflection. Diode termination can be effective if the cause of the problem is undershoot and the frequency response of the diode is considerably higher than the transition frequency of the signal.

With very-high-speed logic families, such as TI's, the frequency response of the output signal transition can reach 400 MHz and beyond. At these frequencies, the effectiveness of diode termination is limited due to the frequency response of the terminator. While some benefit may be realized with diode termination, the inductances, capacitances, and frequency response of the diode and diode connections will probably make the termination scheme less effective when used at high frequencies.

The internal parasitic clamp diode to ground, found on the inputs and outputs of all CMOS logic, will bleed off some of the overshoot current, but this parasitic clamp does not have the necessary frequency response to perform effective diode termination in high-speed applications. Diode termination is frequently used on backplanes and long cables, possibly in conjunction with another form of line termination.

Series (Source Terminated)

Series termination reduces the output edge rate of the driver, the switching amplitude of the signal, and reduces the charge injected into the transmission line. This has significant benefits by reducing signal line noise and EMI. Series termination adds a series resistor at the output of the line driver, effectively increasing the source impedance of the driver (see Figure 13). When using series termination with distributed loads, care must be taken that the combined output impedance of the driver and series resistor is small enough to allow first incident-wave switching. If the output impedance becomes too high, the "step" that is seen in the output transition will not toggle the components at the near end of the transmission line until the signal passes down the line and returns to the source, causing an unnecessary propagation delay. Series termination is the most commonly used form of termination and is found on circuit boards, cables, and in most other applications.

Table 5 provides a comparison of the five termination techniques.

Table 5. Termination Techniques Summary

TECHNIQUE	ADDITIONAL DEVICES	POWER INCREASE	DELAY	HOLDS DEFINED LEVEL	IDEAL VALUE†	COMMENTS
Shunt	1	Significant	No	Yes	$R = Z_O$	Low dc noise margin
Thevenin	2	Yes	No	Yes	$R_1 = R_2 = 2Z_O$	Good for backplanes due to maintaining drive current
AC	2	Yes	No	No	$R = Z_O$ $60 < C < 330$ pF	Increase in frequency and power
Series resistor on device	0	No	Small	No	$25 =< R =< 33\ \Omega$	Good undershoot clamping; useful for point-to-point driving
Diode	1	No	No	No	NA	Good undershoot clamping; useful for standard backplane terminations

† Symbols are defined in Figure 13.

Signal Integrity

System designers often are concerned with the performance of a device when the outputs are switched. The most common method of assessing this is by observing the impact on a single output when multiple outputs are switched.

Simultaneous Switching

In a digital circuit, when multiple outputs switch, the current through the ground or V_{CC} terminals changes rapidly. As this current flows through the ground (or V_{CC}) return path, it develops a voltage across the parasitic inductance of the bond wire and the package pin. The phenomenon is called simultaneous switching noise. Figure 14 shows the equivalent circuit of a typical CMOS output buffer stage with the package parasitics and the external load. The parasitic components that affect the ground bounce are inductance and resistance of the ground bond wire and pin, inductance and resistance of the output bond wire and pin, and load impedance. For the first-order analysis, the parasitics associated with the V_{CC} terminal can be ignored. Also, the external ground plane is assumed to be ideal.

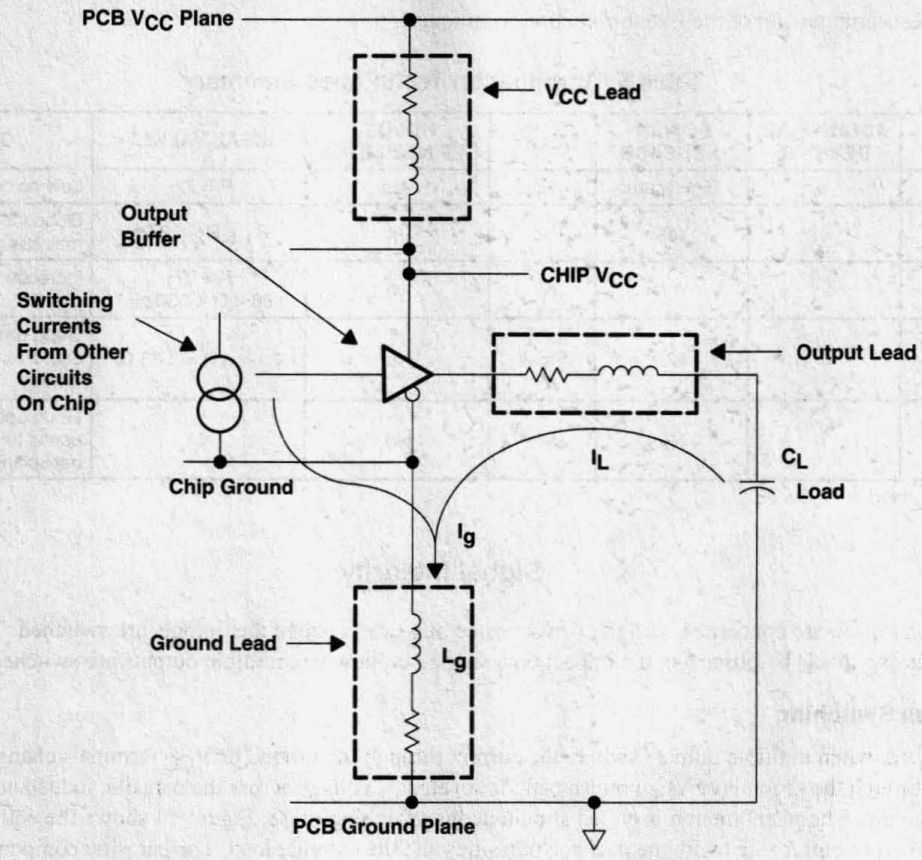


Figure 14. Output Buffer With External Parasitics

During the output high-to-low transition, the sum of the output load current and all switching current through the internal gates of the device flows through the ground lead. The rate of change of this current (di/dt) develops a voltage drop across the ground lead inductance and causes a positive ground bounce or an overshoot in an otherwise quiet ground. This positive ground bounce is normally followed by an undershoot coincident with the voltage waveform on the output terminal. The amplitudes of both the positive and the negative ground bounce are a function of $L_g * di/dt$ and of the number of outputs switching simultaneously (SS noise). The ground-bounce phenomenon can be clearly observed at an unswitched "low" output of a device by switching several other outputs simultaneously from logic high to low. Figure 15 shows the typical output voltage transition and the corresponding ground bounce, as observed at the unswitched low output. Positive ground bounce is primarily the result of the rate of change of current (di/dt) through the ground lead inductance. The rate is determined by the rate at which the gate-to-source voltage (V_{gs}) of the sink transistor changes. During the early part of the fall time, the ground voltage rises while the output voltage falls, forcing the sink transistor into the linear region. The transistor then behaves like a resistor R_{on} (the "on" resistance of the transistor in the linear region). For the remainder of the output voltage excursion, the equivalent circuit at the output can be treated like a resonant L-C-R circuit formed by the ground and the output lead inductance, load capacitance, and the total resistance in the loop, which includes R_{on}. The oscillation frequency is determined by the net values of L and C while damping is determined by L and the total resistance in the loop. Ground bounce is also generated during the output low-to-high transition. However, the magnitude of this ground bounce is much smaller because of the absence of load current in the ground lead.

Ground and V_{CC} bounce cannot be entirely eliminated, but they can be minimized by controlling edge rates and reducing output swing. Ground bounce depends on many factors, with device speed being one of the more important influences. As device speed goes up, the rate of change of current in the parasitic inductances increases and the related switching noise goes up. Due to this correlation between speed and ground bounce, high-speed logic families arouse increased concern over noise due to simultaneous switching of outputs.

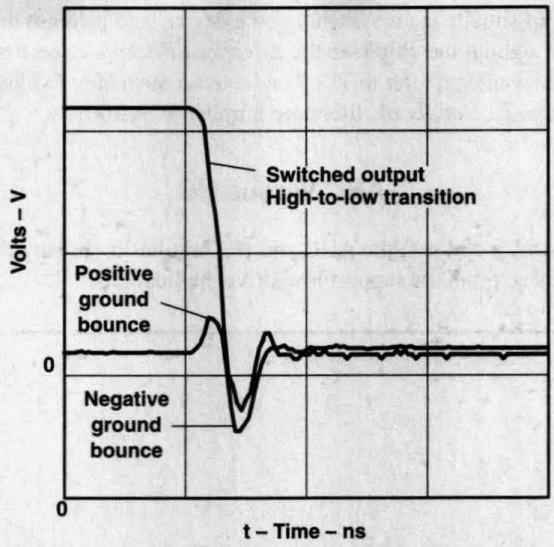


Figure 15. Simultaneous-Switching-Noise Waveform

Ground-Bounce Measurement

There is no industry standard for measuring ground bounce. However, the method most commonly used by IC vendors and customers is based on observing the disturbance of a logic-low level on an unswitched output of a multiple-output device while switching all other outputs from a high to a low state. Figure 16 shows the schematic for measuring ground bounce on a device such as the AHC244 octal buffer. One output is in the low state while the outputs are switched simultaneously. The load on each output consists of a 50-pF capacitor. Two outputs are connected to the oscilloscope: one for observing the high-to-low transition of a switched output and the other for observing the ground bounce on the quiet output.

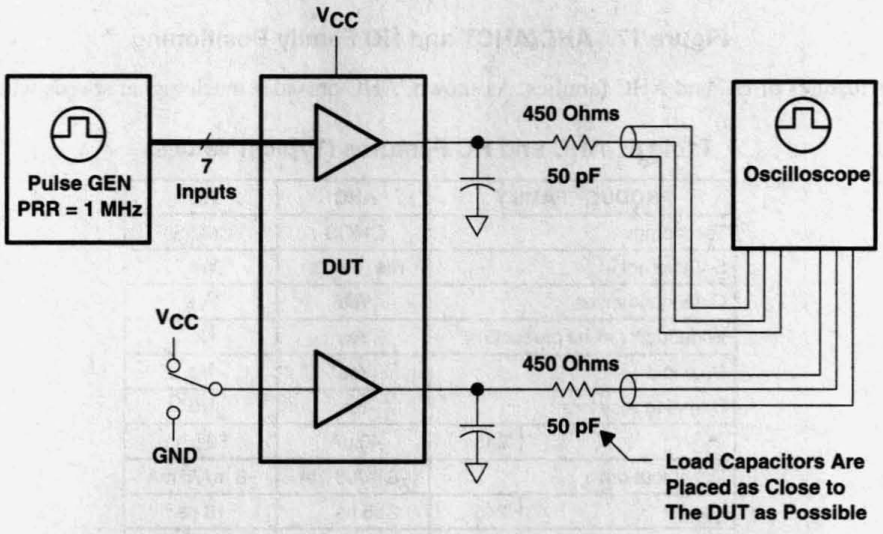


Figure 16. Ground-Bounce Test Circuit

With careful layout, proper bypassing to filter out high-frequency noise, and good oscilloscope probes, it is possible to observe the ground bounce on the internal ground of the chip by observing the voltage at the unswitched "low" output, whose sink transistor operates in the linear region and provides a "Kelvin connection" to the chip ground.

One technique to reduce the impact of simultaneous switching on a device is to increase the number of power and GND pins. The strategy is to disperse them throughout the chip (see the *Advanced Packaging* section of this application report). For a complete discussion of simultaneous switching, refer to TI's *Simultaneous Switching Evaluation and Testing* application report or the *Advanced CMOS Logic Designer's Handbook*, literature number SCAA001A.

AHC Versus HC

A speed versus current-drive comparison between the AHC and HC families is shown in Figure 17. The speed for the AHC is much higher than the HC. Both these products support low-drive applications.

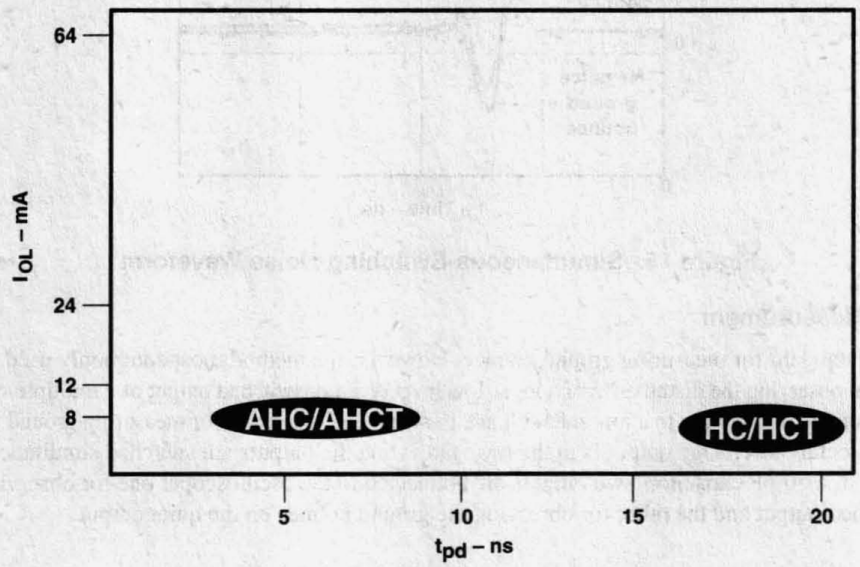


Figure 17. AHC/AHCT and HC Family Positioning

Table 6 shows the features of HC and AHC families. As shown, AHC provides much higher speeds with no noise penalty.

Table 6. AHC and HC Features (Typical Values)

PRODUCT FAMILY		AHC	HC
Technology		CMOS	CMOS
5-V tolerant†		Yes (Inputs)	Yes
Octals and gates		Yes	Yes
Widebus™ (16-bit products)		Yes	No
Bus hold		Yes	No
Damping resistors		No	No
I_{CC}	'245	40 µA	80 µA
DC output drive		–8 mA/8 mA	–8 mA/8 mA
t_{pd}	'245	5 ns	18 ns
C_i	'245	2.5 pF	3 pF
C_{io}	'245	8 pF	10 pF

† When operated at 3.3 V

Advanced Packaging

Figure 18 shows a comparison of the various packages in which AHC devices are available; for ease of analysis, 14-pin packages and 20-pin packages are included. Figure 19 is not an all-inclusive list of pin counts and corresponding packages, e.g., the TSSOP package is available in both 14-pin and 20-pin format. The new TVSOP package, which has a lead pitch of 0.4 mm (16 mil) and a device height of 1.2 mm, is also available in the AHC family. Continued advancements in packaging are making more functionality possible with smaller space requirements.

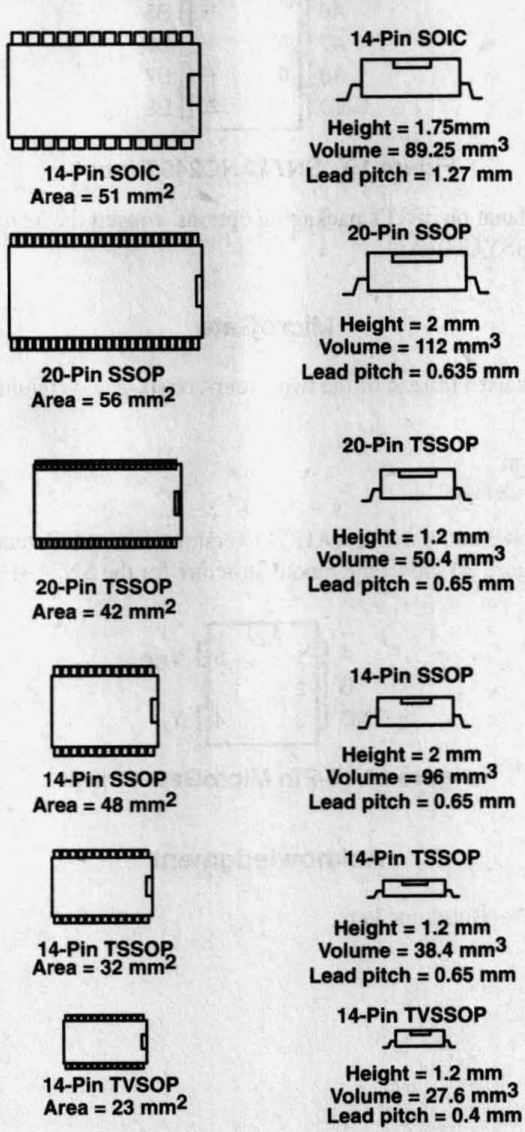


Figure 18. AHC Packages

Figure 19 shows a typical pinout structure for the 20-pin SSOP for the SN74AHC245. This provides for simultaneous switching improvements (see the *Signal Integrity* section of this application report).

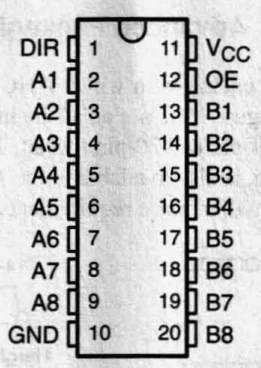


Figure 19. SN74AHC245 Pinout

For a comprehensive listing and explanation of TI's packaging options, consult the *Semiconductor Group Package Outlines Reference Guide*, literature number SSYU001A.

MicroGate

The MicroGate is a single gate that is used instead of the two-, four-, or six-gate versions. The advantages of MicroGate are:

- Simplifies circuit routing
- Helps in ASIC modification
- 3.5 ns typical propagation delay

The MicroGates exist in CMOS (AHC) and the TTL (AHCT) versions. The AHC versions are compatible with Toshiba's TC7SHxx series. As an example, Figure 20 shows the pinout structure for the SN74AHC1G00.

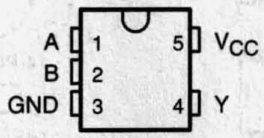


Figure 20. 5-Pin MicroGate Pinout

Acknowledgment

The author of this report is Shankar Balasubramaniam.

Advanced Schottky Load Management

SDYA016
February 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title *Page*

Introduction **4–49**

Waveform Characteristics Influenced by AS Loads Management **4–49**
- Propagation Delay 4–49
- Rise and Fall Times 4–50
- Ringing 4–51
- Overshoot and Undershoot 4–51

Equivalent Circuit Models **4–52**
- Logic Gate 4–52
- Input Equivalent 4–53
- Output Equivalent 4–53
- AS System Model 4–54

Transmission Lines **4–54**
- Transmission-Line Theory 4–54
- Transmission-Line Types 4–57
  - Microstrip Lines 4–57
  - Strip Lines 4–58
- Reflections 4–59
- Lattice Diagrams 4–61

Fanout **4–62**
- Influence on Transmission-Line Model 4–62
- Influence on Rise and Fall Times 4–63
- Combined Effects on Propagation Delay 4–65
- Influence on Ringing 4–65

Termination **4–66**
- When Termination is Needed 4–66
- Resistive Termination 4–68
- Parallel Termination 4–68
- Series Termination 4–69
- Fanout Correction 4–70
- Diode Termination 4–71

Spatial Considerations **4–72**

Ground-Plane Effects **4–72**

Summary **4–75**

Acknowledgment **4–75**

References **4–75**

List of Illustrations

Figure	*Title*	*Page*
1	Definition of Propagation Delay	4–49
2	Waveform Characteristics	4–50
3	Ringing	4–51
4	Overshoot and Undershoot	4–51
5	Schematic of 'AS04	4–52
6	AS Input Structure	4–53
7	AS Output Structure	4–53
8	AS System Model	4–54
9	Transmission-Line Components	4–55
10	Waveforms in the Time and Fourier Domains	4–56
11	Microstrip-Line Structure	4–57
12	Strip-Line Structure	4–59
13	Loaded Transmission Line	4–60
14	Lattice Diagram	4–61
15	Lattice Diagram Example	4–62
16	Transmission Line With Lumped Loading	4–63
17	Schematic Diagram of a Distributed Loaded System	4–64
18	Rise Time and Fall Time Versus Fanout	4–64
19	Propagation Delay Versus Fanout	4–65
20	Waveform Derived From Lattice Example	4–65
21	Overshoot Versus Fanout	4–66
22	Unterminated Single Load	4–66
23	Unterminated Single-Load Waveform	4–67
24	Parallel Termination	4–68
25	Parallel-Termination Waveform	4–68
26	Series Termination	4–69
27	Relation of Series-Termination Waveforms	4–69
28	Series-Termination Waveform	4–70
29	Active Termination	4–71
30	Active-Termination Waveform	4–71
31	Circuit to Observe the Effects of a 45-Degree Bend	4–72
32	Circuit to Observe the Effects of a 90-Degree Bend	4–72
33	Observed Waveforms With a 45-Degree Bend	4–73
34	Observed Waveforms With a 90-Degree Bend	4–74
35	Observed Waveforms	4–77
36	Comparison of Waveforms	4–78

List of Tables

Table	*Title*	*Page*
1	Typical Microstrip-Line Characteristics	4–58
2	Typical Strip-Line Characteristics	4–59
3	Voltage at End Points A and B	4–62
4	Maximum Line Length Without Termination	4–67

Appendices

Title	*Page*
Appendix A: Confirmation of AS Model	**4–77**
Appendix B: Transmission Lines: A Fourier Analysis	**4–79**

Introduction

As the scope of the digital integrated-circuit (IC) market broadens, the need for higher speed and lower-power-dissipation logic families increases. Texas Instruments (TI) serves this ever-expanding market by providing ICs appropriate to both a wide variety of today's applications as well as tomorrow's. The Advanced Schottky (AS) family of TTL ICs was developed by TI to handle high-speed digital applications.

The higher speed of AS devices makes possible new systems designs. However, it also increases the designer's responsibility to create an operating environment conducive to high clock rates, decreased propagation delays, and faster rise and fall times. Many designers of high-speed logic are aware of this responsibility but continue to rely on low-speed TTL design rules. The result can be less than optimal.

The purpose of this application report is to help designers of high-speed digital logic systems use AS TTL ICs. Emphasis is on managing AS loads. The major subjects covered are:

- AS waveforms
- Equivalent input/output circuits
- Transmission-line models
- Effects of fanout
- Termination
- Spatial layout
- Ground-plane effects

Waveform Characteristics Influenced by AS Loads Management

Propagation Delay

Propagation delay is the time between specific reference points on the input and output signals of a digital logic device. Typically, the trip point for a device is used as a reference point. The trip point for an AS device is 1.3 V. Thus, propagation delay for any AS device is the time between an input signal crossing 1.3 V and the associated output signal crossing 1.3 V (see Figure 1).

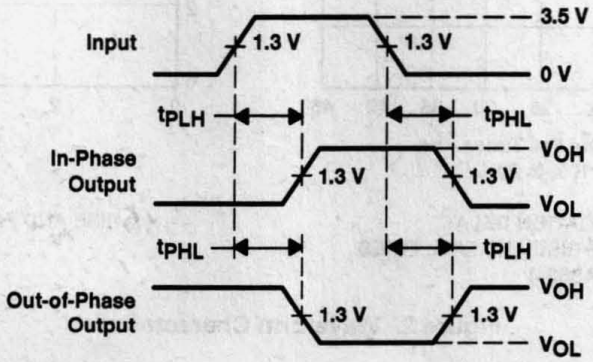
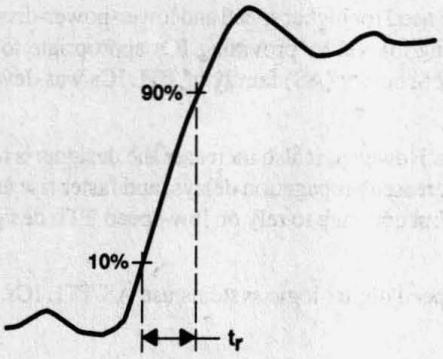


Figure 1. Definition of Propagation Delay

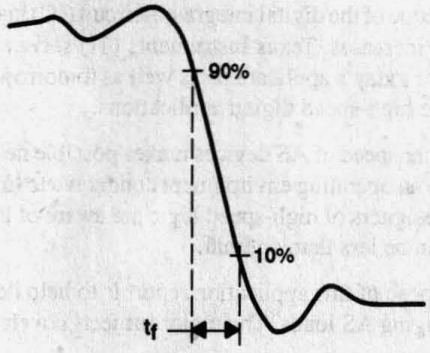
Propagation delay is a function of rise and fall times, ringing, overshoot, undershoot, line length, and fanout. It is important to create a suitable environment to produce propagation delays with acceptable values. Inadequate control of propagation delays can result in skewed signals, causing system failures. Propagation delays also determine the maximum speed of the system.

Rise and Fall Times

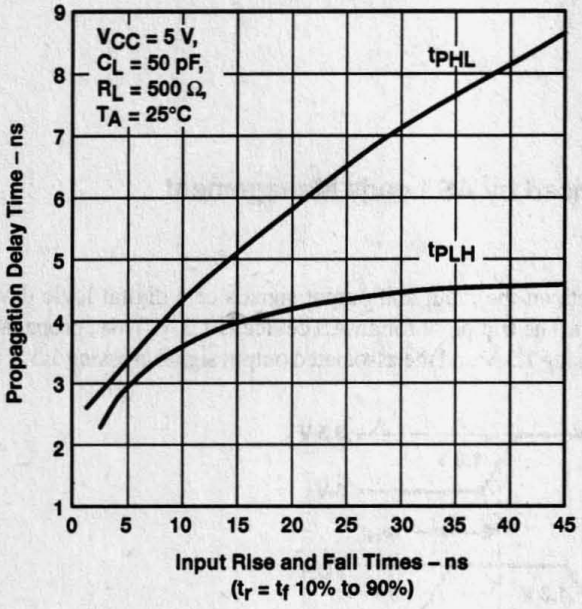
The rise time of an AS waveform (see Figure 2a) is the time a waveform takes to rise from 10% to 90% of its total voltage swing. Likewise, the fall time of an AS waveform (see Figure 2b) is the time a waveform takes to fall from 90% to 10% of its total swing. Figure 2c shows how input rise and fall times affect the propagation delay time of an 'AS804A (hex 2-input inverter). Rise and fall times are shown in Figure 2d. Figure 2 shows two interesting relationships. First, the rise and fall times are not always symmetrical. Second, advances in process technology influence rise and fall times.



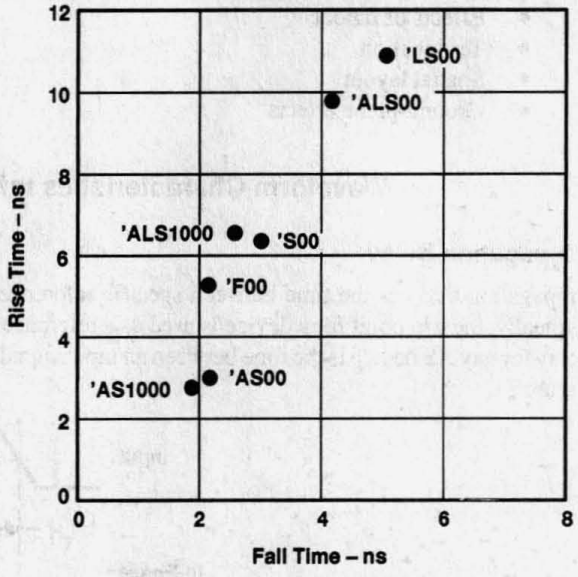
(a) RISE TIME



(b) FALL TIME



(c) PROPAGATION DELAY
AS A FUNCTION OF RISE AND FALL TIMES
('AS804)



(d) RISE AND FALL TIMES FOR TTL FAMILIES

Figure 2. Waveform Characteristics

Ringing

Ringing (in a logic circuit) is the voltage swing above and below a steady-state value occurring after a logic level transition; a typical example is shown in Figure 3. If the amplitude of the voltage swing becomes too high, a loading device may exhibit an undesired response. The bounds of ringing are defined by the maximum overshoot and undershoot values, as explained in the following paragraphs.

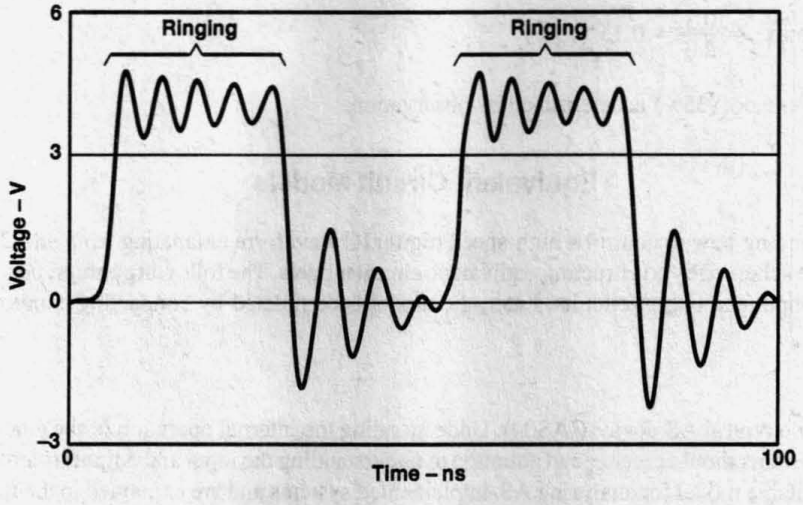


Figure 3. Ringing

Overshoot and Undershoot

In this application report, overshoot is defined as "the peak excursion beyond an expected steady-state value." Likewise, undershoot is "the peak excursion short of an expected steady-state value." Figure 4 illustrates these concepts.

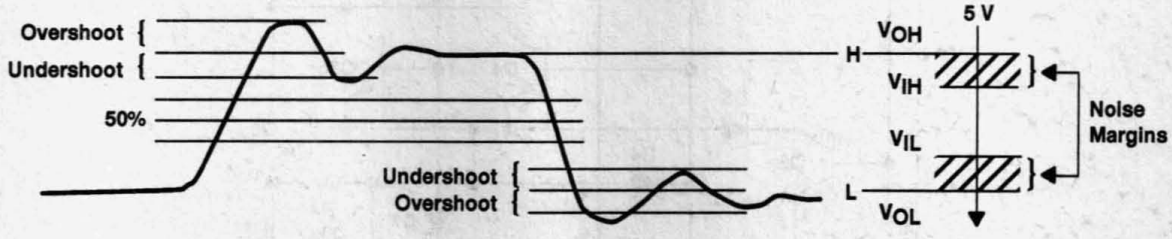


Figure 4. Overshoot and Undershoot

Referring to Figure 4, signal overshoot is defined as either the positive excursion of the signal above the logic 1 level or the negative excursion below the logic 0 level.

The effect of undershoot on the operation of a device is strongly dependent on its noise margin. The noise margin is the amount of noise that can be tolerated before the device begins to switch to a different state (see Figure 4). If the amplitude of the undershoot exceeds the noise margin, the device switches to a different state. If the amplitude of the overshoot is too great, the device may enter an invalid state (latchup) and/or require a finite time to recover before subsequent transitions can occur. The above discussion underlines the importance of minimizing overshoot and undershoot phenomena.

For AS devices, the overshoot should not exceed 35% of the logic voltage swing and undershoot should not exceed 15%. The limiting value for undershoot is determined from the noise margin of a device. Worst-case conditions are:

$V_{IL} \leq 0.8$ V
$V_{OL} \leq 0.5$ V
$V_{IH} \geq 2.0$ V
$V_{OH} \geq 2.5$ V ($V_{CC} = 4.5$ V)

Hence, the largest undershoot allowed before undesired switching would be:

$$V_{IL} - V_{OL} = 0.3 \text{ V}$$

Likewise, the worst-case logic swing for a device family is:

$$V_{OH} - V_{OL} = 2.0 \text{ V}$$

$$\text{Undershoot (max)} = \frac{0.3}{2.0} = 0.15 \ (15\%)$$

The limiting value for overshoot (35%) is determined by observation.

Equivalent Circuit Models

The first step in understanding how to control a high-speed digital IC waveform emanating from an IC is to understand the circuit design. This can be achieved by constructing equivalent-circuit models. The following paragraphs break down the basic logic gate ('AS04) into input and output circuits. Later, the model is completed by connecting components and analyzing the connections.

Logic Gate

Figure 5 is a schematic of a typical AS device ('AS04). Understanding the internal operation of the gate is important, but the designer of high-speed systems should give special attention to understanding the input and output structures. These structures are used to construct a suitable model for analyzing AS-implemented systems and are explained in the following paragraphs.

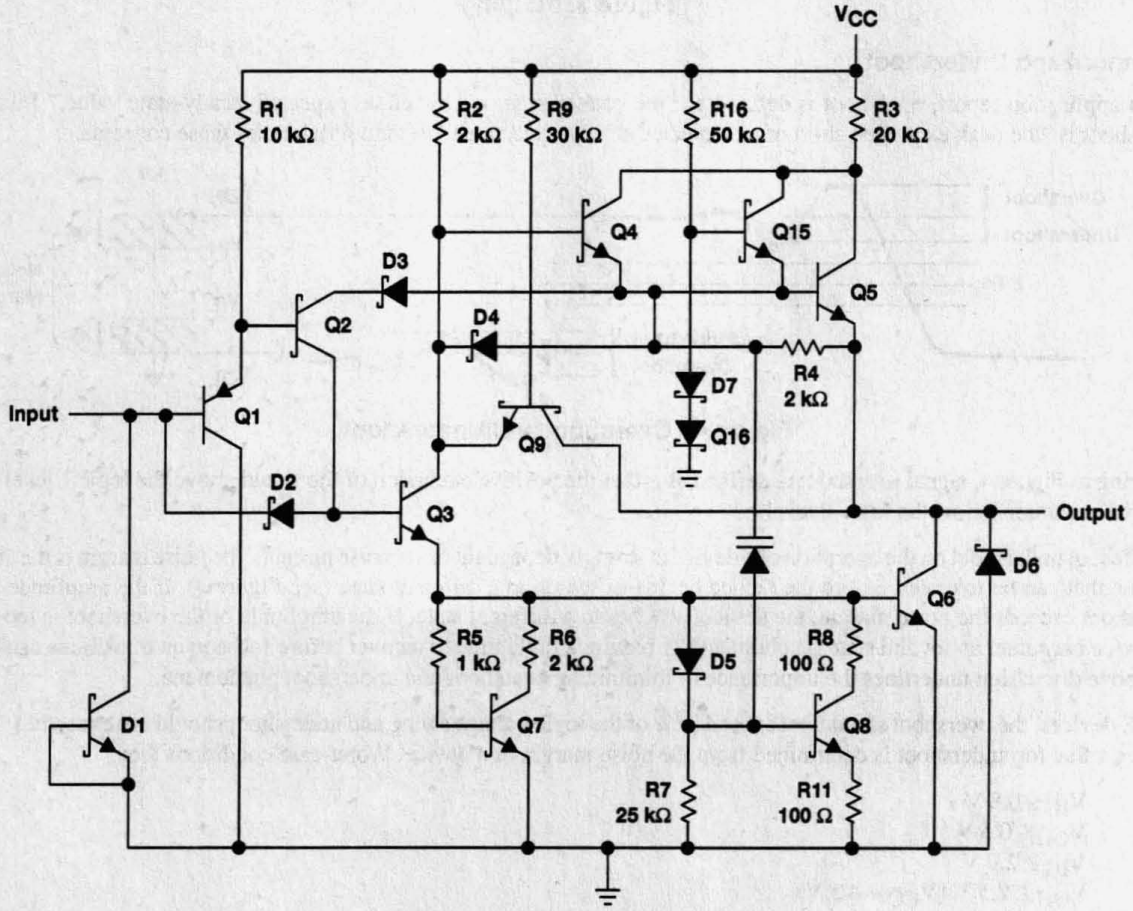


Figure 5. Schematic of 'AS04

The schematic in Figure 5 shows several features of AS gates. These features include ac *miller killers*, zero voltage clamps, ESD protection circuits, and feedback circuitry. TI uses the technological advantages of full Schottky clamping, ion implantation, and oxide isolation to implement these features and thus achieve very fast switching times in a reduced speed-power product. Some benefits are:

- Full Schottky clamping of all saturation transistors virtually eliminates storage of excessive base charge and significantly enhances turn-off time of the transistors.
- Elimination of transistor storage time provides stable switching times across the temperature range.
- An active turnoff squares up the transfer characteristic and provides an improved high-level noise immunity.
- Input and output clamping with Schottky diodes reduces negative-going excursions on the input and outputs.
- The ion implantation process allows smaller geometries with lower parasitic capacitances, thereby decreasing switching times.
- The reduction of the epi-substrate capacitance using oxide isolation also decreases switching times.

Input Equivalent

Isolating the input structure of the 'AS04 simplifies the equivalent input circuit to that shown in the schematic of Figure 6. The string of three diodes (D1, D2, and D3) and the 10-kΩ resistor simulate the loading of the input pnp transistor. D_I provides input clamping and ESD protection. When a negative potential excursion occurs, D_I turns on, clamping the signal voltage to ground. C_I and L_I correspond to the parasitic lead capacitance and inductance, respectively.

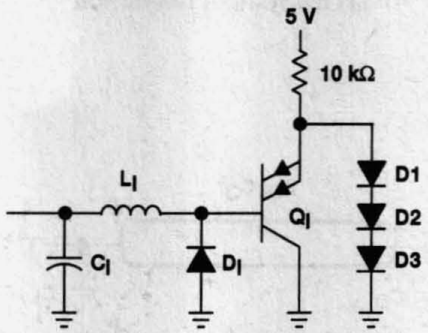
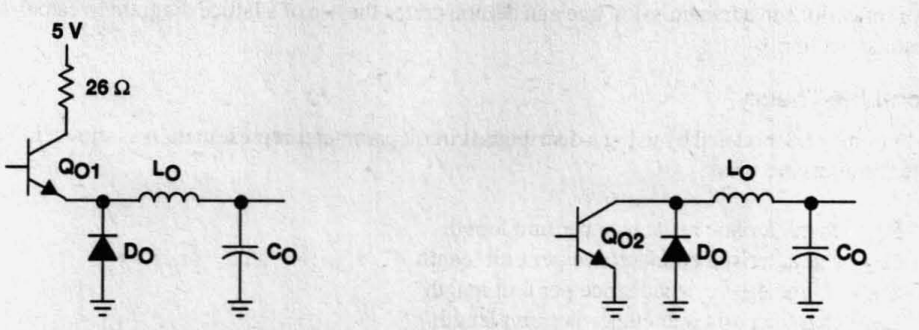


Figure 6. AS Input Structure

Output Equivalent

The output structure of the 'AS04 cannot be simplified as easily as the input structure. Unfortunately, the output impedance of AS devices is not linear or constant. Therefore, a single circuit cannot completely model the output structure. However, modeling of equivalent circuits can be based on the transition being investigated. Figure 7a shows the equivalent output circuit with a low-to-high transition, while Figure 7b shows the equivalent output circuit with a high-to-low transition. D_O simulates a zero-clamp circuit to clamp out negative-going potential excursions. C_O and L_O account for the parasitic lead impedances of the package. While Q_{O1} and Q_{O2} function basically as switches, their bipolar characteristics simulate the switching characteristics of the AS device.



(a) LOW-TO-HIGH TRANSITION MODEL (b) HIGH-TO-LOW TRANSITION MODEL

Figure 7. AS Output Structure

AS System Model

A combination of the equivalent circuits shown in Figures 6 and 7 can model a typical AS system (shown in Figures 8a and 8b). In these models, transmission lines connect AS devices. However, under certain circumstances any line can be modeled as a transmission line. The effects of transmission lines is discussed later.

To test the validity of the model in Figure 8, an experiment was set up comparing a computer-simulated waveform with one observed in a real environment.[1] The resulting data are in Appendix A. Briefly, there exists enough correlation to accept the models as presented in the following paragraphs.

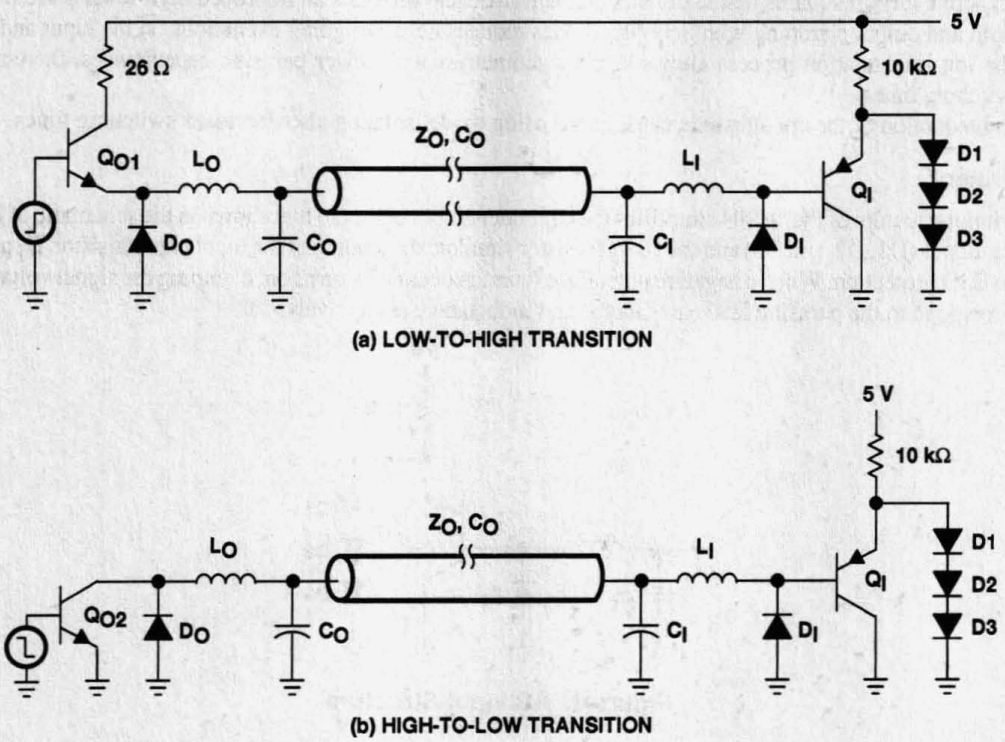


Figure 8. AS System Model

Transmission Lines

Understanding the effects of transmission lines is necessary in any high-speed digital design. Any conductor can exhibit transmission-line effects if certain conditions exist. The following section describes a general model for transmission lines and provides a more detailed analysis of two types of transmission lines — microstrip lines and strip lines. It also explains the phenomenon of reflections in a transmission line and demonstrates the use of a lattice diagram to calculate total voltage at any point in a transmission line.

Transmission-Line Theory

Transmission lines may be modeled by using a distributed circuit parameter representation as shown in Figure 9. In the figure, the following definitions are used:

R_O = characteristic resistance per unit length
G_O = characteristic conductance per unit length
C_O = characteristic capacitance per unit length
L_O = characteristic inductance per unit length
dx = a unit length of transmission line

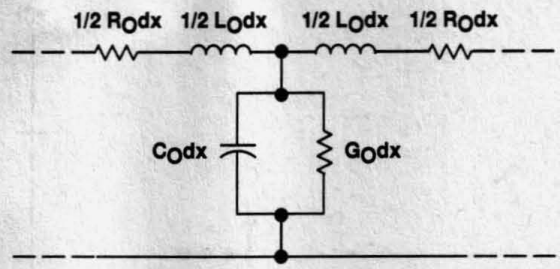


Figure 9. Transmission-Line Components

A finite length of cable can be regarded as an infinite number of differentially small circuits as shown in Figure 9. From this model, we can derive the following differential equation:

$$\frac{d^2v}{dx^2} = L_oC_o\frac{dv^2}{dt^2} + (R_oC_o + L_oG_o)\frac{dv}{dt} + R_oG_ov \quad (1)$$

If the resistive and conductive components of the transmission-line model are neglected (i.e., a lossless line assumed), equation 2 results. For the scope of this analysis, this assumption is valid; the resistive and conductive components are very small, and result in very small potential differences compared to ordinary AS voltage levels.

$$\frac{d^2v}{dx^2} = L_oC_o\frac{d^2v}{dt^2} \quad (2)$$

The general solution of the wave equation is the impulse response of the transmission line. By convolving the impulse response with the actual input to the transmission line, the actual response to any input can be determined. A Fourier analysis provides insight into the impulse response of the transmission-line model, allowing the designer to (1) solve the wave equation, (2) perform convolution easily, and (3) study different characteristics of the resulting signal while remaining in the Fourier domain. Appendix B details the derivation of the impulse response, V(x,t).

$$V(x,t) = \delta(x - vt) \quad (3)$$

Where:

V(x,t) = voltage, a function of time and space

v = velocity = $\frac{1}{\sqrt{L_oC_o}}$

x = space variable ($x \geq 0$)

t = time variable ($t \geq 0$)

δ = Dirac or impulse function

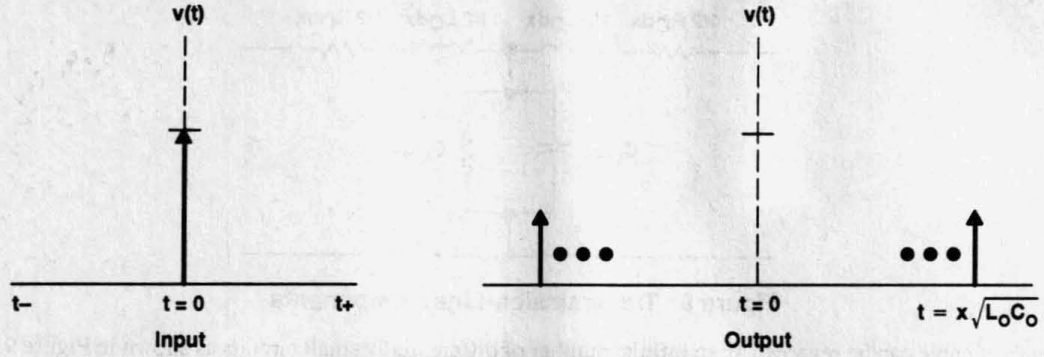
Interpreting the analysis in Appendix B, the impulse response is defined to have an amplitude when x = vt, or when:

$$\frac{x}{t} = \frac{1}{\sqrt{L_oC_o}} \quad (4)$$

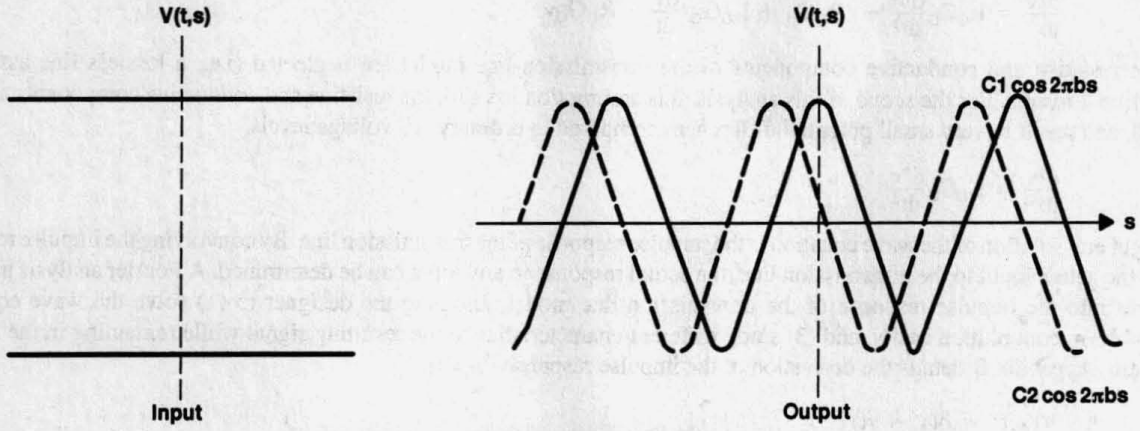
Physically, this represents an impulse traveling down the transmission line with velocity determined by the following equation:

$$v = \frac{1}{\sqrt{L_oC_o}} \quad (5)$$

Figure 10a shows the input signal and its associated output signal in the time domain. Figure 10b shows the input and output signals as represented in the Fourier domain.



(a) WAVEFORMS IN THE TIME DOMAIN



(b) WAVEFORMS IN THE FOURIER DOMAIN

Figure 10. Waveforms in the Time and Fourier Domains

If an input signal is defined as:

$$V_s(t) = V(t)\ H(t) \tag{6}$$

Where:

$H(t) = 1\ (t > 0)$
$H(t) = 0\ (t < 0)$

and the impulse response is convoluted (as shown in Appendix B), the resulting signal can be solved for in the time domain:

$$V(x, t) = V(x - vt)\ H(x - vt) \tag{7}$$

or:

$$V(x, t) = V\left(t - xt_{pd}\right) H\left(t - xt_{pd}\right) \tag{8}$$

Where:

$$t_{pd} = \frac{1}{v}$$

The transmission line passes the signal undistorted at a velocity determined by:

$$v = \frac{1}{\sqrt{L_o C_o}} \tag{9}$$

An identical analysis involving current instead of voltage provides a resulting impulse response in the time domain.

Dividing the voltage response by the current response yields the characteristic impedance (Z_O).

$$Z_O = \sqrt{\frac{L_O}{C_O}} \tag{10}$$

The results lead to the further conclusion that given any input signal, Vs(t), the transmission line responds by passing the input delayed by:

$$t_{pd} = \sqrt{L_O C_O} \tag{11}$$

$$t_{pd} = Z_O C_O \tag{12}$$

Here, t_{pd} has units of time per unit length. If a line length of L is assumed, the actual time can be defined by the following:

$$T_{pd} = L\ t_{pd} \tag{13}$$

In equation 13 and the remainder of this report, the uppercase T_{pd} indicates units of time; lowercase t_{pd} indicates units of time per unit length.

Transmission-Line Types

Although many different types of transmission lines (conductors) exist, this report discusses only the two most commonly found on PC boards: microstrip lines and strip lines.

Microstrip Lines

A microstrip line consists of a signal conductor separated from a ground plane by a dielectric insulating material. The characteristic impedance of a microstrip line is given by:

$$Z_O \simeq \frac{87}{er + 1.41} \ln\frac{5.98\ H}{0.8\ W + T} \quad \text{(Blood 1983)} \tag{14}$$

Where:

er = relative dielectric constant of the board material (about 5 for G-10 fiberglass-epoxy boards)
W, H, T = dimensions (in mils) as indicated in Figure 11

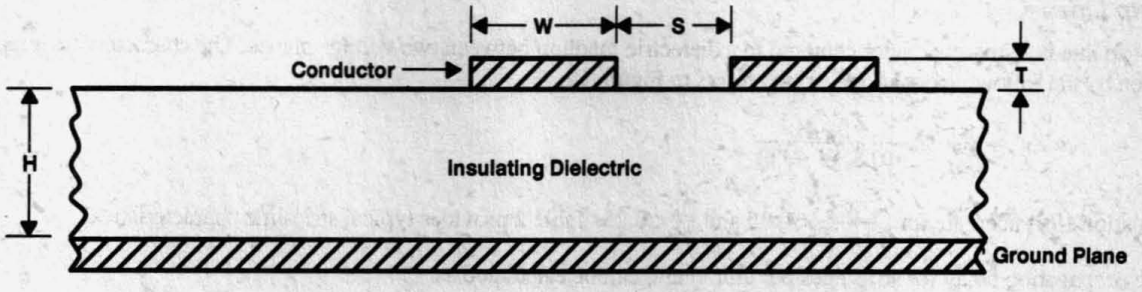


Figure 11. Microstrip-Line Structure

Equation 14 is adequate for $0.1 \le W/H \le 3.0$ and for $1 \le er \le 15$. Table 1 provides typical microstrip-line characteristics.

Table 1. Typical Microstrip-Line Characteristics

DIMENSIONS (mils)		LINE IMPEDANCE Z_O (Ω)	CAPACITANCE C_O (pF/in)
H	W		
6	20	35	3.33
6	15	40	2.92
15	20	56	2.50
15	15	65	2.17
30	20	80	1.67
30	15	89	1.50
60	20	104	1.33
60	15	113	1.17
100	20	121	1.08
100	15	130	1.00

NOTE: er = 5, T = 1.50

The propagation delay can be calculated as:

$$t_{pd} \simeq 1.017\sqrt{0.475er + 0.67} \text{ ns/ft} \quad (15)$$

or:

$$t_{pd} \simeq 3.34\sqrt{0.475er + 0.67} \text{ ns/m} \quad (16)$$

Using the typical value of 5 for er, the propagation delay for microstrip lines is calculated as:

$$t_{pd} \simeq 1.77 \text{ ns/ft} \quad (17)$$

or:

$$t_{pd} \simeq 5.81 \text{ ns/m} \quad (18)$$

Strip Lines

A strip line is a strip conductor centered in a dielectric medium between two voltage planes. The characteristic impedance is given by the following equation[1], which refers to Figure 12:

$$Z_O \simeq \frac{60}{\sqrt{er}} \ln\frac{5.98\ H}{\pi(0.8\ W + T)} \quad (19)$$

Equation 19 is accurate for $\frac{W}{H - T} < 0.35$ and $\frac{T}{H} < 0.25$. Table 2 provides typical strip-line characteristics.

The propagation delay for strip lines per unit length can be calculated as:

$$t_{pd} \simeq 1.017\sqrt{er} \text{ ns/ft} \quad (20)$$

or:

$$t_{pd} \simeq 3.34\sqrt{er} \text{ ns/m} \quad (21)$$

For G-10 fiberglass-epoxy board, the propagation delay reduces to:

$$t_{pd} \simeq 2.26 \text{ ns/ft} \quad (22)$$

or:

$$t_{pd} \simeq 7.41 \text{ ns/m} \quad (23)$$

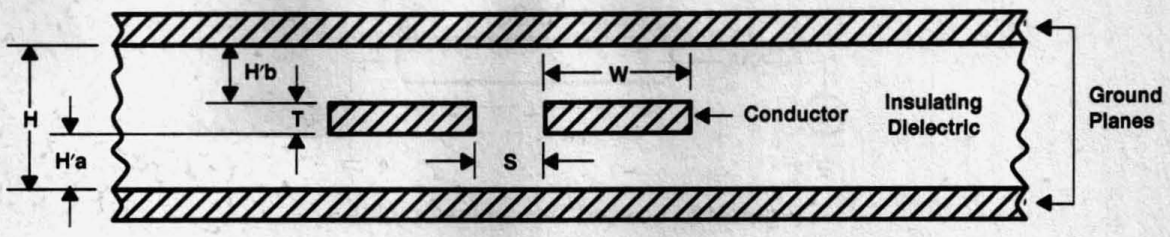


Figure 12. Strip-Line Structure

Table 2. Typical Strip-Line Characteristics

DIMENSIONS (mils)		LINE IMPEDANCE Z_O (Ω)	CAPACITANCE C_O (pF/in)
H	W		
6	20	27	6.67
6	15	32	5.83
10	20	34	5.58
10	15	40	4.67
12	20	37	4.75
12	15	43	4.00
20	20	44	4.00
20	15	51	3.50
30	20	55	3.25
30	15	61	2.92

NOTE: er = 5, T = 1.50, H'a = H'b

Reflections

If a load, Z_L, exists on a transmission line such that $Z_L \neq Z_O$, a waveform reflects into the transmission line upon encountering the load. The magnitude of reflection is normally defined by a reflection coefficient. The reflection coefficient (Γ) at the load is derived by use of Ohm's Law. If V_i is the incident voltage and V_r is the reflected voltage, the following equation must be true at node B of Figure 13:

$$V_i + V_r = \left(\frac{V_i}{Z_O} - \frac{V_r}{Z_O}\right)Z_L \tag{24}$$

Therefore, Γ, defined as $\frac{V_r}{V_i}$ is:

$$\Gamma_{load} = \frac{Z_{load} - Z_O}{Z_{load} + Z_O} \tag{25}$$

Likewise,

$$\Gamma_{source} = \frac{Z_{source} - Z_O}{Z_{source} + Z_O} \tag{26}$$

The amount of reflection voltage (V_r) is given by V_i, the voltage incident at the point of reflection.

The model of the transmission line can now be completed. In Figure 13, the voltage seen at point A is given by equation 27:

$$V_a = V_S\frac{Z_O}{Z_O + Z_S} \tag{27}$$

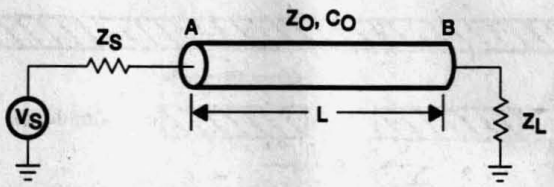


Figure 13. Loaded Transmission Line

Then V_a enters the transmission line and appears at point B delayed by T_{pd}.

$$V_b = V_a(x - vt)\ H(x - vt) \tag{28}$$

For equation 28, x is the distance along the transmission line from point A. The waveform then encounters the load Z_L, and a reflection can occur. The reflected wave enters the transmission line at point B and appears at point A T_{pd} (or L t_{pd}) later.

$$V_{r1} = \Gamma_{load} V_b \tag{29}$$

The process continues indefinitely.

$$V_{r2} = V_{r1}\Gamma_{source} \tag{30}$$

If each reflected waveform is treated as a separate source, dependent on the reflection coefficient at that end and the incident waveform, superposition can be applied to develop equation 31, which describes the waveform seen at any point on the transmission line at any given time.

$$\begin{aligned} V(x,t) = {} & \frac{Z_O}{Z_O + Z_S}[V(x - vt)]\ [H(x - vt)] \\ & + \Gamma_l\{V[x - (2L + vt)]\}\ \{H[x - (2L + vt)]\} \\ & + \Gamma_l\Gamma_s\{V[x - (2L - vt)]\}\ \{H[x - (2L - vt)]\} \\ & + \Gamma_l\Gamma_s\{V[x - (4L - vt)]\}\ \{H[x - (4L - vt)]\} \\ & + \Gamma_l^2\,\Gamma_s^2\{V[x - (4L + vt)]\}\ \{H[x - (4L + vt)]\} + \ldots \end{aligned} \tag{31}$$

Each reflection is added to the total voltage through the unit step function, H(t). Alternately, equation 31 can be rewritten as:

$$\begin{aligned} V(x,t) = {} & \frac{Z_O}{Z_O + Z_S}\left[V\left(t - t_{pd}x\right)\right]\ \left[H\left(t - t_{pd}x\right)\right] \\ & + \Gamma_l\left\{V\left[t - t_{pd}(2L - x)\right]\right\}\ \left\{H\left[t - t_{pd}(2L - x)\right]\right\} \\ & + \Gamma_l\Gamma_s\left\{V\left[t - t_{pd}(2L + x)\right]\right\}\ \left\{H\left[t - t_{pd}(2L + x)\right]\right\} \\ & + \Gamma_l\Gamma_s\left\{V\left[t - t_{pd}(4L - x)\right]\right\}\ \left\{H\left[t - t_{pd}(4L - x)\right]\right\} \\ & + \Gamma_l^2\,\Gamma_s^2\left\{V\left[t - t_{pd}(4L + x)\right]\right\}\ \left\{H\left[t - t_{pd}(4L + x)\right]\right\} + \ldots \end{aligned} \tag{32}$$

With this equation, the potential now can be followed along any point of the transmission line in time. Thus, the model for an entire system has been completed.

Lattice Diagrams

The lattice diagram is a convenient tool for calculating the total voltage as described by equations 31 and 32. Two vertical lines are drawn to represent points A and B on the horizontal dimension, x. The vertical dimension then represents time. Thus, a waveform travels back and forth between points A and B in time, producing the lattice diagram shown in Figure 14. The voltage at a given point can be calculated as the sum of all the individual reflected voltages up to that time. Notice that at each discontinuity, two waves are converging: the incident wave and the reflected wave. Therefore, the voltage at the endpoints A or B at the time of the waveform reflection would be calculated by summing both the incident and reflected waves up to and including the point in question.

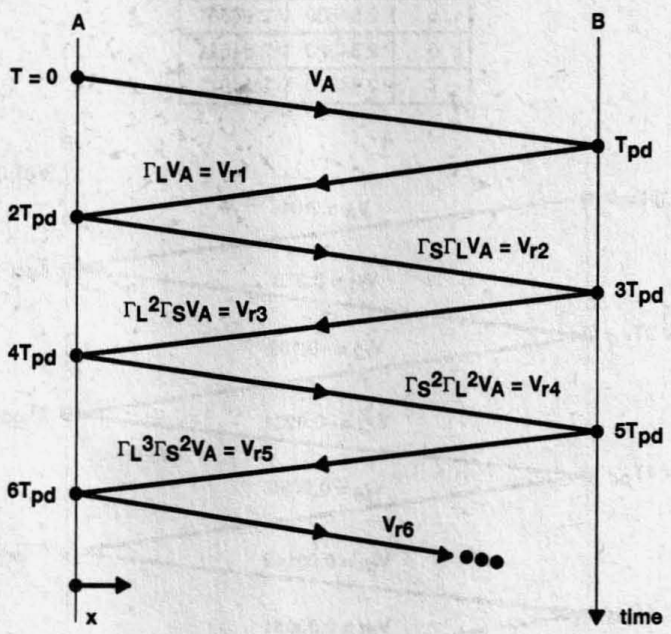


Figure 14. Lattice Diagram

As an example, let the simple configuration shown in Figure 13 be assumed. Let $R_S = 30\ \Omega$ (a typical high-state AS source impedance) and let $R_L = 100\ \Omega$ (arbitrarily). Finally, let $Z_O = 75\ \Omega$. The appropriate reflection coefficients can be calculated as:

$$Z_O = 75\ \Omega$$
$$Z_{source} = 30\ \Omega$$
$$Z_{load} = 100\ \Omega$$

$$\Gamma_{source} = \frac{30 - 75}{30 + 75} = -0.42857$$
$$\Gamma_{load} = \frac{100 - 75}{100 + 75} = 0.14286$$

$$V_S = 3.70000\ V$$
$$V_a = V_s \frac{75}{75 + 30} = 2.64286\ V$$
$$V_{r1} = 2.64286 \times 0.14286 = 0.37755\ V$$
$$V_{r2} = 0.37755 \times -0.42857 = -0.16181\ V$$
$$V_{r3} = -0.16181 \times 0.14286 = -0.02312\ V$$
$$V_{r4} = -0.02312 \times -0.42857 = 0.00991\ V$$
$$V_{r5} = 0.00991 \times 0.14286 = 0.00142\ V$$
$$V_{r6} = 0.00142 \times -0.42857 = -0.00061\ V$$
$$V_{r7} = -0.00061 \times 0.14286 = -0.00009\ V$$

Thus, the voltage at point B can be tabulated as shown in Table 3. The corresponding lattice diagram is shown in Figure 15.

Table 3. Voltage at End Points A and B

T_{pd}	V(A,t)	V(B,t)
0	2.64286	0
1	2.64286	3.02041
2	2.85860	3.02041
3	2.85860	2.83549
4	2.84539	2.83549
5	2.84539	2.84681
6	2.84620	2.84681
7	2.84620	2.84611

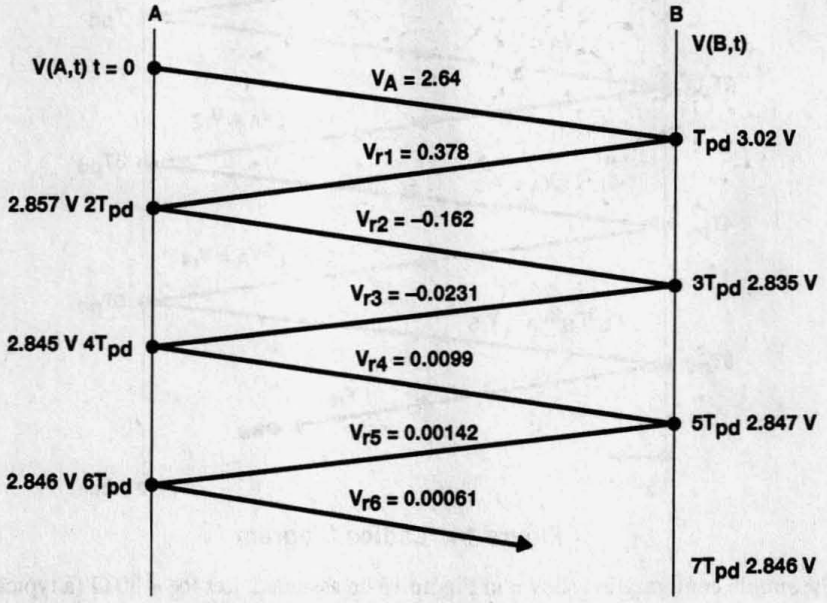


Figure 15. Lattice Diagram Example

Fanout

The fanout of a device is defined as the number of other devices it can drive. While the fanout of a device is specified by the manufacturer, the effects of fanout on the waveform of a device are not. Fanout affects the transmission-line model, the propagation delay as seen by the system, the rise and fall times of system waveforms, and the proposed solutions to control overshoot and undershoot. Therefore, it is important that these effects be kept in mind.

Influence on Transmission-Line Model

A device driving more than one other device is said to have a fanout of more than one. The configuration of the loading devices is important. If the loading devices are all lumped at the end of the transmission line (see Figure 16 for lumped loading), the transmission model developed above is still valid. However, a correction is required because of the excess capacitance at the load.[2] This correction is also dependent on the type of termination scheme, as discussed in the following paragraphs.

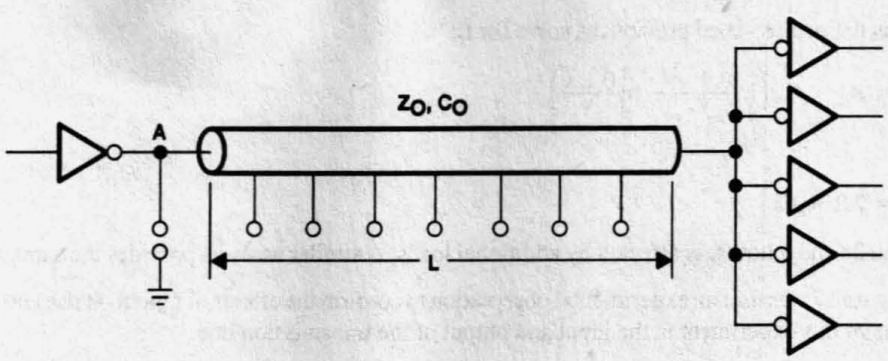


Figure 16. Transmission Line With Lumped Loading

If the loading devices are approximately equally spaced along the length of the transmission line, the model must be altered regardless of the termination scheme.

The input equivalent models of AS devices discussed above show that the impedance of a loading device is very high and can be considered here as purely capacitive. This is especially true when AS devices operate at high speeds. Therefore, each load is seen by the driving device as a capacitor, C_n, to ground. If the loads are distributed evenly, d inches apart, the characteristic capacitance (C_O) is increased from C_O to $C_O + C_d$, where C_d is C_n/d.

$$Z_O = \sqrt{\frac{L_O}{C_O + C_d}} \tag{33}$$

and:

$$t_{pd} = \sqrt{L_O(C_O + C_d)} \tag{34}$$

or:

$$t_{pd}(\text{new}) = t_{pd}(\text{old}) \sqrt{1 + \frac{C_d}{C_O}} \tag{35}$$

Equations 34 and 35 clearly show that the propagation delay of the waveform on the transmission line increases, that is, the velocity of the propagating signal decreases as each load is added to the line.

Influence on Rise and Fall Times

The rise and fall times of a signal are also affected by fanout, both adversely (for both lumped and distributed loads). Yeargan[1] treats the output waveform (V_O) as an exponential with a time constant defined by R_S and C_{eq}:

$$V_O = V\left(1 - \exp\frac{-t}{R_S C_{eq}}\right) \tag{36}$$

Where:

$C_{eq} = C_O = nC_n$
R_S = output impedance of the driving gate
n = number of loads on the transmission line

If the rise time is defined as stated previously, solve for t_r:

$$t_r = R_S \times C_{eq}\left(\ln\frac{0.9\ v}{v} - \ln\frac{0.1\ v}{v}\right) \quad (37)$$

or:

$$t_r = 2.2\ R_S C_{eq} \quad (38)$$

Equations 37 and 38 show how t_r is affected by additional loads. A similar analysis provides the same relation for fall times.

The circuit in Figure 17 was used in experimental observation to confirm the effects of fanout on rise and fall times.[1] Figure 18 shows the results of this experiment at the input and output of the transmission line.

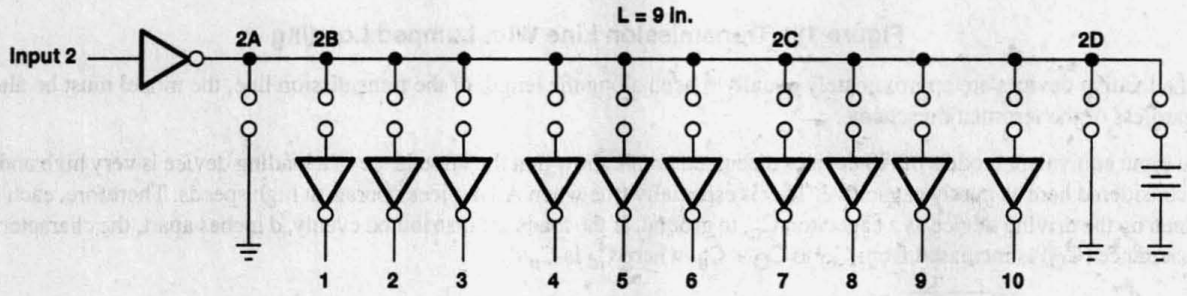


Figure 17. Schematic Diagram of a Distributed Loaded System

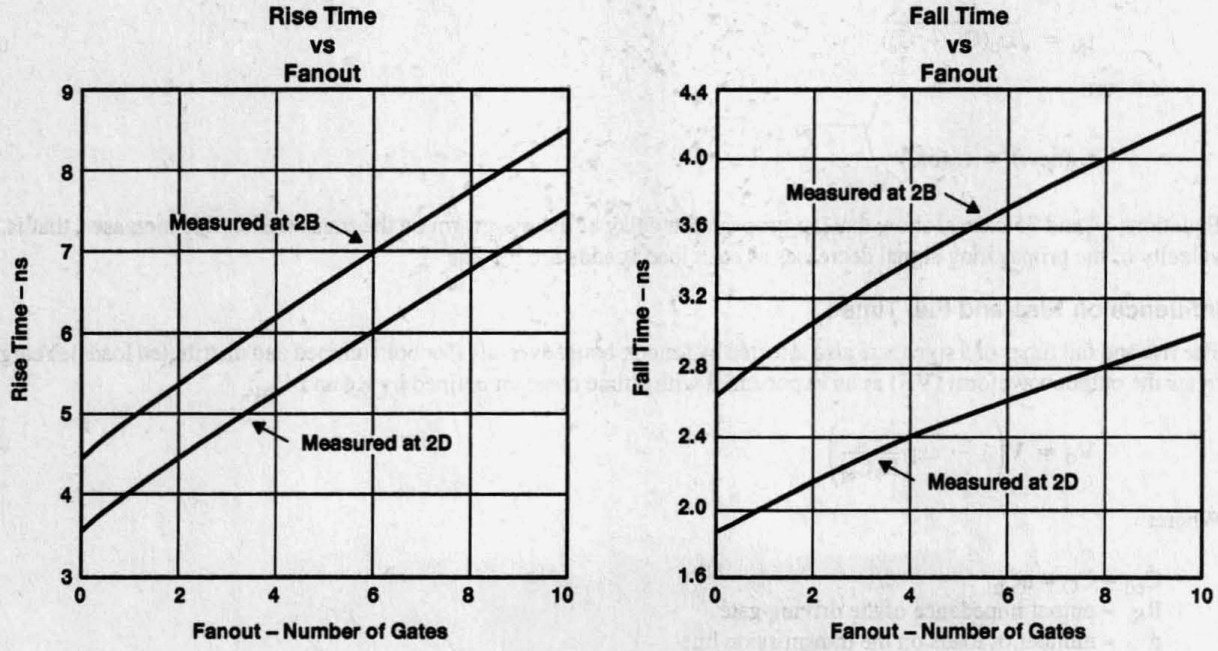


Figure 18. Rise Time and Fall Time Versus Fanout

Combined Effects on Propagation Delay

As stated previously, propagation delay is a function of rise and fall times, as well as the characteristic impedance of the transmission line. If both are affected by fanout (distributed loads), the propagation delay of these factors is also affected. The experimental circuit shown in Figure 17 confirms this effect on propagation delay.[1] Figure 19 plots the relationship of propagation delay and fanout.

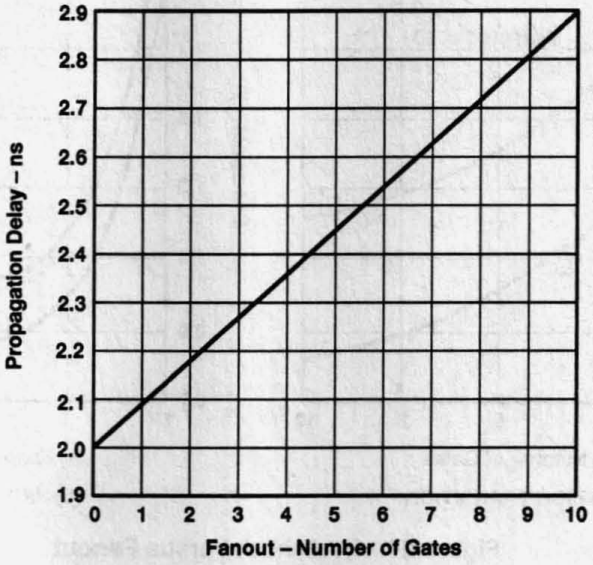


Figure 19. Propagation Delay Versus Fanout

Influence on Ringing

Finally, fanout influences the overshoot and undershoot characteristics of the waveform. That is, overshoot and undershoot are dependent on the characteristic impedance of the transmission line. Figure 20 shows an example of a waveform derived from the lattice diagram example in Figure 15. The lattice diagram shows how the waveform reacts with the reflection coefficients, which are dependent on Z_O. Overshoot is very dependent on Γ_{load}.

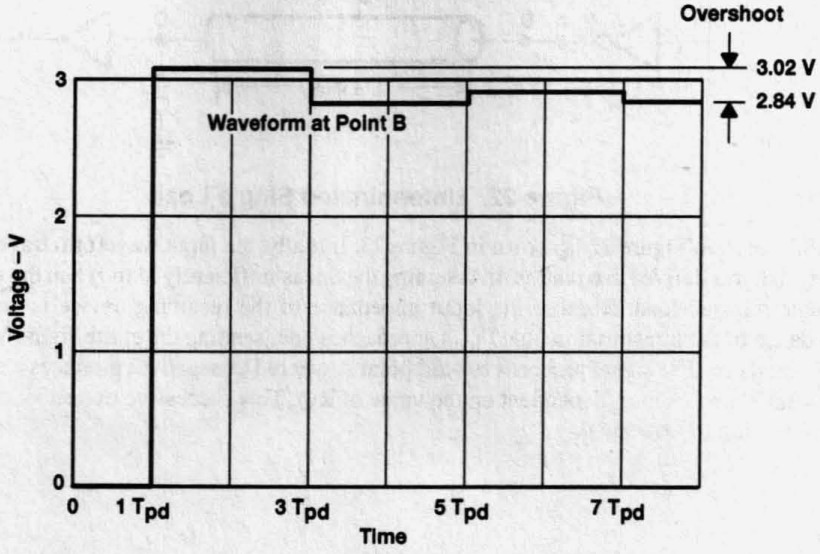


Figure 20. Waveform Derived From Lattice Example

Figure 21 shows the influence of fanout on overshoot in the test circuit of Figure 17. As fanout increases, Z_O decreases, Γ_{load} decreases, and overshoot decreases. If the reflected overshoot decreases, the subsequent undershoot decreases as well.

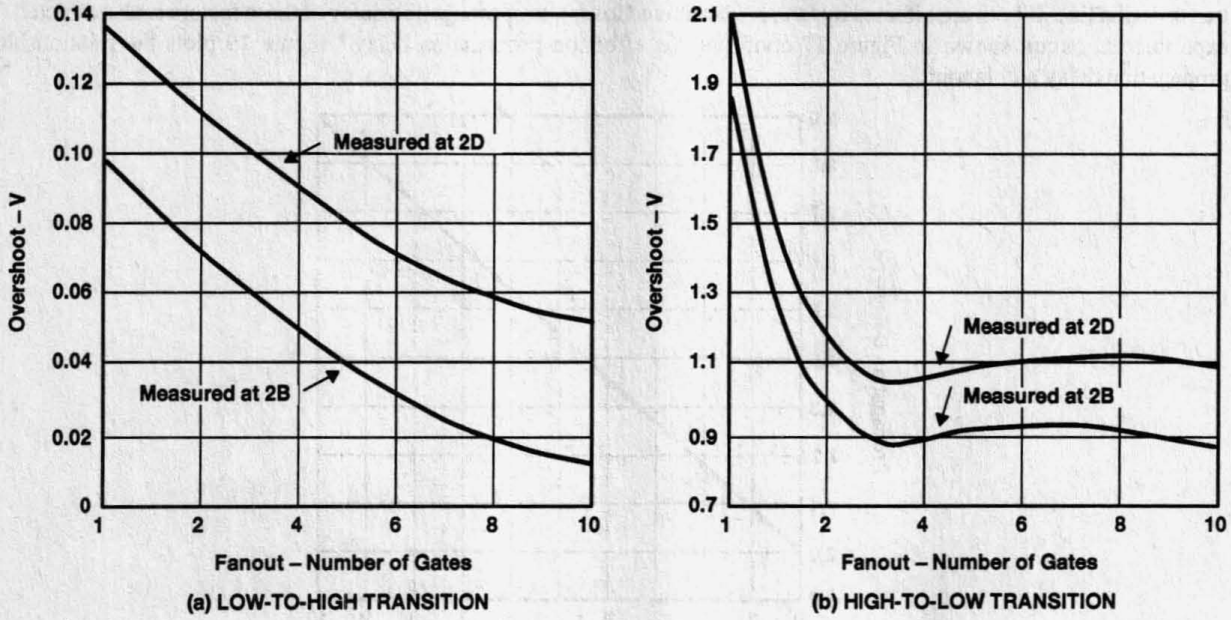


Figure 21. Overshoot Versus Fanout

Termination

When Termination is Needed

The preceding analysis and derivations can be used to predict how a signal reacts to certain environments. Figure 22 shows an unterminated line with a single load.

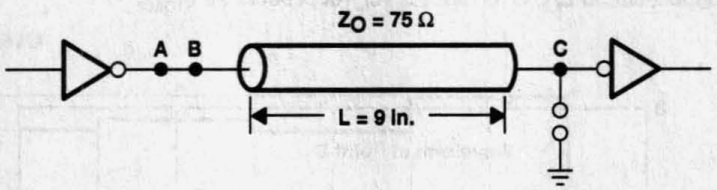


Figure 22. Unterminated Single Load

The waveform of the circuit in Figure 22 is shown in Figure 23. Initially, the input waveform travels down the transmission line with the velocity that was derived in equation 4. Assuming the line is sufficiently long, when the waveform reaches point C it encounters the unterminated load. Because the input impedance of the receiving device is very high compared to the characteristic impedance of the transmission line, Γ_{load} approaches one, sending the entire signal V_O back to the source and resulting in a large overshoot. The signal proceeds toward point A where Γ_s (negative) produces a negative-going reflection, thus creating a substantial undershoot (dependent on the value of R_S). This successive overshoot and undershoot continues, and the phenomenon of ringing occurs.

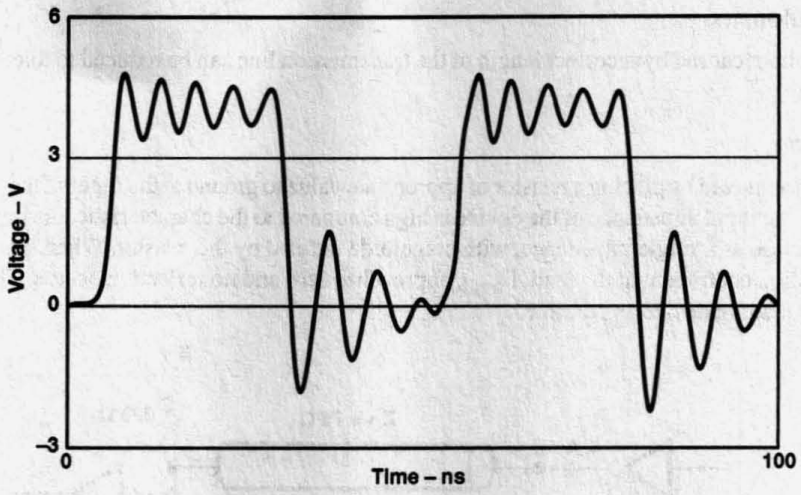


Figure 23. Unterminated Single-Load Waveform

If the line is sufficiently short, reflections are part of the rise time of the signal. Being part of the rise or fall time, the reflections do not contribute to overshoot or undershoot. Hence, if the length of the transmission line is shorter than l_{max} (see equation 39), overshoot and undershoot are held to less than 15% of the logic swing.[3]

$$l_{max} \leq \frac{t_r}{2t_{pd}} \tag{39}$$

Where:

t_r = rise time of the signal
$t_{pd} = Z_O C_O$

and:

Z_O = characteristic line impedance
C_O = equivalent capacitance per unit length of the line

If the line is longer than l_{max}, termination is required to reduce overshoot and undershoot (i.e., ringing). Table 4 is a good guide to deciding when termination is needed. It shows the longest unterminated length of transmission line, given its characteristics and the fanout. The values are derived from the preceding analysis and are observed to be approximately correct. It is important to reduce these values by 10% for added margin.

Table 4. Maximum Line Length Without Termination

FANOUT	1	2	4	8	Z_O
C_{pd} (pF)	4.70	9.40	18.80	37.60	(Ω)
Microstrip 0.15 t_{pd} (ns/in)† (maximum length in inches)	9.37	8.67	7.45	5.61	50
	9.11	8.20	6.70	4.68	68
	9.01	8.03	6.44	4.38	75
	8.92	7.86	6.19	4.12	82
	8.81	7.67	5.92	3.85	90
	8.67	7.45	5.61	3.55	100
Strip 0.19 t_{pd} (ns/in)† (maximum length in inches)	7.38	6.83	5.86	4.42	50
	7.17	6.46	5.27	3.68	68
	7.10	6.32	5.07	3.45	75
	7.02	6.19	4.87	3.24	82
	6.93	6.04	4.66	3.03	90
	6.83	5.86	4.42	2.79	100

† t_r = 4 ns

Resistive Termination

Overshoot and undershoot caused by incorrect length of the transmission line can be reduced to tolerable levels by the c[illegible] choice of termination.

Parallel Termination

Parallel termination is achieved by placing a resistor of appropriate value to ground at the input of the loading device, as shown in Figure 24. Because the input impedance of the device is high compared to the characteristic line impedance, the resistor and device in parallel function as a single impedance, with magnitude defined by the resistor. When the resistor matches the line impedance, the reflection coefficient at the load, Γ_{load}, approaches zero and no reflection occurs. The termination should be placed as close to the loading device as possible.

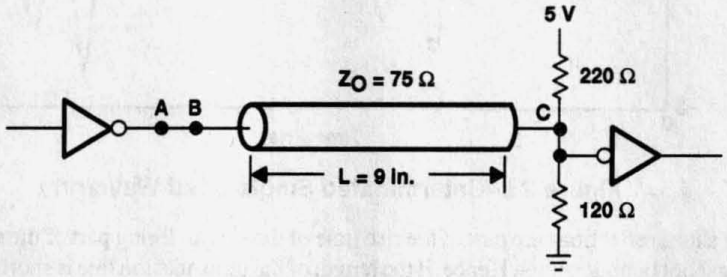


Figure 24. Parallel Termination

Blood[2] highlights an important feature of parallel termination: an undistorted waveform along the entire line. Another feature is that loading a long line (fanout greater than one, lumped at the end of the line) while using parallel termination does not affect rise and fall times or the propagation delay of the driving device. Figure 25 shows the waveforms observed from the transmission line in Figure 24 with parallel termination.

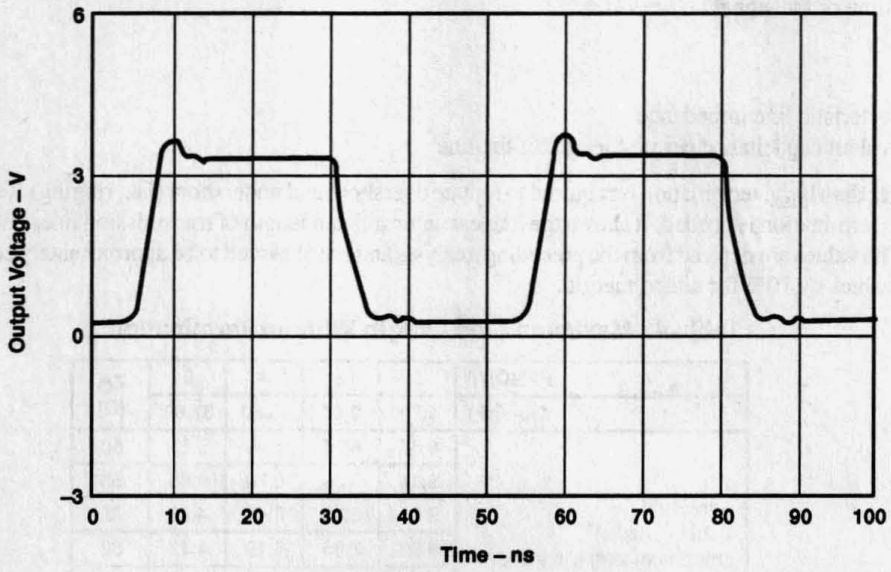


Figure 25. Parallel-Termination Waveform

Series Termination

Ringing on longer lines may also be controlled by using a series termination technique. Series termination is accomplished by putting a resistor in series with the transmission line at the driving device. This is also known as series damping. The value of the resistor plus the impedance looking into the driving device should approximate the impedance of the transmitting line as closely as possible. When this condition is obtained, the reflection coefficient at the source goes to zero and the ringing is damped out. See Figure 26 for an example of series termination.

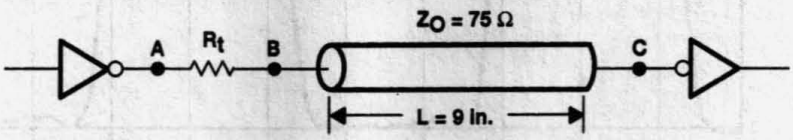


Figure 26. Series Termination

At t0, the voltage at point A is V_S. The voltage at point B (at t0+) is given by equation 40:

$$V_b = V_a \frac{Z_O}{R_t + R_S + Z_O} \tag{40}$$

$$V_b = \frac{V_a}{2} \tag{41}$$

Half the signal is propagated to the load, whose reflection coefficient sends the entire signal back into the transmission line, effectively doubling the signal.

$$V_{rl} = V_b \tag{42}$$

$$V(x, T_{pd}+) = V_b + V_{rl} = V_a \tag{43}$$

The zero-reflection coefficient at the source prevents further reflections, thereby leaving the value of the voltage on the transmission line at the desired potential.

Series termination requires no additional power supplies, making it an attractive alternative to parallel termination schemes. However, the designer should not use distributed loading because, as shown in Figure 27, the waveforms are not undistorted along the entire length of the line.[2] Instead, lumped loading can be used with any number of loading devices at the receiving end. In this and all cases, the designer should always be sure the driving gate can supply enough current for its application and to ensure proper V_{OH} and V_{OL} levels on the line. Figure 28 shows the waveform of the circuit shown in Figure 26.

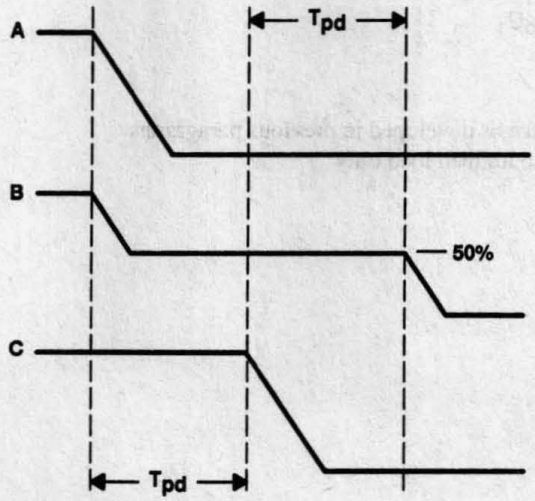


Figure 27. Relation of Series-Termination Waveforms

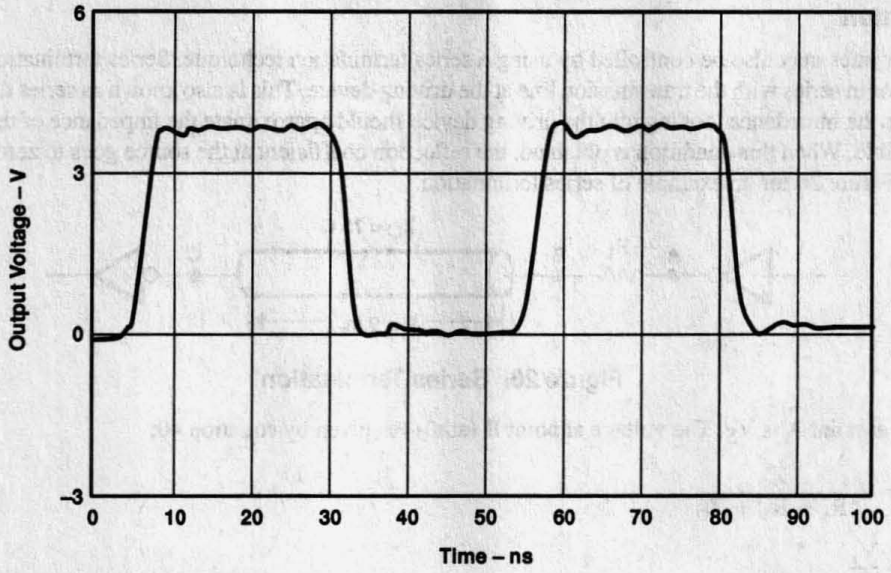


Figure 28. Series-Termination Waveform

Series termination does affect the propagation delay of a loaded system. In fact, a system with series termination experiences twice the loading effect than a system with parallel termination.[2] That is, when lumped loading is present, the increase in rise and fall times of the signal increases the propagation delay. Again, series termination is appropriate only for fanouts of one or more (lumped at the end of the line). However, as the fanout increases, the propagation delay of the waveform increases.

Fanout Correction

The propagation delay for lumped loads requires a correction and is dependent on the type of termination used. The correction is:

For series termination:

$$t_{pd} = Z_O C_O + 0.7 Z_O C_T \quad (44)$$

For parallel termination:

$$t_{pd} = Z_O C_O + 0.35 Z_O C_T \quad (45)$$

Where:

Z_O = characteristic impedance as developed in previous paragraphs
C_T = total capacitance due to lumped load only

Diode Termination

The parallel and series terminations previously discussed are passive. However, power-supply constraints often lead the designer to use diodes as a termination alternative. This technique is called active termination.

Two Schottky diodes placed as shown in Figure 29 effectively reduce ringing. Several advantages are gained by this use of active termination[2]:

- No matched-impedance strip lines are required.
- No line-matching termination resistors are required.
- All overshoots, undershoots, or external noise are clamped to safe voltage-excursion levels.
- The total cost of layout can be less than with resistors because no precise transmission-line environment is necessary.
- If ringing is a problem on a line during system checkout, diode termination can be used to improve the waveform.
- Where line impedances are not well defined, as in breadboarding or prototype construction of systems using AS, use of diode termination is convenient and cost effective.

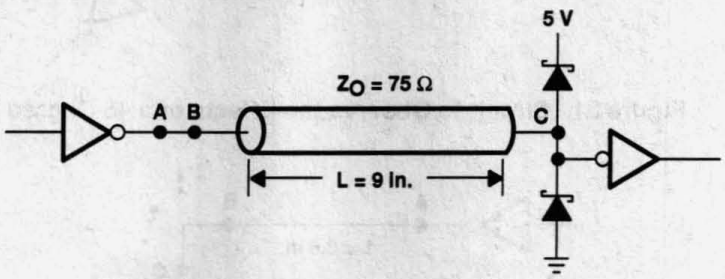


Figure 29. Active Termination

Observed waveforms of the circuit shown in Figure 29 are shown in Figure 30. Comparison of Figures 23 and 30 shows the effect of the diodes — ringing, though still present, is now within the acceptable noise margin.

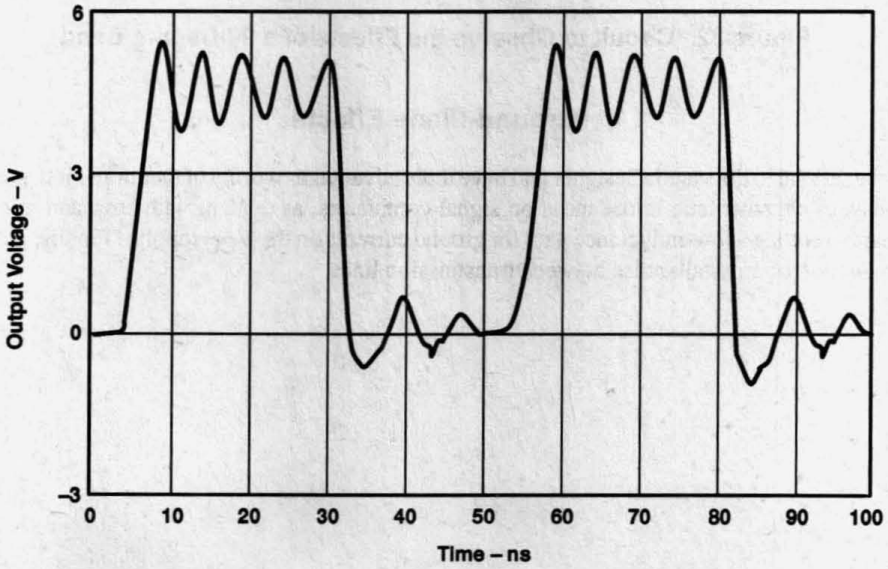


Figure 30. Active-Termination Waveform

Spatial Considerations

In very-high-speed applications, spatial considerations become very important. It has been demonstrated that the lengths of the transmission lines determine when termination is required. Therefore, these lines should be as short as possible. Any required termination — parallel-resistive, series-resistive, or diode — must be located as close to the device as possible.

In addition to the effects of line length, square corners on lines can also have an adverse effect on the system.[2] Blood[2] observed a 7.5% increase in reflection amplitude when using square rather than rounded corners. However, experiments show that the bending of runs does not seem to cause any significant signal degradation in AS systems.[1] The circuits in Figures 31 and 32 were used to establish these observations.

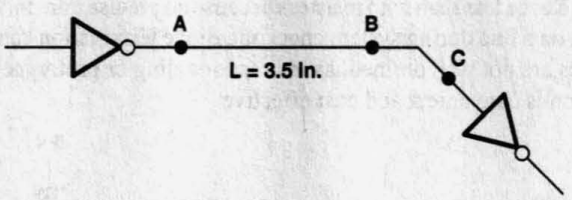


Figure 31. Circuit to Observe the Effects of a 45-Degree Bend

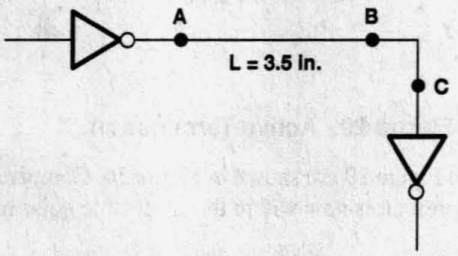
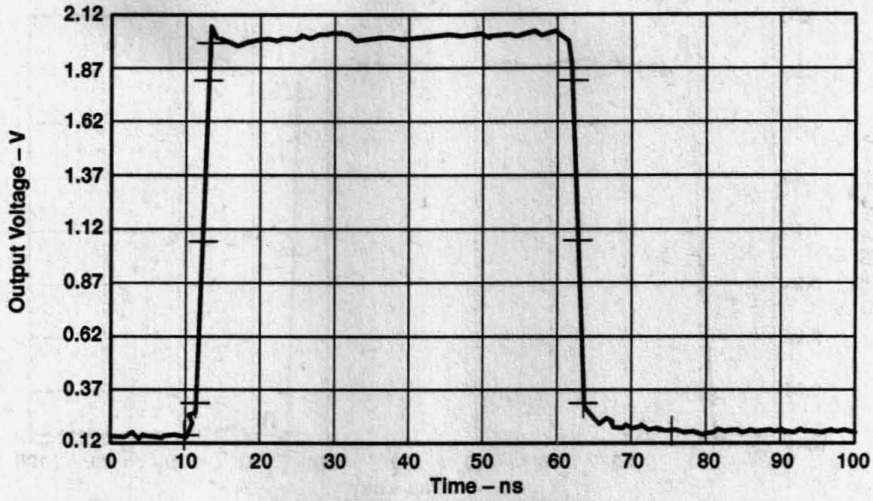


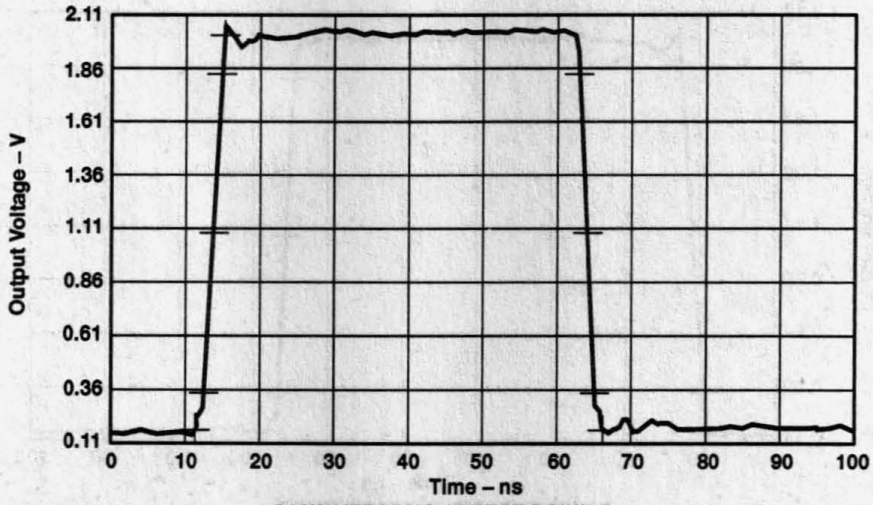
Figure 32. Circuit to Observe the Effects of a 90-Degree Bend

Ground-Plane Effects

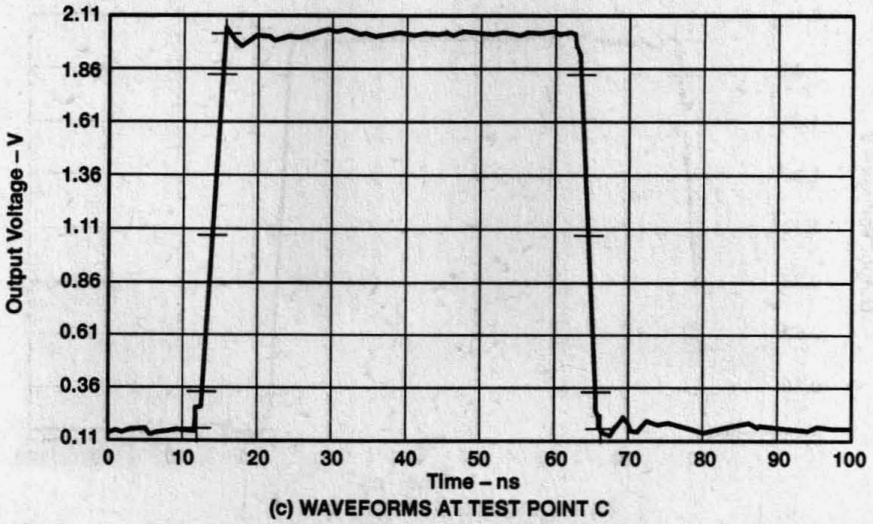
Ground planes are beneficial to the system designer and have three advantages worthy of mention. First, ground planes provide constant (well-behaved) characteristic impedances on signal conductors, as evident with strip and microstrip conductors. Second, ground planes provide a low-inductance path for ground currents on the V_{CC} supply.[2] Finally, ground planes are also beneficial in the reduction of crosstalk noise between transmission lines.



(a) WAVEFORMS AT TEST POINT A

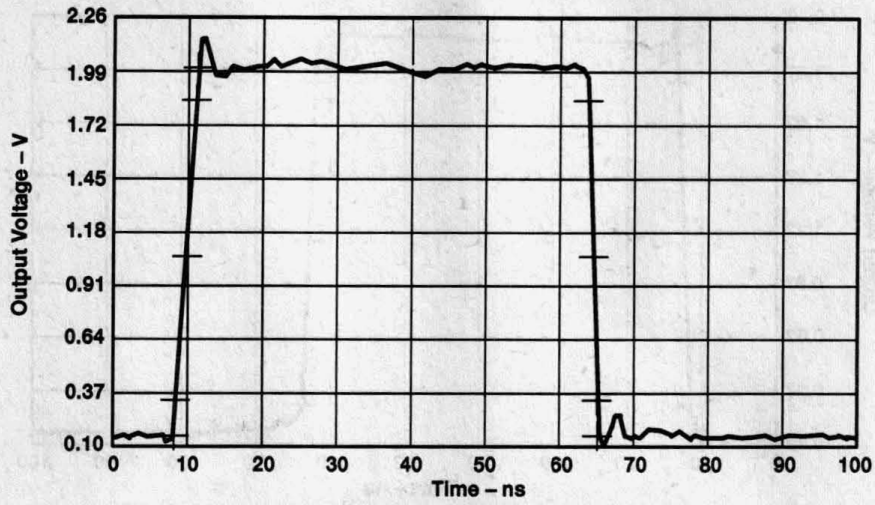


(b) WAVEFORMS AT TEST POINT B

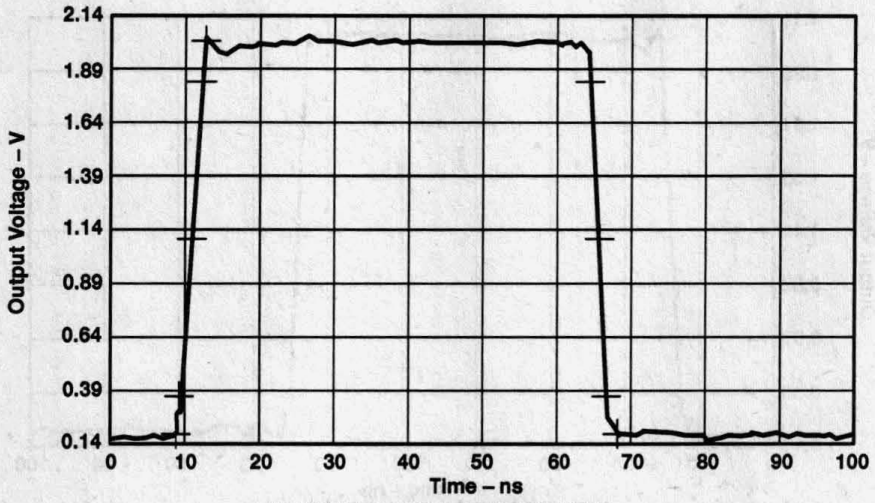


(c) WAVEFORMS AT TEST POINT C

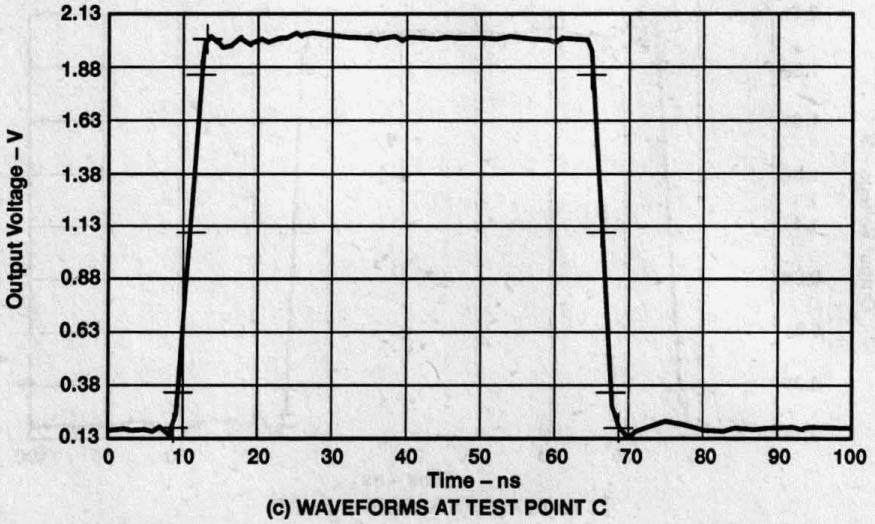
Figure 33. Observed Waveforms With a 45-Degree Bend (See Figure 31)



(a) WAVEFORMS AT TEST POINT A



(b) WAVEFORMS AT TEST POINT B



(c) WAVEFORMS AT TEST POINT C

Figure 34. Observed Waveforms With a 90-Degree Bend (See Figure 32)

Summary

In summary, the designer of high-speed systems that include AS devices must take into account the effects of the operating environment. As the system operating speed increases, the requirement for better control of the operating environment also increases. The designer of such systems must be aware not only of all the characteristics of the individual devices that are designed into the system, but also of all interactions between those devices and the source and load circuits with which they interface.

System models are very helpful in aiding the designer to understand:

- How waveforms are affected by line length.
- How (and when) to terminate signals.
- How fanout affects waveforms and can influence the choice of termination devices.

The mounting of the devices and associated effects of ground planes and conductors must also be considered.

This report has presented the basic essentials of high-speed logic design with special emphasis on the TI AS family of devices. The concepts presented are appropriate for all high-speed digital designs.

Acknowledgment

The author of this document is Mike Higgs.

References

1 Yeargan, J.R. et al., March 1985. "Printed Circuit Board Design for Advanced Schottky Family", *Proceedings of the IEEE Region 5 Conference*.

2 Blood, W.R., Jr., 1983. *MECL System Design Handbook*, 4th ed., Motorola, Inc. Chapters 3 and 7.

3 Kaup, H.R., April 1967. "Characteristics of Microstrip Transmission Lines", *IEEE Transactions on Electronic Computers*, Vol. EC-16, No. 2.

4 Bracewell, R.N., 1978. *The Fourier Transform and its Applications*, McGraw-Hill Electrical and Electronic Engineering Series.

5 Van Valkenburg, M.E., 1974. *Network Analysis*, Prentice-Hill.

Appendix A

Confirmation of AS Model

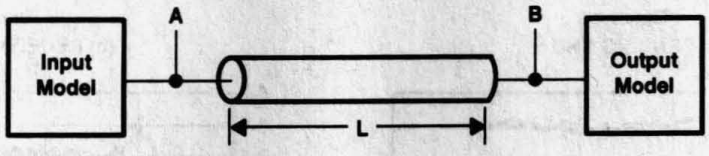


Figure 35. Observed Waveforms

Key to observed and simulated waveforms in Figure 36 for low-to-high transitions at nodes A and B shown in Figure 35:

(a) at node A for L = 4 in.
(b) at node B for L = 4 in.
(c) at node A for L = 6.5 in.
(d) at node B for L = 6.5 in.
(e) at node A for L = 9 in.
(f) at node B for L = 9 in.
(g) at node A for L = 20 in.
(h) at node B for L = 20 in.

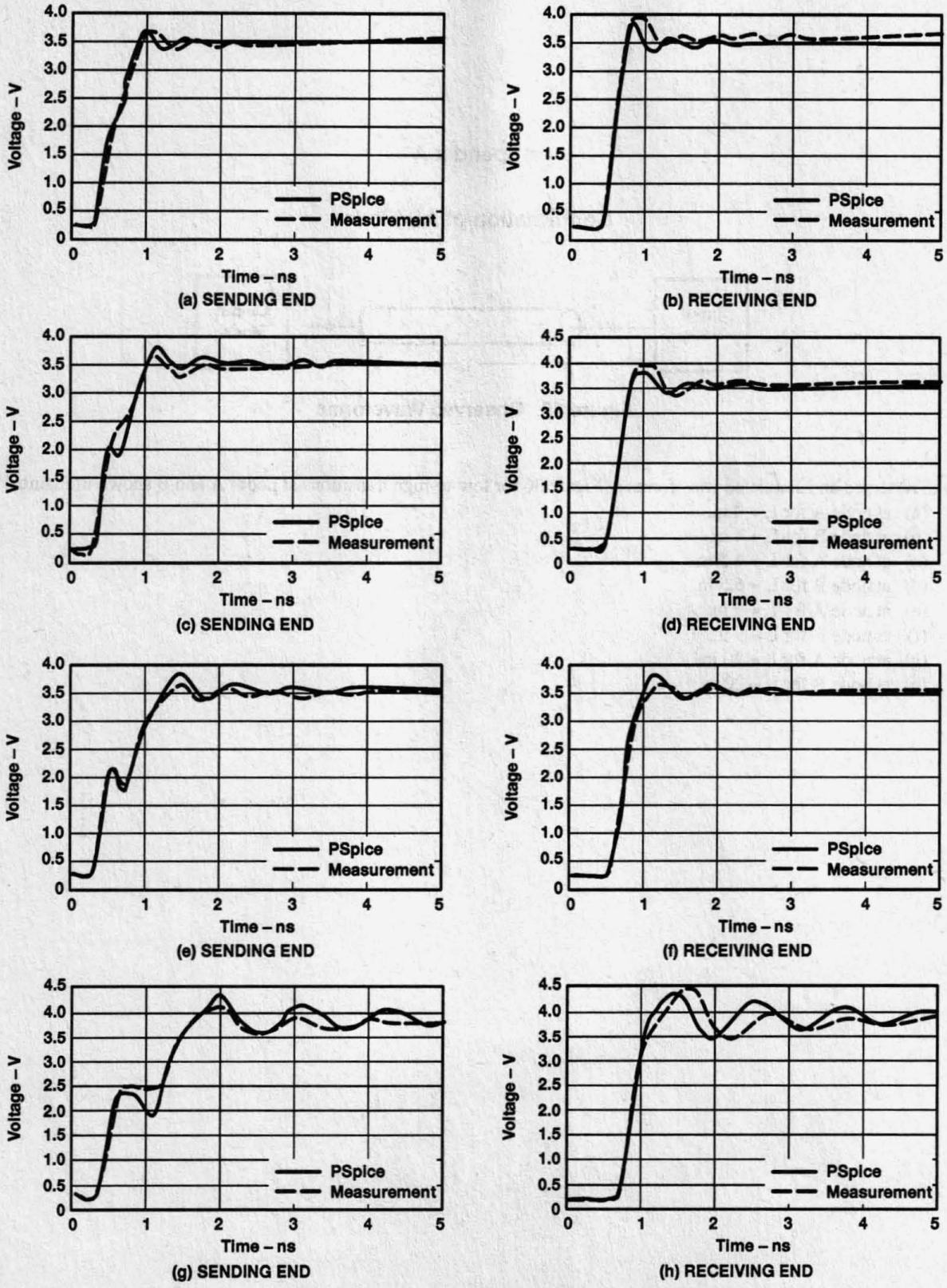


Figure 36. Comparison of Waveforms (See Figure 35)

Appendix B

Transmission Lines: A Fourier Analysis

From equation 2:

$$\frac{d^2v}{dx^2}(t,x) = L_oC_o\frac{d^2v}{dt^2}(t,x) \tag{46}$$

If f(x) transforms to F(s), $f'(x) \rightarrow i\,2\pi\,s\,F(s)$ by the derivative theorem. Therefore, equation 46 becomes:

$$(i\ 2\pi\ s)^2V = L_oC_o\frac{d^2V}{dt^2} \tag{47}$$

Where:

$i = \sqrt{-1}$

V = voltage waveform in Fourier domain

$$-4\pi^2s^2V = L_oC_o\frac{d^2V}{dt^2} \tag{48}$$

$$\frac{d^2V}{dt^2} + \frac{4\pi^2s^2V}{L_oC_o} = 0 \tag{49}$$

Equation 49 is a second-order, linear, homogeneous equation whose solution is shown in equation 50.

$$V = C_1\cos\frac{2\pi st}{\sqrt{L_oC_o}} + C_2\sin\frac{2\pi st}{\sqrt{L_oC_o}} \tag{50}$$

Let $b = vt = \frac{t}{\sqrt{L_oC_o}}$, then V becomes:

$$V = C_1\cos(b\ 2\pi\ s) + C_2\sin(b\ 2\pi\ s) \tag{51}$$

This equation is the impulse response of the transmission-line model in the Fourier domain.

[Brac 78] asserts that:

$$\cos\ \pi s \text{ transforms to } \sqcap\!\sqcup(x) \tag{52}$$

and:

$$\sin\ \pi s \text{ transforms to } \sqcup\!\sqcap(x) \tag{53}$$

Where:

$$\sqcap\!\sqcup(x) \triangleq \frac{1}{2}\left[\delta\left(x + \frac{1}{2}\right) + \delta\left(x - \frac{1}{2}\right)\right] \tag{54}$$

and:

$$\sqcup\!\sqcap(x) \triangleq \frac{1}{2}\left[\delta\left(x + \frac{1}{2}\right) - \delta\left(x - \frac{1}{2}\right)\right] \tag{55}$$

In equations 54 and 55, $\delta(x)$ is the unit impulse or Dirac function.

Equations 52 through 55 and the following theorems are used to find the impulse response in the time domain.

Addition:

$$F(s) + G(s) \text{ transforms to } f(x) + g(x) \tag{56}$$

Similarly:

$$F(bs) \text{ transforms to } \frac{1}{|b|} f\left(\frac{x}{b}\right) \tag{57}$$

Therefore:

$$V_t(x) = \frac{C_1}{|2b|} \left[\left(\frac{x}{2b}\right) + \frac{C_2 i}{|2b|} \right] \left[\left(\frac{x}{2b}\right) \right] \tag{58}$$

or:

$$V_t(x) = \frac{C_1}{|4b|}\left[\delta\left(\frac{x}{2b} + \frac{1}{2}\right) + \delta\left(\frac{x}{2b} - \frac{1}{2}\right)\right] + \frac{C_2 i}{|4b|}\left[\delta\left(\frac{x}{2b} + \frac{1}{2}\right) - \delta\left(\frac{x}{2b} - \frac{1}{2}\right)\right] \tag{59}$$

Redefining constants and assuming $x \geq 0$:

$$V_t(x) = C_1\delta\left(\frac{x}{2b} - \frac{1}{2}\right) + C_2 i\delta\left(\frac{x}{2b} - \frac{1}{2}\right) \tag{60}$$

Another approach is to take advantage of the theorem of modulation [Brac 78]:

$$F(s) \cos \omega s \text{ transforms to } \frac{1}{2}\left[f\left(x - \frac{\omega}{2\pi}\right) + f\left(x + \frac{\omega}{2\pi}\right)\right] \tag{61}$$

and:

$$F(s) \sin \omega s \text{ transforms to } \frac{1}{2}\left[f\left(x + \frac{\omega}{2\pi}\right) - f\left(x - \frac{\omega}{2\pi}\right)\right] \tag{62}$$

Using equations 61 and 62, transform V (equation 51) to the following:

$$V_t(x) = C_1\left[\delta\left(x + \frac{2b}{2}\right) + \delta\left(x - \frac{2b}{2}\right)\right] + iC_2\left[\delta\left(x + \frac{2b}{2}\right) - \delta\left(x - \frac{2b}{2}\right)\right] \tag{63}$$

Finally, using the condition that $V_O + (0) = \delta(0) = 1$, C_1 and C_2 are unity.

Hence, the impulse response to the transmission-line model is:

$$V_t(x) = \delta(x - b) + \delta(x + b) \tag{64}$$

If the definition $b = vt$ is used, equation 64 becomes:

$$V_t(x) = \delta(x - vt) + \delta(x + vt) \tag{65}$$

Finally, with $t \geq 0$, the transform can be qualified with the unit step, H(t), where:

$H(t) = 0, t < 0$
$H(t) = 1, t > 0$

Thus:

$$V_t(x) = \delta(x - vt)\ H(x - vt) \tag{66}$$

If the impulse response is called V_i, and with any input signal V_s, the voltage seen on the transmission line is V_O, the convolution of V_i and V_s is:

$$V_O = V_i * V_s \tag{67}$$

Convolution corresponds to multiplication in the Fourier domain.

$$f(x) * g(x) \rightarrow F(s)\ G(s) \tag{68}$$

$$V_o = V_i V_s = V_i \cos(b\ 2\pi\ s) + V_i \sin(b\ 2\pi\ s) \tag{69}$$

Again, by using the modulation theorem:

$$V_o = V_i(x - vt)\ H(x - vt) \tag{70}$$

SN74CBTS3384 Bus Switches Provide Fast Connection and Ensure Isolation

SCDA002A
August 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**4–87**
The Mechanics of the MOSFET Switch Leading to False Switching	**4–87**
Disruption of the Bus	**4–88**
The SN74CBTS3384 Solution	**4–89**
Conclusion	**4–90**
Acknowledgment	**4–90**

List of Illustrations

Figure	*Title*	*Page*
1	The SN74CBTS3384 With Schottky Diodes Attached at Both Ports	4–87
2	Switching Mechanics of the NMOS Switch	4–87
3	Mechanics Behind False Switching	4–88
4	The Effect of Bus Interruption on Data Flow and Signal Integrity	4–88
5	Test Conditions of the SN74CBTS3384 With Switch Disabled	4–89
6	V_O Versus V_I of the SN74CBTS3384 and a SN74CBT3384A in the Disabled State	4–89
7	Input Current Versus V_I of SN74CBTS3384 in the Disabled State	4–90

Introduction

Buses are the pathways for communication between the CPU, memory, and I/O ports in electronic systems. Today's standards demand both fast connection as well as isolation of these buses. Bus switches are usually used to address these demands because the use of a single MOSFET provides negligible propagation delay, low power dissipation and bidirectional switching; however, the use of a single transistor also can allow large negative undershoots below –1 V to cause unwanted switching and possible disruption of the bus. To prevent this problem from occurring, the SN74CBTS3384 bus switches are developed with Schottky diodes at the inputs that clamp any undershoot to approximately –300 mV (see Figure 1).

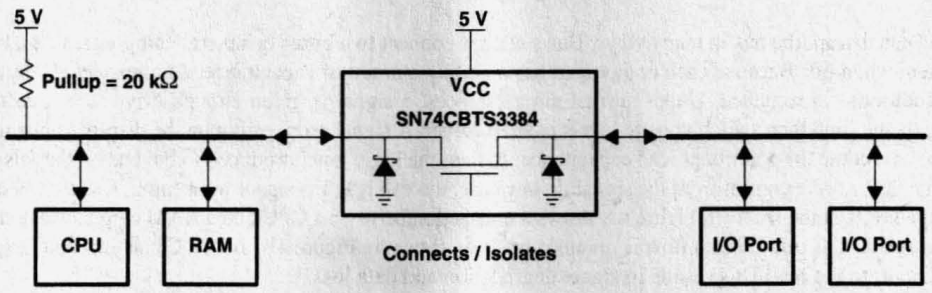
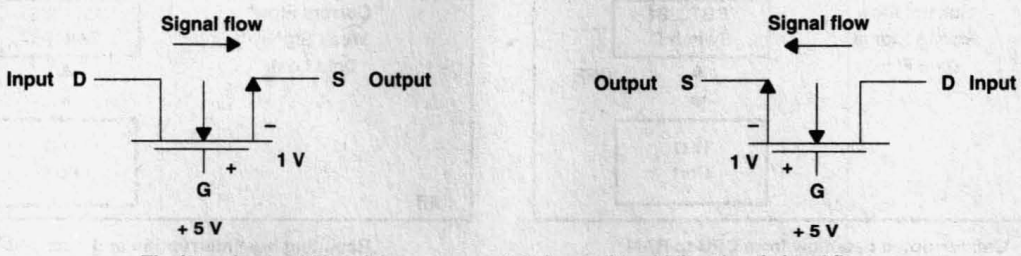


Figure 1. The SN74CBTS3384 With Schottky Diodes Attached at Both Ports

The Mechanics of the MOSFET Switch Leading to False Switching

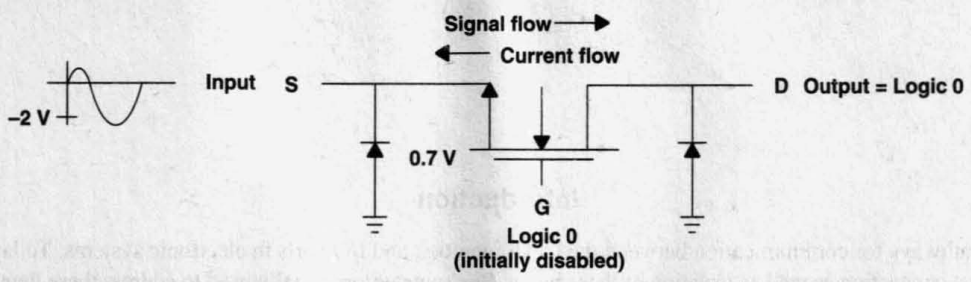
The MOSFET is used for bus switches because of its enabling and disabling speed, its low on-state resistance, and its high off-state resistance. The substrate of the N-channel MOSFET is grounded and the two n-type doped regions are interchangeable. As shown in Figure 2, when a logic high is applied to the gate, the region with a voltage of 1 V or more below the gate becomes the source and the other region the drain. At this point, the switch turns fully on and a signal flows from the input side. While this physical structure of the MOSFET provides bidirectional capability in a switch, it also allows large negative undershoots on either port to turn on a disabled switch.



The interchangeability of the source and drain provides bidirectional signal flow.

Figure 2. Switching Mechanics of the NMOS Switch

As Figure 3 shows, even though the switch is initially disabled and there is a logic low at the gate, large negative undershoots at the input cause the existing clamping diode to clamp to approximately –650 mV. Since this voltage is parallel to the gate-to-source voltage of the transistor and lasts for a few nanoseconds, the transistor starts conducting a certain amount of current. This causes a logic low to appear on the bus and disrupts any signals on it.

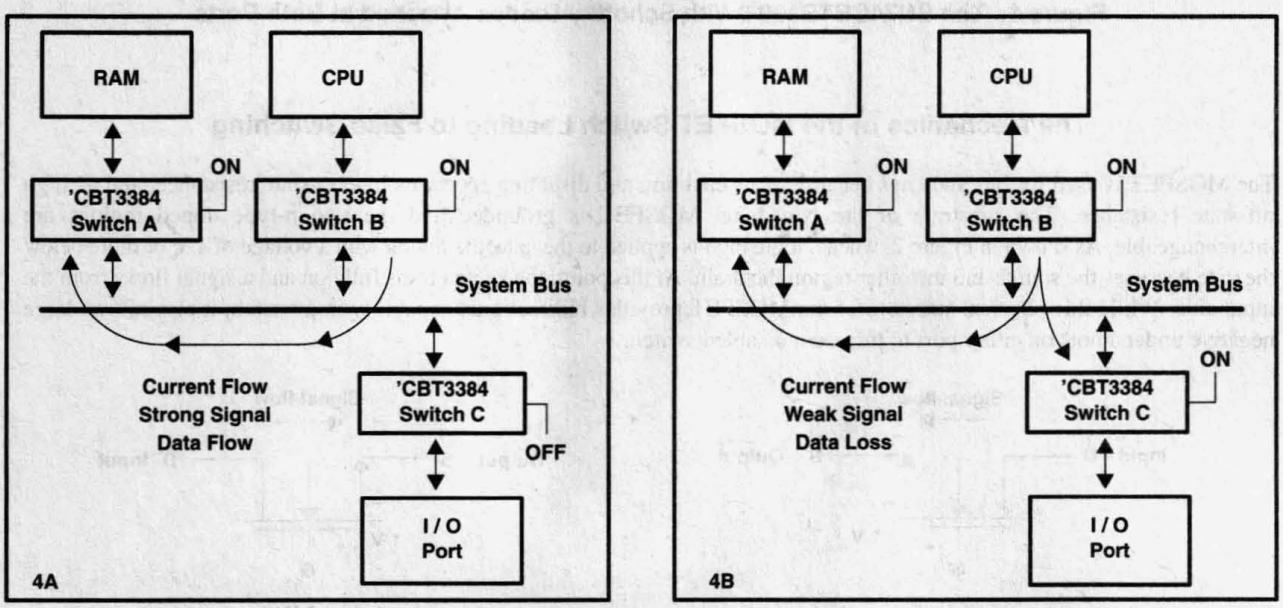


Output enable ($\overline{OE}$) is high, but large negative undershoot causes NMOS switch to turn on.

Figure 3. Mechanics Behind False Switching

Disruption of the Bus

False switching can disrupt the bus in many ways. Bus switches connect two buses or several components on a bus when on, and isolates them when off. Because each component has a certain amount of capacitance, an unexpected connection loads the bus with additional capacitance. Under normal circumstances, a signal is given enough drive to charge the expected capacitance on the bus and then switch voltage levels at the receiver. A signal propagating on the disrupted line may not have enough drive to overcome the additional load capacitance. In fact, the logic low introduced to the bus by the false connection can absorb some of the drive current from the signal. In any case, the end result is signal weakening, loss of speed, and failure to switch voltage levels at the receiver. Figure 4A shows a transaction between a CPU and a RAM chip connected by switches A and B. When switch C is off, the data flow is uninterrupted. As shown in Figure 4B, switch C can turn on unexpectedly and connect the I/O port to the bus. This results in signal degradation and data loss.



Uninterrupted data flow from CPU to RAM

Resulting bus interruption and data loss

Figure 4. The Effect of Bus Interruption on Data Flow and Signal Integrity

False switching also can cause bus contention, a case occurring when two or more transmitters on a bus are active at the same time. If the logic levels of these outputs are different, a high current flows on the line, possibly damaging the line or the components connected to it. These problems can cause serious setbacks to the high performance and reliability demands of today's systems. The use of the SN74CBTS3384 bus switch helps prevent false switching and addresses many of these problems.

The SN74CBTS3384 Solution

The SN74CBTS3384 utilizes Schottky diode at the inputs to clamp undershoot to about 300 mV below ground (see Figure 5). With the gate grounded in the disabled state, the Schottky diode prevents the gate-to-source voltage from exceeding the threshold voltage of the NMOS transistor, thus preventing weak enabling. In addition, a disabled SN74CBTS3384 switch offers a very low capacitance of about 6 pF and very low leakage current. Figure 5 shows total leakage current of only 2 μA. As a result, the disabled SN74CBTS3384 bus switch succeeds in isolating its output from any unwanted undershoots at the input. The buses are left uninterrupted and the signals on the buses are not disturbed.

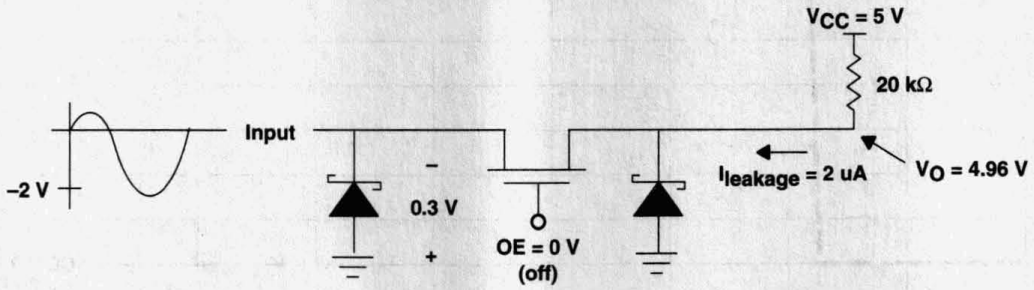


Figure 5. Test Conditions of the SN74CBTS3384 With Switch Disabled

Figure 6 shows the output of a disabled SN74CBT3384A (without Schottky diodes) as it turns on and follows the input to a negative level. This level is low enough to possibly disrupt the bus. Figure 6 also shows the SN74CBTS3384 where the Schottky diode prevents any switching throughout the wide input sweep and keeps the output at a steady level. Figure 7 shows the input current of the SN74CBTS3384 as the Schottky diode turns on, conducting about 10 mA from ground.

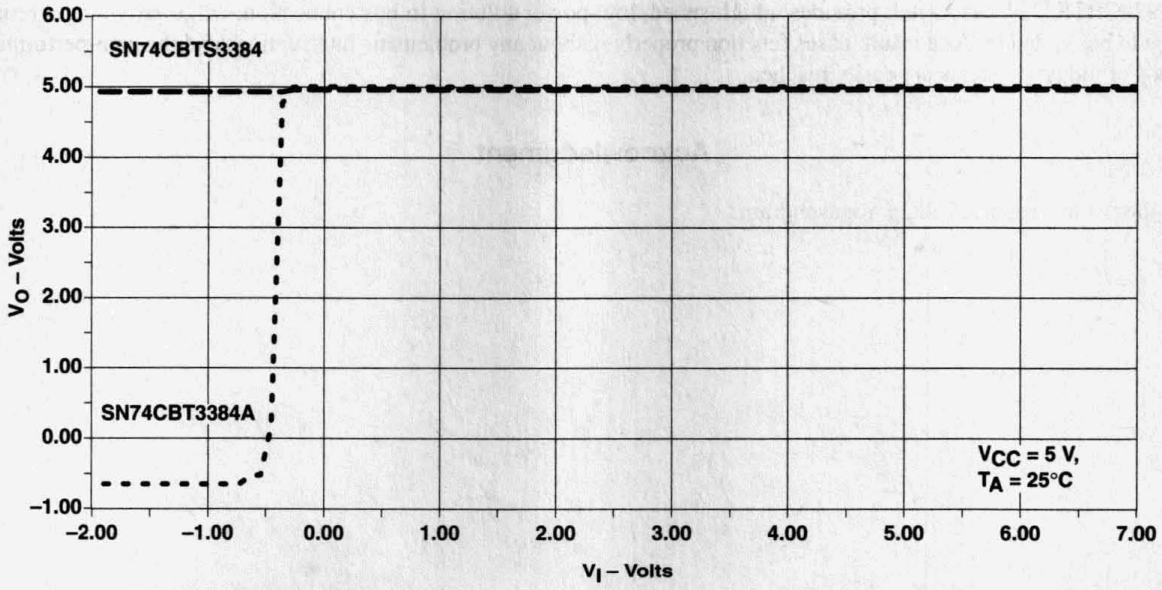


Figure 6. V_O vs V_I of the SN74CBTS3384 and a SN74CBT3384A in the Disabled State

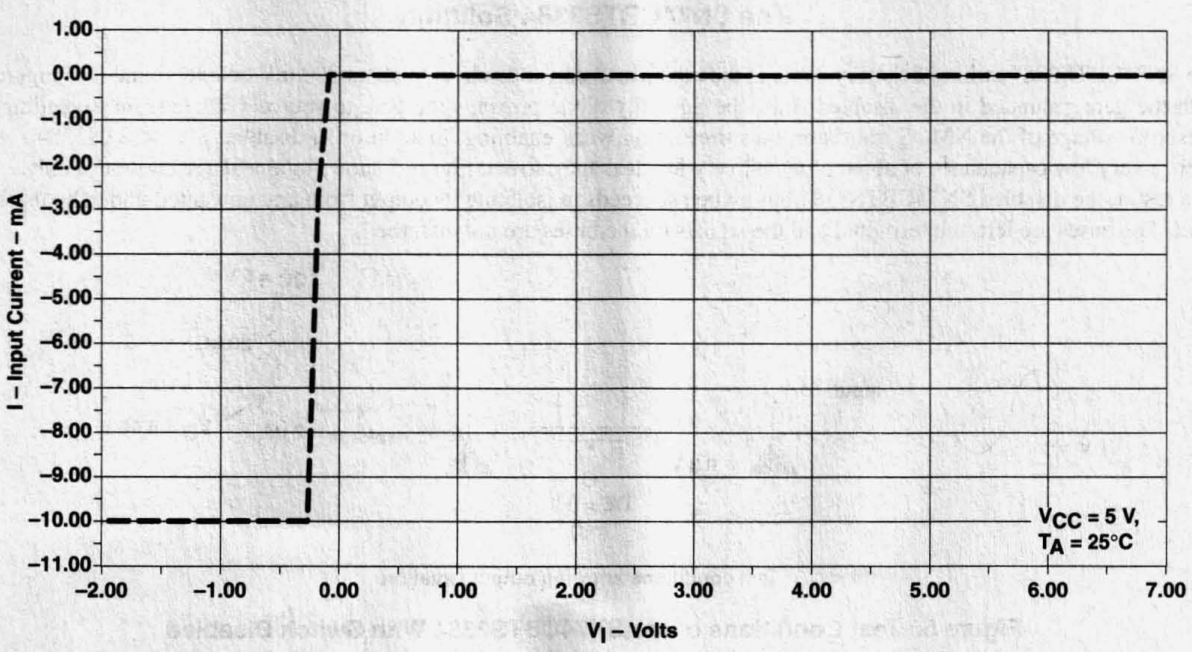


Figure 7. Input Current vs V_I of SN74CBTS3384 in the Disabled State

Conclusion

The SN74CBTS3384 bus switch provides a high-speed, low-power solution to bus connection, while providing a reliable solution to bus isolation. As a result, buses function properly without any problematic interruptions and the high-performance demands of today's systems are easily reached.

Acknowledgment

The author of this report is Nalin Yogasundram.

Texas Instruments Crossbar Switches

SCDA001A
July 1995

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1995, Texas Instruments Incorporated

Contents

Title	*Page*
What Are Texas Instruments Crossbar Switches?	**4–95**
Bus Switches Provide 5-V to 3-V Translation When 3-V Supply Line Is Not Provided	**4–97**
Bus Switches Can Be Used to Replace Drivers and Transceivers in Bus Applications	**4–97**
Bus Switches Convert TTL Logic to Hot Card-Insertion Capability	**4–97**
Conclusion	**4–99**
Acknowledgment	**4–99**

List of Illustrations

Figure	*Title*	*Page*
1	Output Voltage Versus Supply Voltage	4–95
2	Output Voltage Versus Input Voltage	4–96
3	On-State Resistance Versus Input Voltage	4–96
4	5-V TTL to 3-V TTL Translator System	4–97
5	ACL Direction of Current Flow When $V_{CC} = 0$ V	4–98
6	No ABT Current Flow When $V_{CC} = 0$ V	4–98
7	Hot Card-Insertion Application	4–98
8	Power-Up High-Impedance State With CBT	4–99

What Are Texas Instruments Crossbar Switches?

Crossbar switches are high-speed bus-connect devices. Each switch consists of an n-channel MOS transistor driven by a CMOS gate. When enabled, the n-channel transistor gate is pulled to V_{CC} and the switch is on. These devices have an on-state resistance of approximately 5 Ω and a propagation delay of 250 ps. They are capable of conducting a current of 64 mA each. The transistor clamps the output at ≈1 V less than the gate potential, regardless of the level at the input pin. This is one of the n-channel transistor characteristics (see Figures 1 and 2). Note the ≈1-V difference between the gate (V_{CC}) and the source (V_O) at any point on the graph.

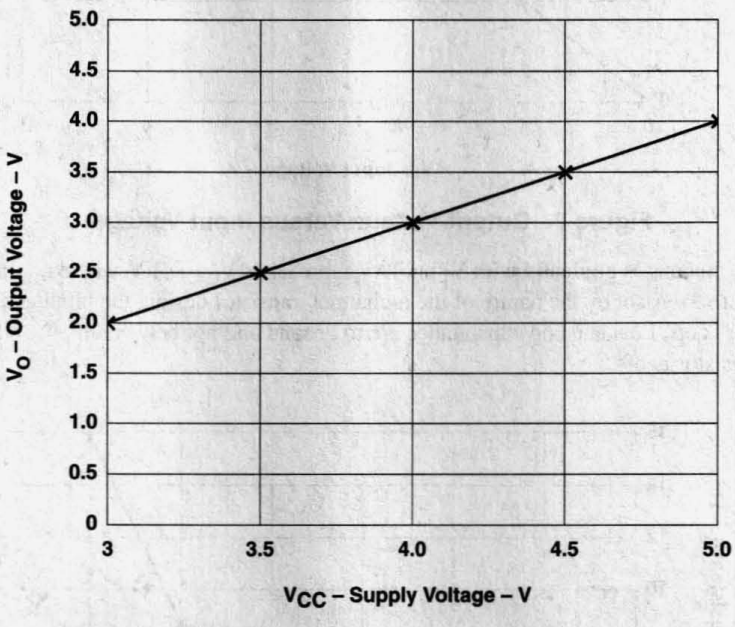


Figure 1. Output Voltage Versus Supply Voltage

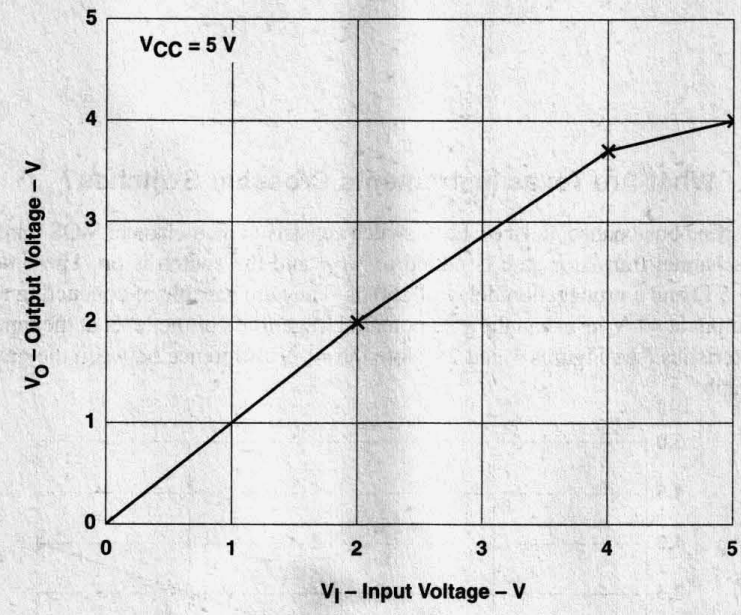


Figure 2. Output Voltage Versus Input Voltage

The on-state resistance (r_{on}) increases gradually with V_I until V_I approaches V_{CC} – 1 V, where r_{on} rapidly increases, clamping V_O at V_{CC} – 1 V (see Figure 3). Also, by the nature of the n-channel transistor design, the input and output terminals are fully isolated when the transistor is off. Leakage and capacitance are to ground and not between input and output, which minimizes feedthrough when the transistor is off.

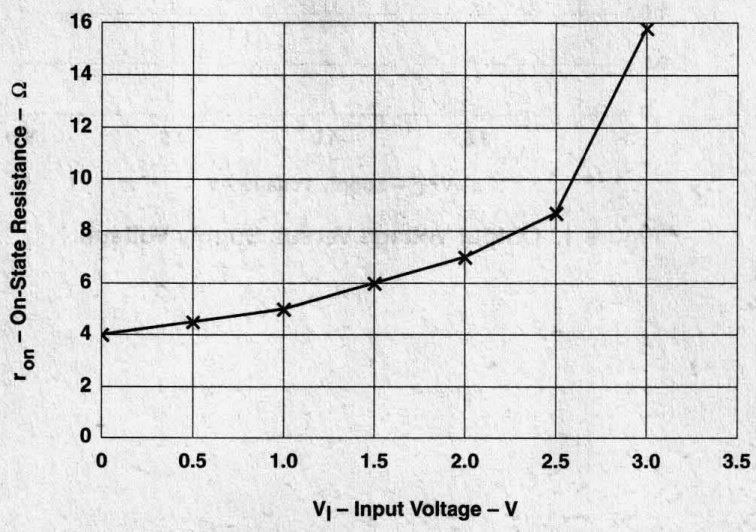


Figure 3. On-State Resistance Versus Input Voltage

Bus Switches Provide 5-V to 3-V Translation When 3-V Supply Line Is Not Provided

These devices also can provide bidirectional 5-V to 3-V translation with minimal propagation delay or direction control, using only a 5-V supply line and a diode. Figure 4 illustrates this application. A 4.3-V V_{CC} can be created by placing a diode between V_{CC} and the switch. This causes gate voltage of 4.3 V due to the diode drop of approximately 0.7 V. This drop, coupled with the gate-to-source drop of 1 V, brings V_O to a maximum 3.3-V level that can be used to drive a signal in a 3-V environment.

These devices consume very little current (I_{CC} = 3 μA). This current is not satisfactory for the diode to operate. Using a resistor from the cathode of the diode to GND allows more current from the supply voltage, causing the diode to operate and to clamp at the specified 4.3 V (see Figure 4). The recommended value of the resistor is 1 kΩ or less.

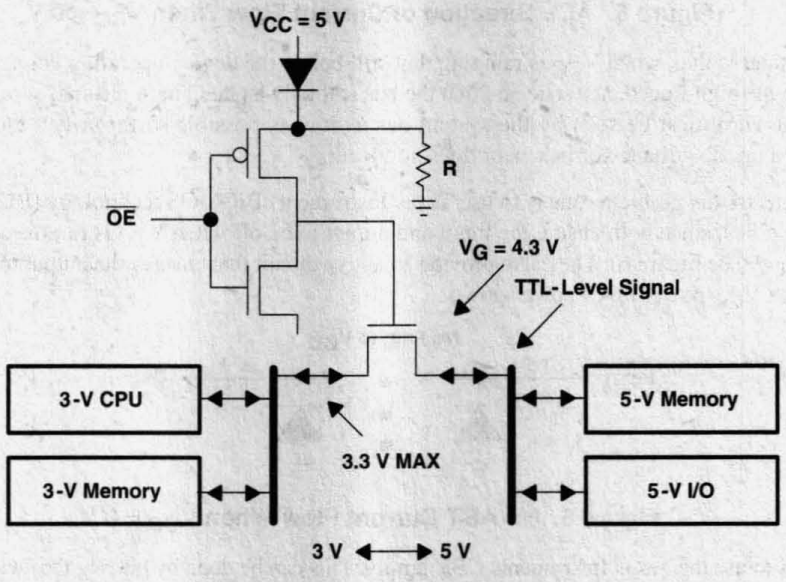


Figure 4. 5-V TTL to 3-V TTL Translator System

Bus Switches Can Be Used to Replace Drivers and Transceivers in Bus Applications

Bus switches introduce near-zero propagation delay. They can replace drivers and transceivers in systems in which signal buffering is not required. They can be used in a multiprocessor system as a fast bus connect, or they can be used as a bus-exchange switch for crossbar systems, ping-pong memory connect, or bus-byte swap. These devices also can replace relays that are used in automated test equipment (ATE) to connect or disconnect load resistors in negligible time with the same low on-state resistance and without relay-reliability problems.

Bus Switches Convert TTL Logic to Hot Card-Insertion Capability

This application is used mostly in systems that require hot card insertion or removal of cards without disturbing or loading down the bus. These systems are designed to run continuously and cannot be shut down for any reason, such as telephone switches, manufacturing controls, real-time transaction systems, and airline-reservation networks. These systems/cards use some logic families like ACL, HCMOS, etc., which do not provide isolation from the bus when power is partially removed, causing system error. Also, connectors are designed so that the ground pins are connected first, followed by the signal pins, then V_{CC} last. In this condition, the existing logic must ensure that the I/O signals do not disturb or load down the bus. This assurance cannot be achieved using CMOS logic since it contains p-channel transistors that provide an inherent diode between the I/O pins and V_{CC}. The diode is forward biased when driven above V_{CC} (see Figure 5). In a situation where V_{CC} is disconnected, these diodes are capable of pulling the system bus to approximately one diode drop above ground, leaving the bus disturbed.

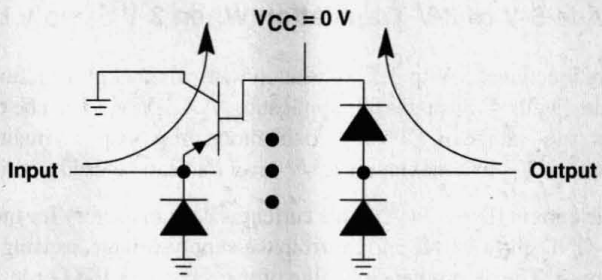


Figure 5. ACL Direction of Current Flow When V_{CC} = 0 V

Another issue to consider is that, when V_{CC} is ramping, but still below the device-operating voltage, the logic should ensure that the outputs are in the high-impedance state and that the bus is totally isolated until the card is ready for operation. Finally, the capacitance of the card must be seen by the system bus as low as possible so that when the card is inserted and the capacitance is charged up, disturbance or bus error does not occur.

There are two solutions to this problem; one is to use Texas Instruments BiCMOS technology (BCT) or advanced BiCMOS technology (ABT) families, since both ensure the input and output to be off when V_{CC} is removed due to the absence of the clamping diodes to V_{CC} (see Figure 6). They also provide an active circuit that ensures the output to be in the high-impedance state during part of the V_{CC} power up or power down.

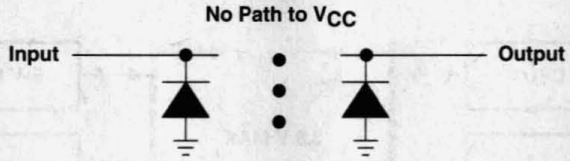


Figure 6. No ABT Current Flow When V_{CC} = 0 V

The second solution is to use the Texas Instruments CBT family. This can be done by placing the switch between the card logic and the connector to serve as an isolator when power is removed. The switch uses an n channel that prevents the current from flowing into the switch when powered down (see Figure 7). One device in particular, the SN74CBT6800, is designed specifically for hot card insertion. It has a built-in channel pullup tied to a bias voltage (BIASV) that is provided to ensure power up with the buses not connected. Other devices can be used in the same manner, however, to ensure the high-impedance state during power up or power down. The enable pins of the switch should be tied to V_{CC} through a pullup resistor. The minimum value of the resistor is determined by the current-sinking capability of the driver (see Figure 8).

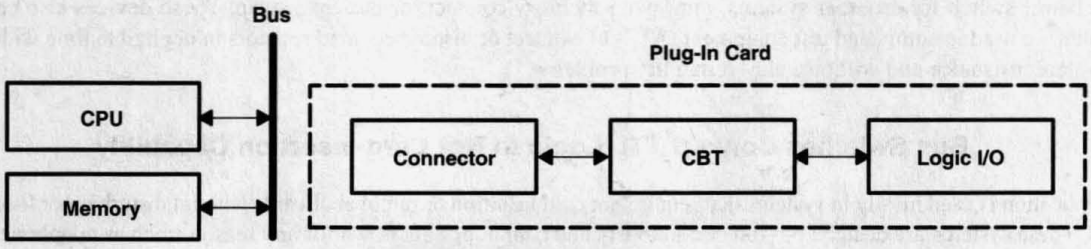
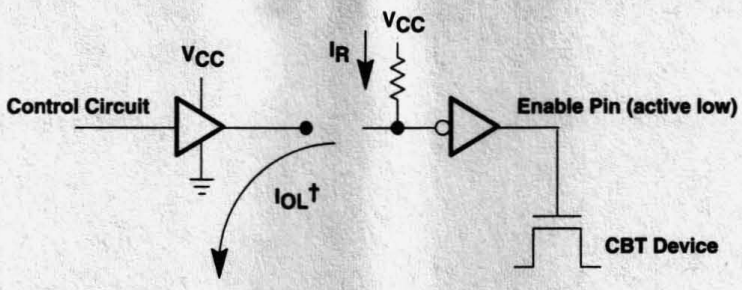


Figure 7. Hot Card-Insertion Application



† $I_{OL} > I_R$, so the control signal can override the pullup resistor.

Figure 8. Power-Up High-Impedance State With CBT

Conclusion

Texas Instruments crossbar switches can be used in several applications. Although they are simple n-channel transistors, they are capable of providing several important bus functions, such as hot card insertion, near-zero-delay communication, 5-V to 3-V translation, and memory management in multiprocessor environments.

Acknowledgment

The author of this document is Ramzi Ammar.

General Design Considerations 1
Backplane Design 2
Device-Specific Design Aspects 3
5-V Logic Design 4
3.3-V Logic Design 5
Clock-Distribution Circuits (CDC) 6
Boundary-Scan IEEE Std 1149.1 (JTAG) Logic 7
Packaging 8
Index 9

Contents

	Page
5-V to 3.3-V Translation With the SN74CBTD3384	5–3
Low-Cost, Low-Power Level Shifting in Mixed-Voltage Systems	5–11
LVC Characterization Information	5–21
Mixing It Up With 3.3 Volts	5–45
CMOS Power Consumption and C_{pd} Calculation	5–55

5-V to 3.3-V Translation With the SN74CBTD3384

SCDA003B
March 1997

Pericom
PI 74FCT3244
→ PI 74LCX541

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**5–7**
The Need for 5-V to 3.3-V Translation	**5–7**
The Mechanics of 5-V to 3.3-V Translation	**5–8**
SN74CBTD3384 Improves Upon Existing Methods for 5-V to 3.3-V Translation	**5–8**
Conclusion	**5–10**
Acknowledgment	**5–10**

List of Illustrations

Figure	*Title*	*Page*
1	The SN74CBTD3384 Bus Switch Provides 5-V to 3.3-V Translation and Bidirectional Switching	5–7
2	Comparison of 5-V and 3.3-V Interface Levels	5–7
3	NMOS Switch of SN74CBTD3384 With Maximum V_O of 3.5 V	5–8
4	V_O Versus V_I of SN74CBT3384A, SN74CBT3384A With 1N916 External Diode, and SN74CBTD3384	5–9
5	V_O Versus V_{CC} of the SN74CBTD3384	5–9

Introduction

The emergence of low-voltage technology has required existing 5-V systems to interact with 3.3-V systems. Issues concerning compatibility of the two systems in mixed-mode operation have created the need for 5-V to 3.3-V translation. Buffers and transceivers serve as effective translators. While providing additional drive, these devices also add propagation delay and require directional control. In cases where additional drive is not required, the solution that provides 5-V to 3.3-V translation, in addition to negligible propagation delay, lower power dissipation, and bidirectional bus switching, is the SN74CBTD3384 bus switch. The SN74CBTD3384 uses the inherent voltage drop of its MOSFET switch, coupled with an internal diode from V_{CC} to provide the necessary 5-V to 3.3-V translation (see Figure 1).

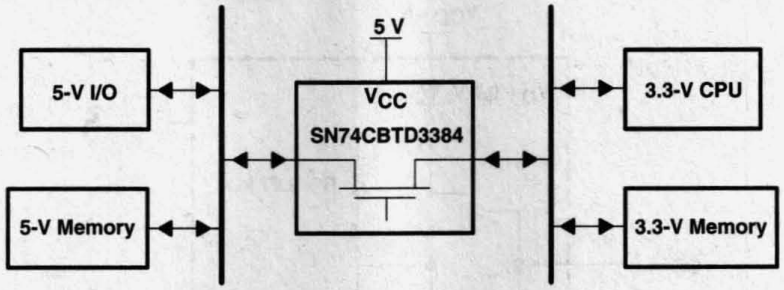
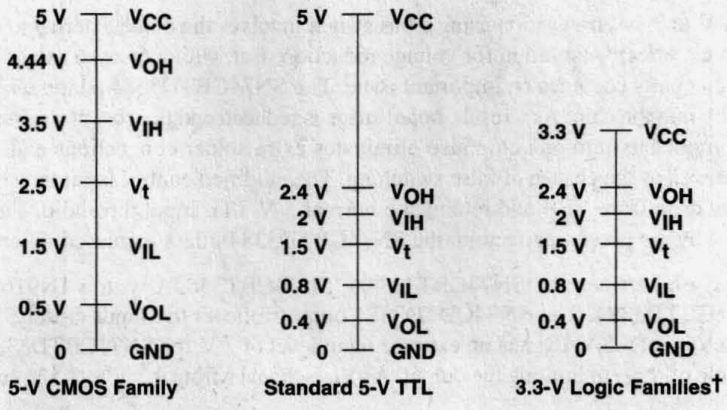


Figure 1. The SN74CBTD3384 Bus Switch Provides 5-V to 3.3-V Translation and Bidirectional Switching

The Need for 5-V to 3.3-V Translation

To realize the need for 5-V to 3.3-V translation, the I/O specifications for mixed-mode operation must be understood. Devices operating in this mode must have TTL-compatible output levels and be able to accept up to 5.5 V at the input. Figure 2 shows various interface levels for 5-V and 3.3-V families. While many 5-V and 3.3-V logic families have been designed with TTL-compatible interface levels and 5-V input tolerance, some CMOS families lack these features. Some 5-V CMOS outputs drive to 5 V; however, certain 3.3-V CMOS inputs do not tolerate 5 V. It is the incompatibility of the described input and output structures that creates the need for 5-V to 3.3-V translation.



† In accordance with JEDEC Standard 8-A for LV interface levels

Figure 2. Comparison of 5-V and 3.3-V Interface levels

The Mechanics of 5-V to 3.3-V Translation

The CBT bus switches consist of an N-channel MOSFET with its drain and source connected from input to output. The nominal value of the threshold of the MOSFET is 1 V. The MOSFET (Pass transistor) is on when the gate-to-source voltage (V_g) exceeds 1 V. A V_{CC} of 5 V connected to the gate, and a gate-to-source voltage drop of 1 V results in a maximum source voltage of about 4 V. This source voltage limitation, coupled with the transistor's typical on-state resistance of 5 Ω, gives the switch both 5-V to 4-V translation and low propagation delay. If the gate voltage is reduced lower than V_{CC}, the source will be limited to a voltage lower than 4 V. As shown in Figure 3, the SN74CBTD3384 has a diode from V_{CC} to the rest of the circuit. This diode voltage drop is 0.7 V from V_{CC}, which leads to 4.3 V at the gate of the Pass transistor. With the additional 1-V drop from gate to source, the typical output of the SN74CBTD3384 is 3.3 V. Additional diodes can be added to limit the output to even lower voltages. It is important to note that in some cases, the quiescent current (I_{CC}) flowing through the diode may not be enough to turn on the diode. A resistor (R) is added to ground to ensure enough bias current through the diode. The bidirectional nature of the switch is not sacrificed in this translation. A logic high from a 3.3-V device is relayed to the output untranslated. A 5-V receiver with TTL-compatible interface levels reads this signal as a valid high.

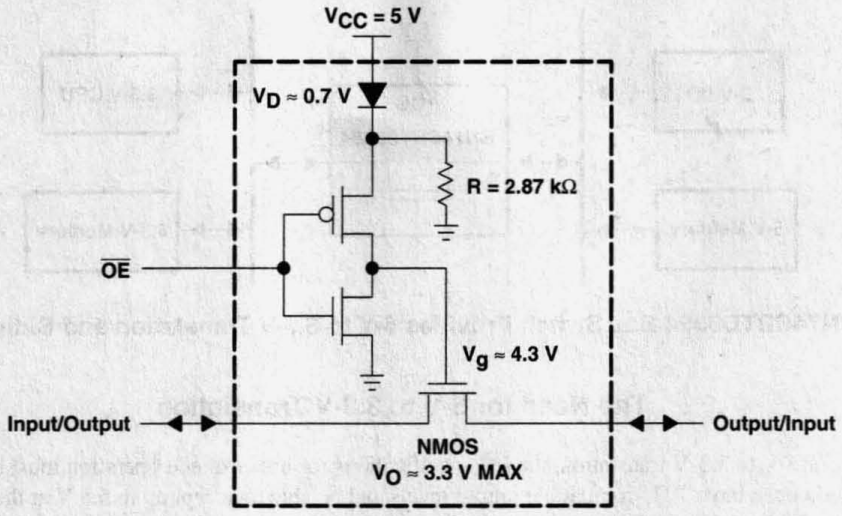


Figure 3. NMOS Switch of SN74CBTD3384 With Maximum V_O of 3.5 V

SN74CBTD3384 Improves Upon Existing Methods for 5-V to 3.3-V Translation

An existing practice for 5-V to 3.3-V translation using a bus switch involves the diode external to the chip. For most purposes, this method provides a quick, effective solution for voltage reduction. But, with increased use of low-voltage technology, the use of smaller, more reliable parts becomes an important issue. The SN74CBTD3384 addresses this issue by integrating the diode and resistor internally into the chip. As a result, board space is reduced and the cost of external components is eliminated. The integration of the components into one chip also eliminates extra solder connections and makes testing easier. Noise sensitivity is decreased, as well as the chance of false switching. The modified control input threshold of the SN74CBTD3384 compensates for the diode drop from V_{CC} and retains the normal 5-V TTL input threshold. This further reduces the noise problem. As demonstrated by the preceding factors, the SN74CBTD3384 offers increased reliability.

Figure 4 shows a comparison between the SN74CBT3384A, SN74CBT3384A with a 1N916 external diode for voltage translation, and the SN74CBTD3384. The SN74CBTD3384 output follows the input closely, but reaches a maximum of approximately 3.45 V at a V_{CC} of 5.5 V. Even at an extreme input level of 7 V, the SN74CBTD3384 limits the output to 3.5 V. Figure 5 emphasizes the role of V_{CC} in limiting the output. As V_{CC} changes from 4.5 V to 5.5 V, so does the limit of the output.

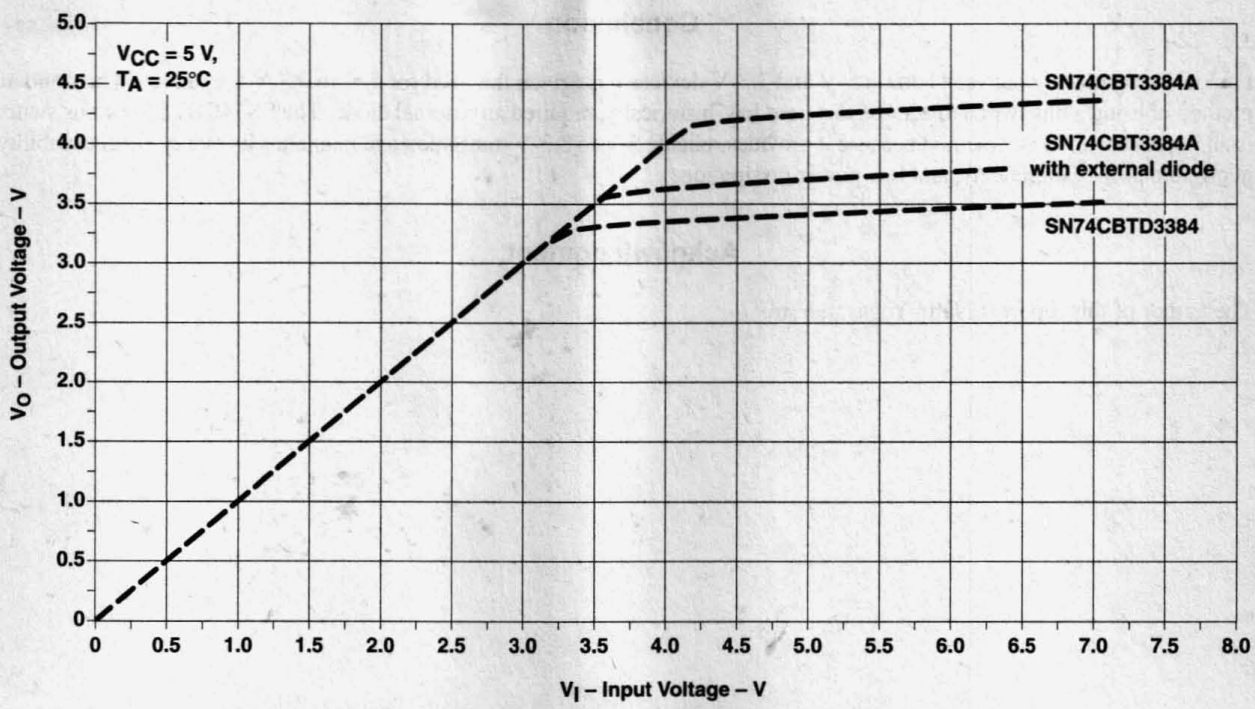


Figure 4. V_O Versus V_I of SN74CBT3384A, SN74CBT3384A With 1N916 External Diode, and SN74CBTD3384

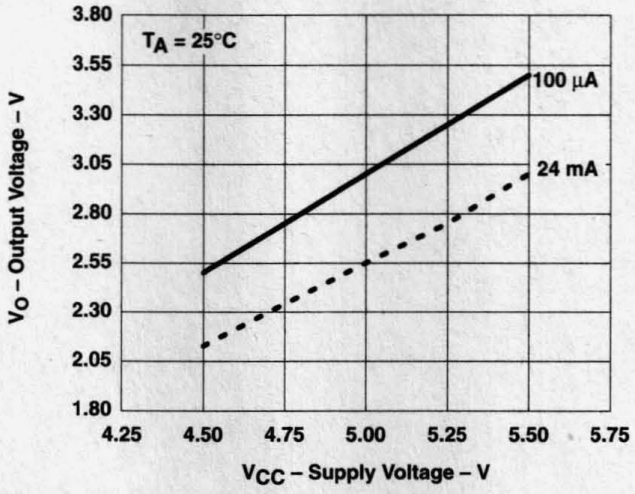


Figure 5. V_O Versus V_{CC} of the SN74CBTD3384

Conclusion

Lack of compatibility between certain 5-V and 3.3-V devices has driven the need for 5-V to 3.3-V translation. The standard method of using a bus switch to address this need has, historically, required an external diode. The SN74CBTD3384 bus switch is an improvement to this method because it provides reliable 5-V to 3.3-V translation and maintains its bidirectional capability, negligible propagation delay, and low power dissipation.

Acknowledgment

The author of this report is Nalin Yogasundram.

Low-Cost, Low-Power Level Shifting in Mixed-Voltage Systems

SCBA002
June 1994

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Please be aware that TI products are not intended for use in life-support appliances, devices, or systems. Use of TI product in such applications requires the written approval of the appropriate TI officer. Certain applications using semiconductor devices may involve potential risks of personal injury, property damage, or loss of life. In order to minimize these risks, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards. Inclusion of TI products in such applications is understood to be fully at the risk of the customer using TI devices or systems.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1994, Texas Instruments Incorporated

Printed in the U.S.A.

Contents

Title	*Page*
Introduction	**5–15**
Split-Rail Level Shifters	**5–15**
5-V Tolerant, Pure 3.3-V V_{CC} Level Shifters	**5–15**
The Misconception About ΔI_{CC}	**5–15**
More Savings Are Possible	**5–18**
Conclusion	**5–19**
Acknowledgment	**5–19**

List of Illustrations

Figure	*Title*	*Page*
1	Basic Logic Data Transceiver	5–16
2	Basic CMOS Input Structure and Typical ΔI_{CC} Current	5–16
3	ΔI_{CC} – 16-Bit Device	5–17
4	V_{OH} of FCT164245 and 'LVT16245A	5–17
5	Total System Power Dissipation Impact	5–18
6	LVT Bus-Hold Cell	5–19

Introduction

The increasing demand for lower system power consumption has brought many new design challenges. Among them is the problem of safely and efficiently interfacing the various switching levels in today's mixed 3.3-V and 5-V systems while maintaining the lowest possible total system power consumption. Two competing methods of accomplishing this mixed-mode signal translation have emerged:

- Split-rail or dual 3.3-V and 5-V V_{CC} devices
- Completely 5-V tolerant, pure 3.3-V V_{CC} components

This application report deals with the pros and cons of using both device types and offers additional suggestions for even greater system power savings.

Split-Rail Level Shifters

Split-rail level shifters are a class of transceiver devices that have both a 5-V and 3.3-V V_{CC} rail. Products in this class can be used effectively as level shifters and datapath voltage translators, but the following precautions are usually recommended:

- Dual-V_{CC} rail devices typically have strict power sequencing requirements to prevent leakage or even damage to the devices in the event that one V_{CC} rail ramps faster than the other. These stringent requirements are often difficult to meet from a system-timing standpoint and offer little flexibility for partial system power down or other advanced power-saving design techniques.
- Simply because the device has a 5-V V_{CC} pin does not necessarily ensure that the part will actually switch all the way to the 5-V rail. Switching to 5 V is one way to reduce the power consumption in 5-V memories or other pure 5-V CMOS circuits that are driven by a level-shifter device (this application report will demonstrate others as well).

The data sheet for the product in question reveals whether the part drives all the way to the 5-V rail. If the output high-voltage (V_{OH}) minimum is around 4.44 V, it does drive to the rail. Five-volt level shifters with TTL-compatible outputs typically drive only to around 3.6 V.

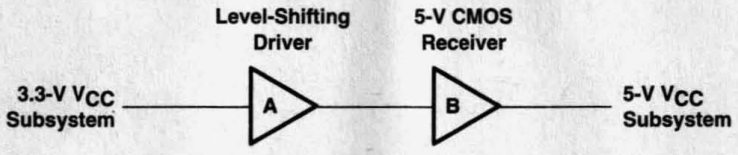
5-V Tolerant, Pure 3.3-V V_{CC} Level Shifters

A second class of products created to meet these design challenges offers the same voltage translation and level-shifting capabilities as the split-rail devices previously mentioned. From a single V_{CC} source, they avoid the power-sequencing problems of the split rails and also are offered in a number of functions, bit widths, and storage options. The one potential drawback of the single-V_{CC} products is that the outputs do not pull all the way to the 5-V V_{CC} rail. But, is this really a drawback?

The Misconception About ΔI_{CC}

The component selection of a level shifter impacts two major aspects of total system-power dissipation:

- The impact that the V_{OH} level of the driving part (A, in Figure 1) has on the power dissipation of the receiving device (B, in Figure 1), commonly known as ΔI_{CC}
- The power of the device itself



Note: Unidirectional mode illustrated for simplicity.

Figure 1. Basic Logic Data Transceiver

ΔI_{CC} is the added power dissipation induced into a TTL-compatible 5-V CMOS device (B, in Figure 1) due to the V_{OH} level of the driving device (A, in Figure 1). It would be correct to expect that a TTL-compatible 5-V CMOS product have higher power dissipation if it was driven by a device with a V_{OH} of 3.6 V than if that same device was driven by a 5-V V_{OH} driver.

Figure 2 shows a typical CMOS input stage and the ΔI_{CC} current associated with switching the device through the input voltage range from 0 to V_{CC}.

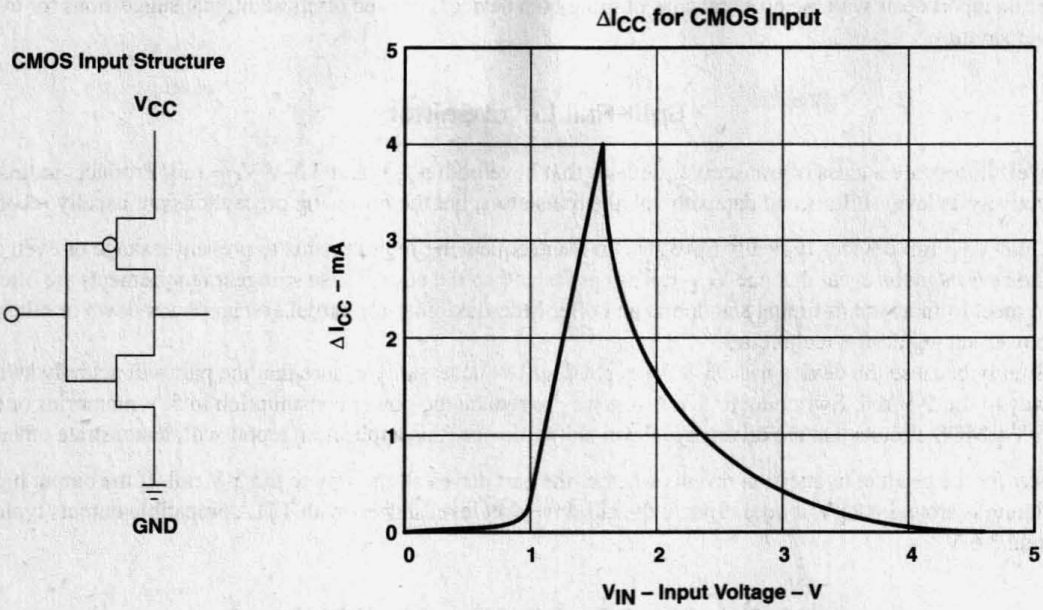


Figure 2. Basic CMOS Input Structure and Typical ΔI_{CC} Current

As expected, the ΔI_{CC} current approaches zero at the V_{CC} and ground rails, and peaks in the TTL-threshold region of 1.5 V.

Figure 3 is a graph of the ΔI_{CC} (i.e., additional I_{CC}) that is induced into a 16-bit device (all outputs switching) as a function of V_{OH} and frequency.

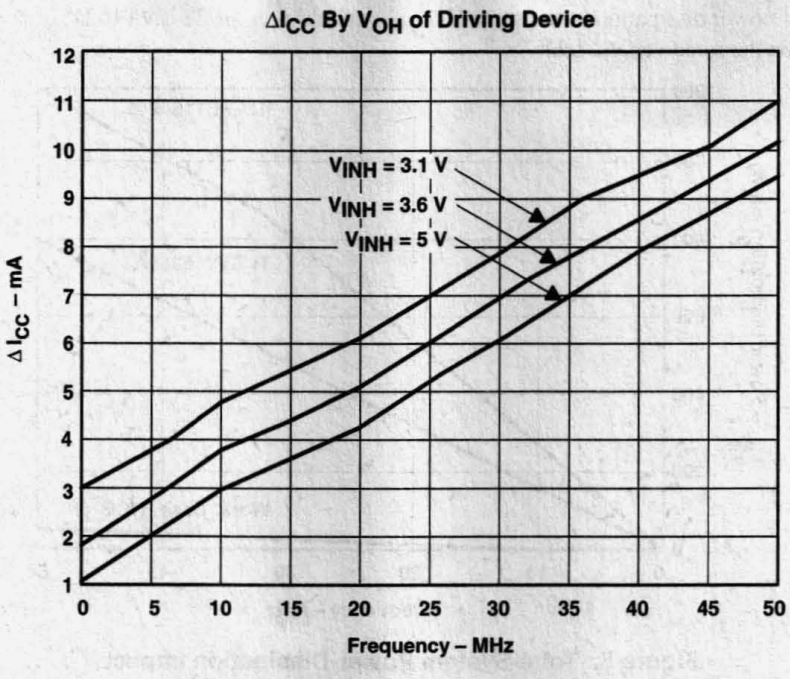


Figure 3. ΔI_{CC} – 16-Bit Device

As shown in Figure 3, ΔI_{CC} is, in fact, 2 to 3 mA higher for the case where V_{OH} is only 3.1 V, than for the same device driven to the 5-V rail by a pure 5-V CMOS device. From this, one might conclude that the best possible solution would be to always select a part that switches all the way to the 5-V rail, but this conclusion fails to consider the impact of system power on the driving device.

Figure 4 shows the V_{OH} of two devices: the FCT164245 split-rail device from Integrated Device Technologies (IDT) and the 'LVT16245A from Texas Instruments.

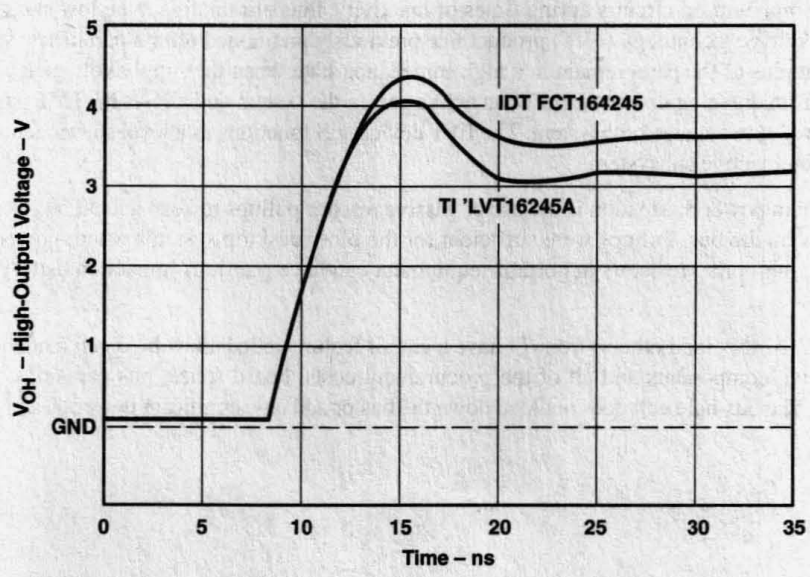


Figure 4. V_{OH} of FCT164245 and 'LVT16245A

From Figure 4, it can be correctly concluded that the induced ΔI_{CC} current in a part driven by the LVT part would be higher than the FCT device. The problem with this conclusion is that ΔI_{CC} is only one of the two components of total system power dissipation that selection of a level-shifter device has from a system standpoint.

Figure 5 shows the total power dissipation of the same IDT split-rail device, the TI 'LVT16245A, and the worst-case ΔI_{CC} (V_{OH} = 3.1 V) plotted on the same vertical scale.

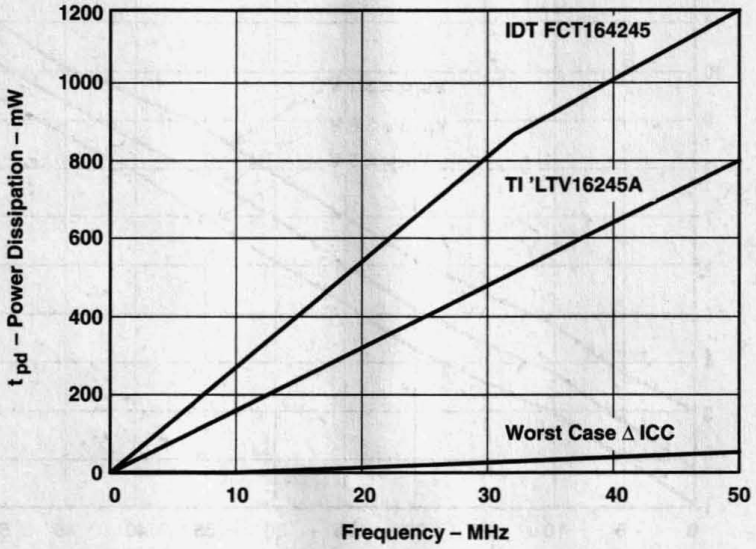


Figure 5. Total-System Power-Dissipation Impact

From Figure 5, it can be seen that, even if a split-rail device pulls all the way to the 5-V rail (which the IDT part does not), the power savings in ΔI_{CC} is more than offset by the huge switching currents that the split rail draws from the 5-V rail. The negative implications on heating, reliability, and battery life are obvious.

More Savings Are Possible

Some systems use a means of power savings known as partial power down. In partial power-down mode, a system basically shuts off the V_{CC} to some unused circuits during times of inactivity, thus eliminating even low standby currents. All of the members of TI's low-voltage technology (LVT) product line previously mentioned offer a parametric specification I_{off}, which ensures that the output pins of the parts remain in a high-impedance state when the supply voltage is at 0 V. This prevents an inactive LVT device from dragging down the bus of an active part in the system and allows the LVT part to become a partition for the partially powered-down unused subsystem. The LVT device still functions as a level shifter and voltage translator when power is restored to the inactive subsystem.

Another aspect of system power dissipation is the use of passive resistor pullups to keep a local bus from floating and causing damage to the devices on the bus. Pullups were sufficient for the older desktop systems where power consumption was not as much of a concern, but pullup resistors in portable equipment can have a serious impact on battery life, and as such must be addressed.

Products like the 'LVT16245A (and others) from TI have a circuit feature called a bus-hold cell (shown in Figure 6). This cell eliminates these passive components and all of the procurement costs, board space, bus parasitics, and power dissipation associated with them. The bus-hold cell does not load down the bus or add any significant power dissipation to the LVT device.

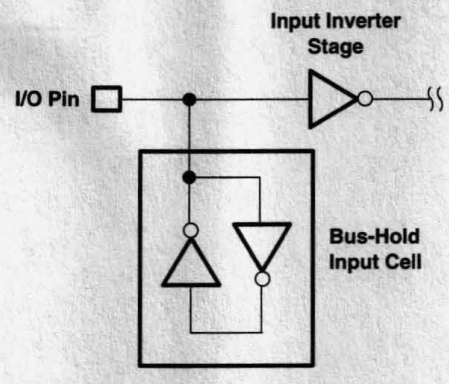


Figure 6. LVT Bus-Hold Cell

Conclusion

Mixed 3.3-V and 5-V systems can be optimized for low power and low cost by the judicious selection of the appropriate voltage-level shifter component. Split-rail level shifters can affect this voltage translation, but selection of this device is burdened with serious design tradeoffs in power sequencing, partial system power down, and system power dissipation. Further savings in both power and component cost can be realized if the component selected has a bus-hold cell or other means of eliminating passive system components.

Acknowledgment

The author of this document is Mark McClear.

LVC Characterization Information

SCBA011
December 1996

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**5–25**
The Case for Low Voltage	5–25
Considerations for Interfacing to 5-V Logic	**5–26**
Case 1	5–28
Case 2	5–28
Case 3	5–28
Case 4	5–28
ac Performance	**5–29**
Power Considerations	**5–33**
Input Characteristics	**5–35**
LVC Input Circuitry	5–35
Input Current Loading	5–37
Supply Current Change (ΔI_{CC})	5–38
Proper Termination of Unused Inputs and Bus Hold	5–38
Output Characteristics	**5–39**
LVC Output Circuitry	5–40
Output Drive	5–40
Partial Power Down	5–40
Proper Termination of Outputs	5–40
Technique 1	5–41
Technique 2	5–41
Technique 3	5–41
Technique 4	5–42
Technique 5	5–42
Signal Integrity	**5–43**
Acknowledgment	**5–43**

EPIC is a trademark of Texas Instruments Incorporated.

List of Illustrations

Figure	*Title*	*Page*
1	Comparison of 5-V CMOS, 5-V TTL, and 3.3-V TTL Switching Standards	5–26
2	Summary of Four Cases When Interfacing 3.3-V Devices With 5-V Devices	5–27
3	Propagation Delay Time Versus Operating Free-Air Temperature	5–29
4	Propagation Delay Time Versus Number of Outputs Switching	5–31
5	Propagation Delay Time Versus Load Capacitance	5–32
6	I_{CC} Versus Frequency	5–34
7	Supply Current Versus Input Voltage	5–35
8	Simplified Input Stage of an LVC Circuit	5–35
9	Output Voltage Versus Input Voltage	5–36
10	Input Current Versus Input Voltage	5–36
11	Input Leakage Current Versus Input Voltage	5–37
12	Bus Hold	5–38
13	$I_{I(hold)}$ Versus V_I	5–39
14	Simplified Output Stage of an LVC Circuit	5–40
15	Typical LVC Output Characteristics	5–40
16	Termination Techniques	5–41
17	Simultaneous Switching Noise Waveform	5–43

List of Tables

Table	*Title*	*Page*
1	Input Current Specifications	5–37
2	ΔI_{CC} Current Specifications	5–38
3	Bus-Hold Specifications [$I_{I(hold)}$]	5–39
4	LVC Output Specifications	5–39
5	Termination Techniques Summary	5–42

Introduction

The Case for Low Voltage

LVL, or low-voltage logic, in the context of this application report, refers to devices designed specifically to operate from a 3.3-V power supply. Initially, an alternative method of achieving low-voltage operation was to use a device designed for 5-V operation, but power it with a 3.3-V supply. Although this resulted in 3.3-V characteristics, this method resulted in significantly slower propagation time. Subsequently, parts were designed to operate using a 3.3-V power supply.

A primary benefit of using a 3.3-V power supply as opposed to the traditional 5-V power supply is the reduced power consumption. Because power consumption is a function of the load capacitance, the frequency of operation, and the supply voltage, a reduction in any one of these is beneficial. Supply voltage has a square relationship in the reduction of power consumed, whereas load capacitance and frequency of operation have a linear effect. As a result, a small decrease in the supply voltage yields significant reduction in the power consumption. Equation 1 provides the dynamic component of the power calculation. (The calculation for computing the total power consumed is provided in *Power Considerations*.)

$$P_D(\text{dynamic}) = [(C_{pd} + C_L) \times V_{CC}^{\ 2} \times f]\ N_{SW} \quad (1)$$

Where:

C_{pd} = Power dissipation capacitance (F)
C_L = External load capacitance (F)
V_{CC} = Supply voltage (V)
f = Operating frequency (Hz)
N_{SW} = Total number of outputs switching

A reduction of power consumption provides several other benefits. Less heat is generated, which reduces problems associated with high temperature. This may provide the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower temperature stress gradients on the device, and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. An additional benefit of the reduced power consumption is the extended life of the battery when a system is not powered by a regulated power supply.

Although a complete migration may not be feasible for a particular application, beginning to integrate 3.3-V components in a system still has benefits. If system parts are designed using 3.3-V parts, then when the remaining parts become available, converting the system completely to 3.3-V parts is a much smaller task. For example, having the internal parts of a personal computer powered from a 3.3-V power supply while having the memory powered from a 5-V power supply is a fairly common current configuration. Although LVL devices are not used throughout the entire design, this system is easily adapted to a complete 3.3-V system when 3.3-V memory becomes cost effective.

Considerations for Interfacing to 5-V Logic

Interfacing 3.3-V devices to 5-V devices requires consideration of the logic switching levels of the driver and the receiver. Figure 1 illustrates the various switching standards for 5-V CMOS, 5-V TTL, and 3.3-V TTL. The switching levels for the 5-V TTL and the 3.3-V TTL are identical, whereas the 5-V CMOS switching levels are different. The impact of this must be considered when interfacing 3.3-V systems with 5-V systems.

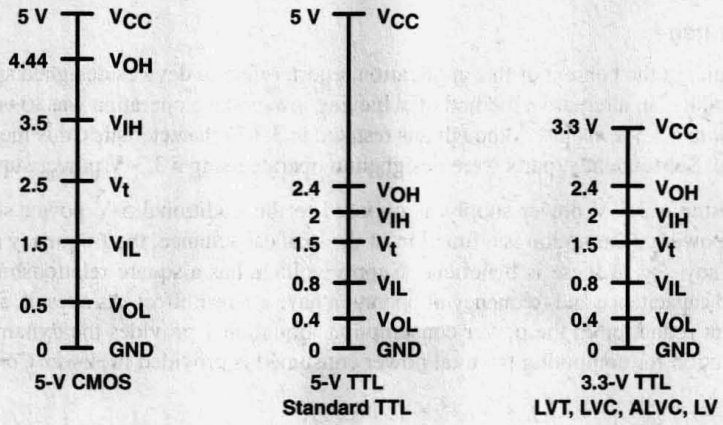
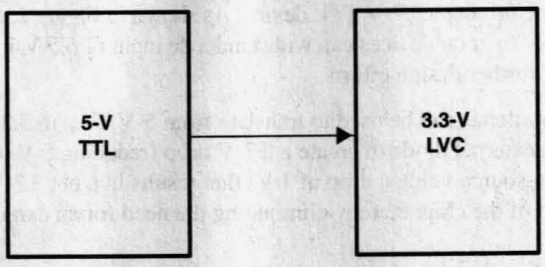


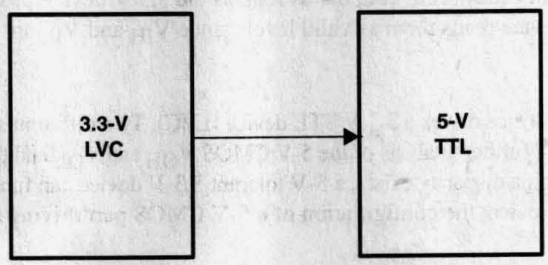
Figure 1. Comparison of 5-V CMOS, 5-V TTL, and 3.3-V TTL Switching Standards

Depending on the specific parts used in a system, four different cases can result. These cases are illustrated in Figure 2.

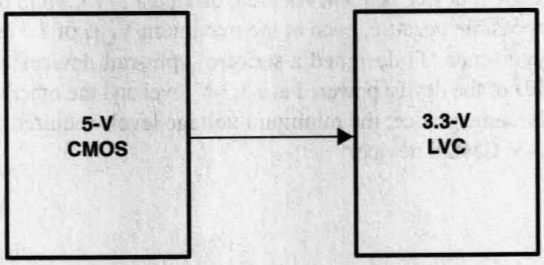
Case 1: 5-V TTL Device Driving 3.3-V TTL Device (LVC)



Case 2: 3.3-V TTL Device (LVC) Driving 5-V TTL Device



Case 3: 5-V CMOS Device Driving 3.3-V TTL Device (LVC)



Case 4: 3.3-V TTL Device (LVC) Driving 5-V CMOS Device

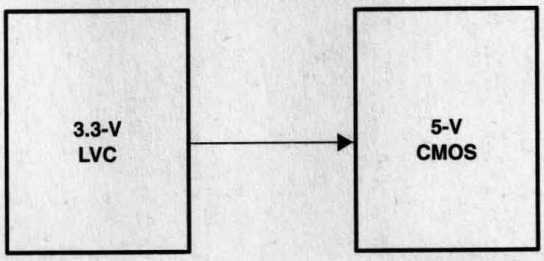


Figure 2. Summary of Four Cases When Interfacing 3.3-V Devices With 5-V Devices

Case 1

Case 1 addresses a 5-V TTL device driving a 3.3-V TTL device. As shown in Figure 1, the switching levels for 5-V TTL and 3.3-V LVC are the same. Since 5-V tolerant devices can withstand a dc input of 6.5 V, interfacing these two devices does not require additional components or further design efforts.

TI's crossbar technology (CBT) switches can be used to translate from 5-V TTL to 3.3-V devices that are not 5-V tolerant. This is accomplished by using an external diode to create a 0.7-V drop (reducing 5 V to 4.3 V) with the CBT (of which the field effect transistor has a gate-to-source voltage drop of 1 V) that results in a net 3.3-V level. TI produces a CBTD device that incorporates the diode as part of the chip, thereby eliminating the need for an external diode.

Case 2

Case 2 occurs when a 3.3-V TTL device (LVC) drives a 5-V TTL device. The switching levels are the same and it is possible to interface in this configuration without additional circuitry or devices. Driving a 5-V device from a 3.3-V device without additional complications or circuitry may seem odd, but as long as the 3.3-V device produces V_{OH} and V_{OL} levels of 2.4 V and 0.4 V, the input of the 5-V device reads them as valid levels since V_{IH} and V_{IL} are 2 V and 0.8 V.

Case 3

Case 3 occurs when a 5-V CMOS device drives a 3.3-V TTL device (LVC). Two different switching standards that do not match (see Figure 1) are interfacing. Upon further analysis of the 5-V CMOS V_{OH} and V_{OL} and the 3.3-V LVC V_{IH} and V_{IL} switching levels, Figure 1 shows that although a disparity exists, a 5-V tolerant 3.3-V device can function properly with 5-V CMOS input levels. With a 5-V tolerant LVC device, the configuration of a 5-V CMOS part driving a 3.3-V LVC part is possible.

Case 4

Case 4 occurs when a 3.3-V TTL device (LVC) drives a 5-V CMOS device. Two different switching standards are interfacing. As shown in Figure 1, the specified V_{OH} for a 3.3-V LVC is 2.4 V (higher output levels up to 3.3 V are possible), whereas the minimum required V_{IH} for a 5-V CMOS device is 3.5 V. As such, driving a 5-V CMOS device with a 3.3-V LVC (or any other standard 3.3-V logic) device is impossible because, even at the maximum V_{OH} of 3.3 V, the minimum V_{IH} of 3.5 V is never attained. To accommodate this occurrence, TI designed a series of split-rail devices; e.g., the SN74ALVC164245 and the SN74LVC4245, which have one side of the device powered at a 3.3-V level and the other side powered at a 5-V level. By having two different power supplies on the same device, the minimum voltage levels required for switching can be met and a 3.3-V logic part can essentially drive a 5-V CMOS device.

ac Performance

A desirable objective is for systems to operate at faster speeds that allow less time for performing operations. For example, consider the impact a continually increasing operating frequency has on accessing memory or on performing arithmetic computations; the faster the system runs, the less time is available for other support functions to be performed.

To meet this need, advances have been made in the fabrication of integrated circuits (ICs). Specifically in the low-voltage arena, the LV, LVC, ALVC, and LVT logic family fabrication geometries have undergone changes that have consistently improved their performance. This is shown in Figures 3 through 5, which compare the propagation delay times of LV, LVC, ALVC, and LVT devices for differing values of operating free-air temperature, number of outputs switching, and load capacitance.

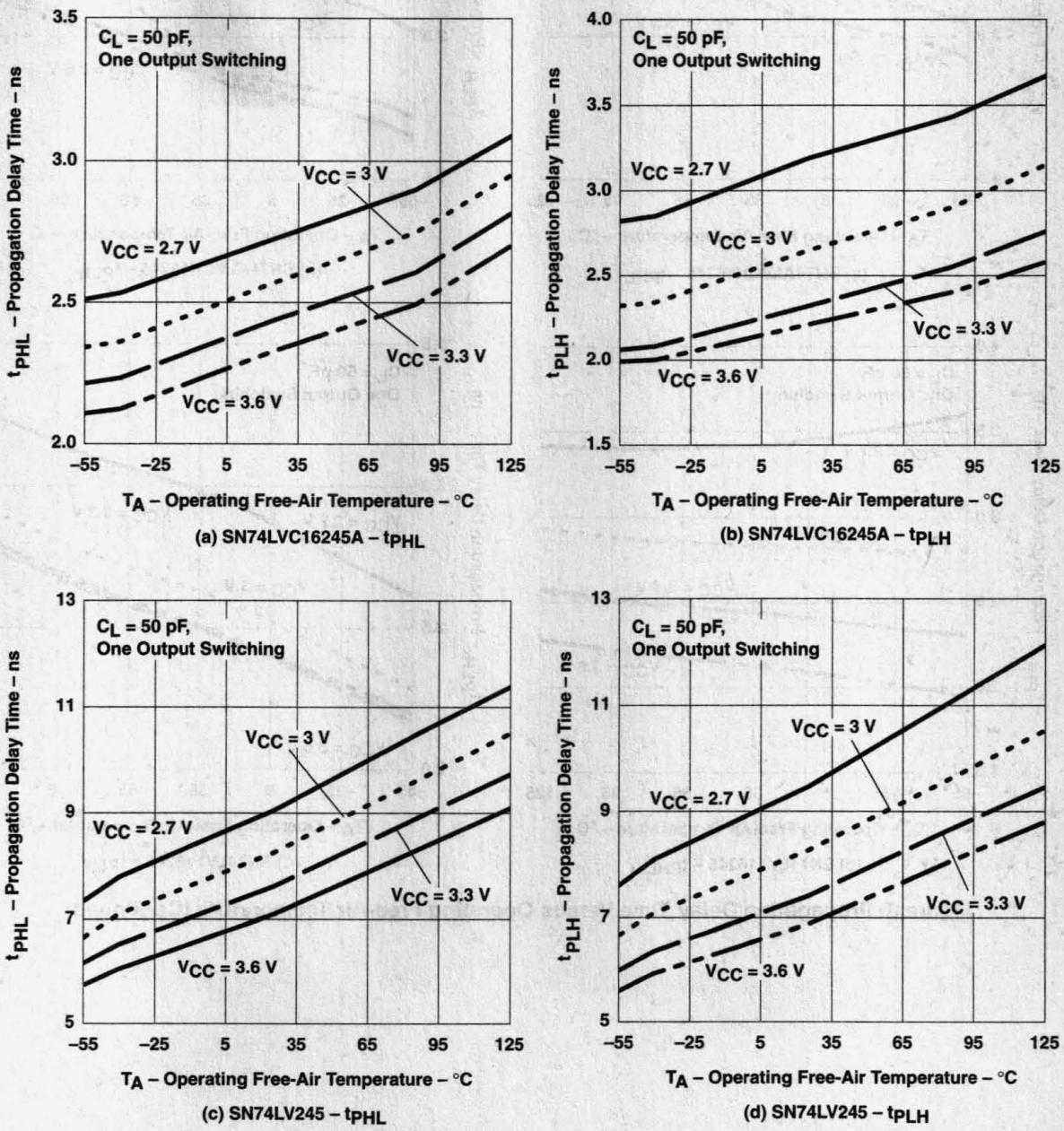
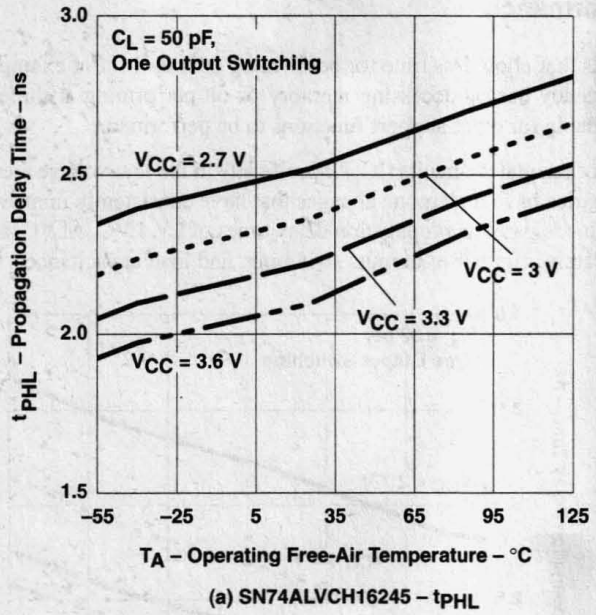
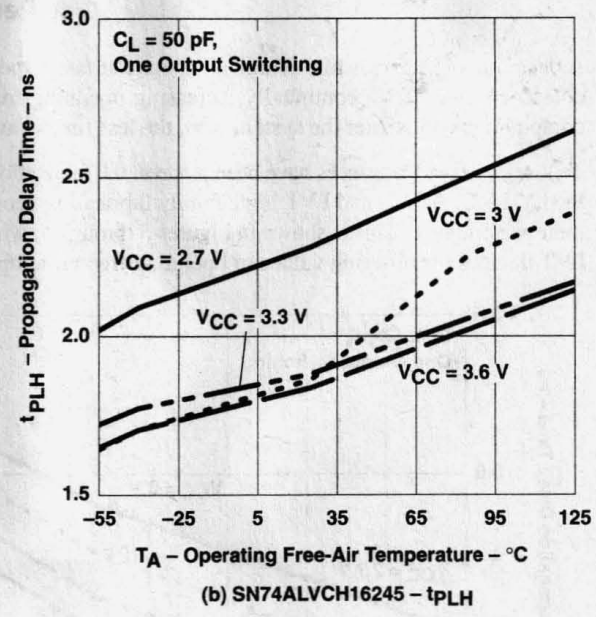


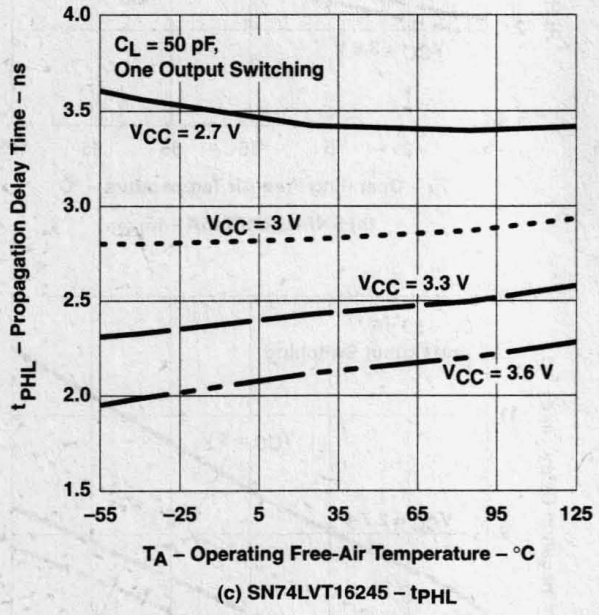
Figure 3. Propagation Delay Time Versus Operating Free-Air Temperature



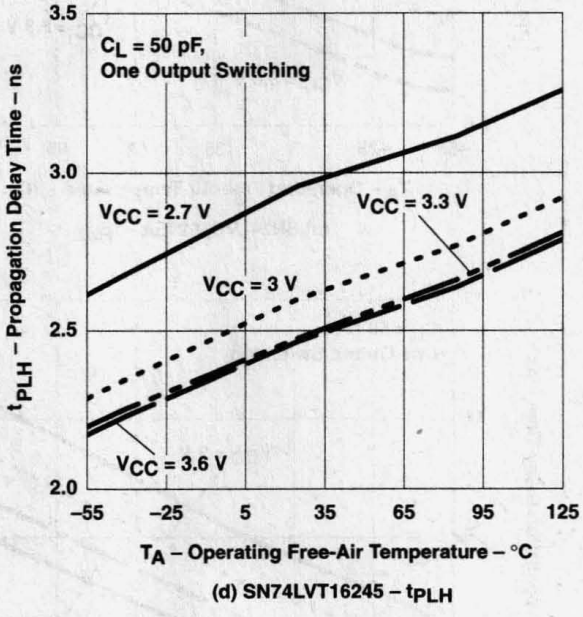
(a) SN74ALVCH16245 – t_{PHL}



(b) SN74ALVCH16245 – t_{PLH}

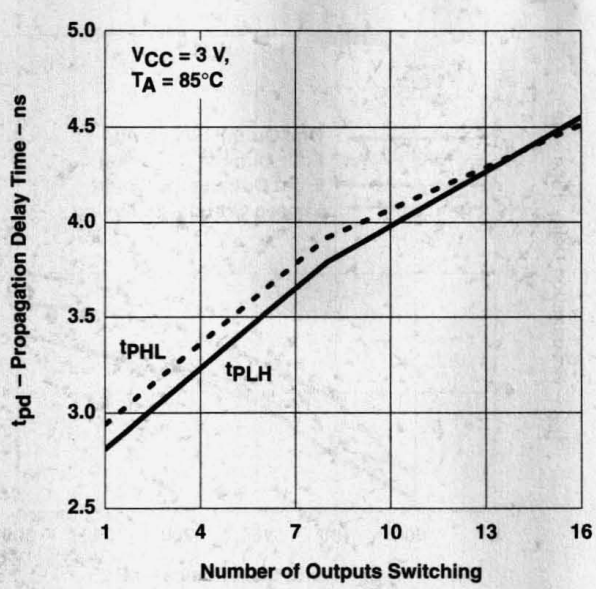


(c) SN74LVT16245 – t_{PHL}

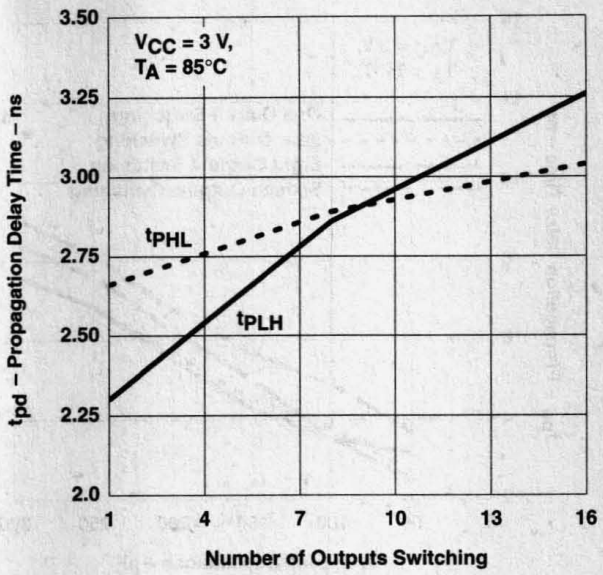


(d) SN74LVT16245 – t_{PLH}

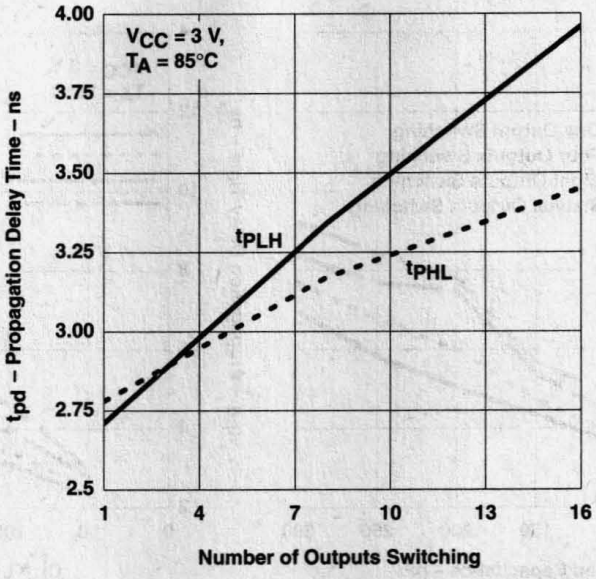
Figure 3. Propagation Delay Time Versus Operating Free-Air Temperature (Continued)



(a) SN74LVC16245A



(b) SN74ALVCH16245



(c) SN74LVT16245

Figure 4. Propagation Delay Time Versus Number of Outputs Switching

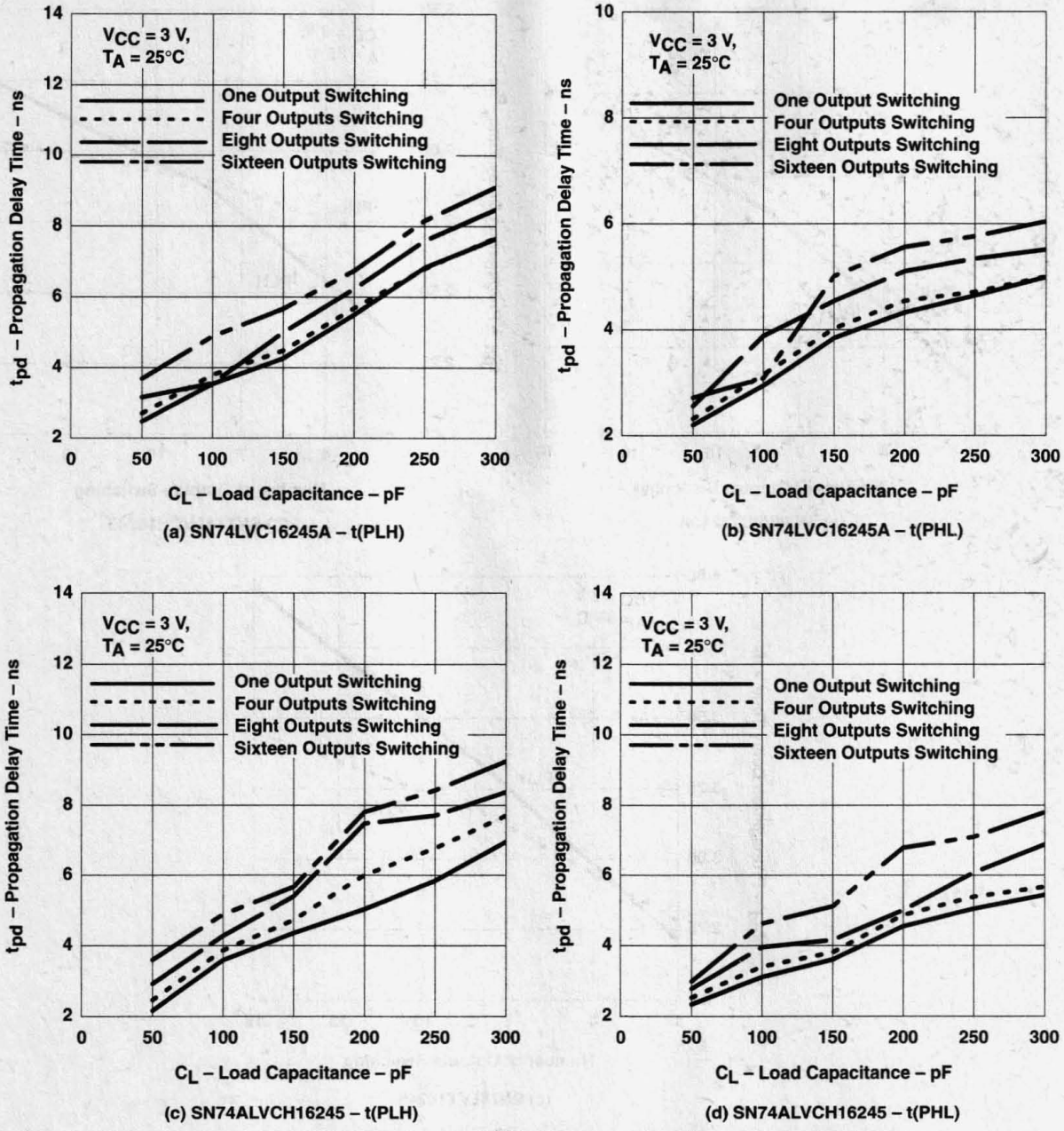


Figure 5. Propagation Delay Time Versus Load Capacitance

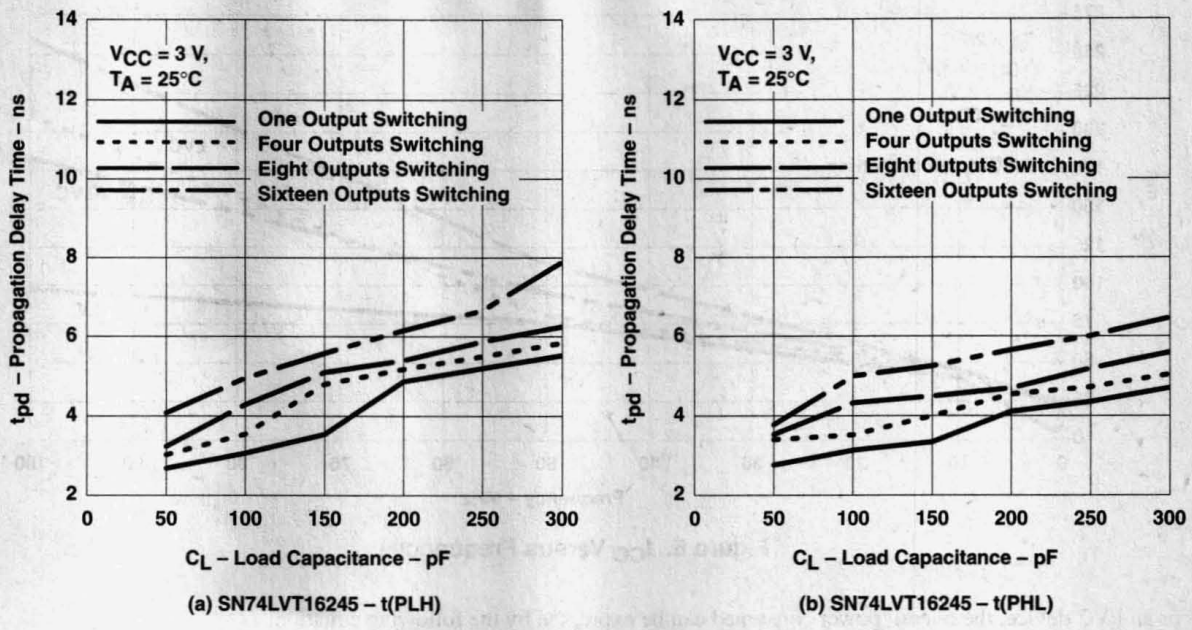


Figure 5. Propagation Delay Time Versus Load Capacitance (Continued)

Power Considerations

The continued general industry trend is to make devices more robust and faster while reducing their size and power consumption. The LVC family of devices uses a CMOS output structure that has low power consumption and provides a medium drive current capability.

When calculating the amount of power consumed, both static (dc) and dynamic (ac) power must be considered. A variable when computing static power is I_{CC} and is provided in the data sheet for each specific device. The LVC family I_{CC} typically offers one-half of the LV family I_{CC}, one-fourth of the ALVC family I_{CC}, and a small fraction of the LVT family I_{CC}.

The majority of power consumed is dynamic due to the charging and discharging of internal capacitance and external load capacitance. The internal parasitic capacitances are known as C_{pd} and are expressed by Equation 2.

$$C_{pd} = [(I_{CC}(\text{dynamic}) \div (V_{CC} \times f)] - C_L \quad (2)$$

Where:

I_{CC} = Measured value of current into the device (A)
V_{CC} = Supply voltage (V)
f = Frequency (Hz)
C_L = External load capacitance (F)

When comparing the dynamic power consumed between LV, LVC, ALVC and LVT, Figure 6 shows that pure CMOS devices (the LV, LVC, and ALVC families) consume approximately the same power as BiCMOS devices (the LVT family) around the frequency of 10 MHz, but consume significantly less power as the frequency approaches 100 MHz.

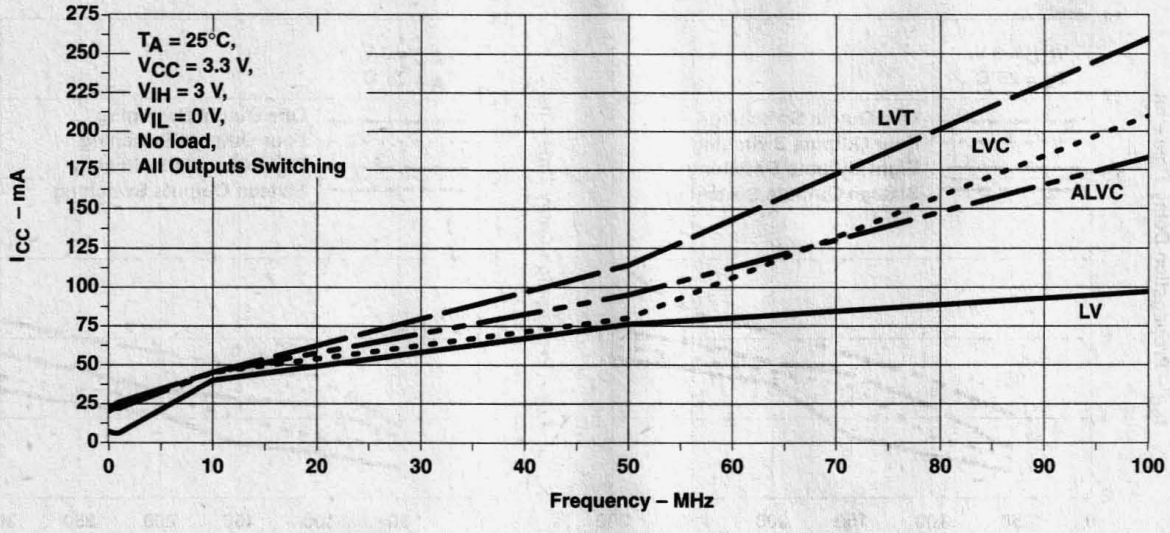


Figure 6. I_{CC} Versus Frequency

For an LVC device, the overall power consumed can be expressed by the following equation:

$$P_T = P_{(static)} + P_{(dynamic)} \quad (3)$$

Where:

for inputs with rail-to-rail signal swing:

$$P_S = V_{CC} \times I_{CC} \quad (4)$$
$$P_D = [(C_{pd} + C_L) \times V_{CC}{}^2 \times f] \times N_{SW}$$

and for TTL-level inputs:

$$P_S = V_{CC}[I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)] \quad (5)$$
$$P_D = [(C_{pd} + C_L) \times V_{CC}{}^2 \times f] \times N_{SW}$$

Where:

V_{CC} = Supply voltage (V)
I_{CC} = Power supply current (A)
C_{pd} = Power dissipation capacitance (F)
C_L = External load capacitance (F)
f = Operating frequency (Hz)
N_{SW} = Total number of outputs switching
N_{TTL} = Total number of outputs (where corresponding input is at the TTL level)
ΔI_{CC} = Power supply current (A) when inputs are at a TTL level
DC_d = % duty cycle of the data (50% = 0.5)

Input Characteristics

The LVC family input structure is such that the 3.3-V CMOS dc V_{IL} and V_{IH} fixed levels of 0.8 V and 2 V are ensured, meaning that while the threshold voltage of 1.5 V is typically where the transition from a recognized low input to a recognized high input occurs (see Figure 7), it is at the levels of 0.8 V and 2 V where the corresponding output state is ensured. Additionally, a reduction in overall bus loading exists in the LVC family due to the relatively high impedance and low capacitance characteristics of CMOS input circuitry.

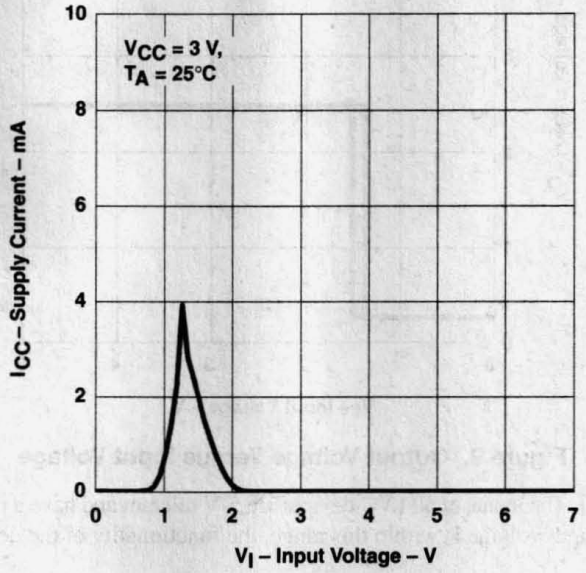


Figure 7. Supply Current Versus Input Voltage

LVC Input Circuitry

The simplified LVC input circuit shown in Figure 8 consists of two transistors, sized to achieve a threshold voltage of 1.5 V (see Figure 9). Since V_{CC} is 3.3 V and the threshold voltage is commonly set to be centered around one-half of V_{CC} in a pure CMOS input (see Figure 1), additional circuitry to reduce the voltage level is not required and the resulting simplified input structure consists of two transistors. When the input voltage V_I is low, the PMOS transistor (Q_p) turns on and the NMOS transistor (Q_n) turns off, causing current to flow through Q_p, resulting in the output voltage (of the input stage) to be pulled high. Conversely, when V_I is high, Q_n turns on and Q_p turns off, causing current to flow through Q_n, resulting in the output voltage (on the input stage) to be pulled low.

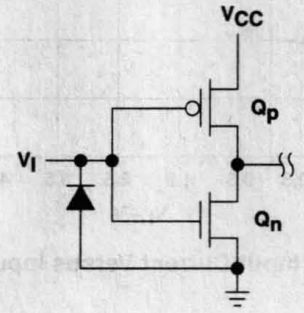


Figure 8. Simplified Input Stage of an LVC Circuit

Figure 9 is a graph of V_O versus V_I. An input hysteresis of approximately 100 mV is inherent to the LVC process geometry, which ensures the devices are free from oscillations by increasing the noise margin around the threshold voltage.

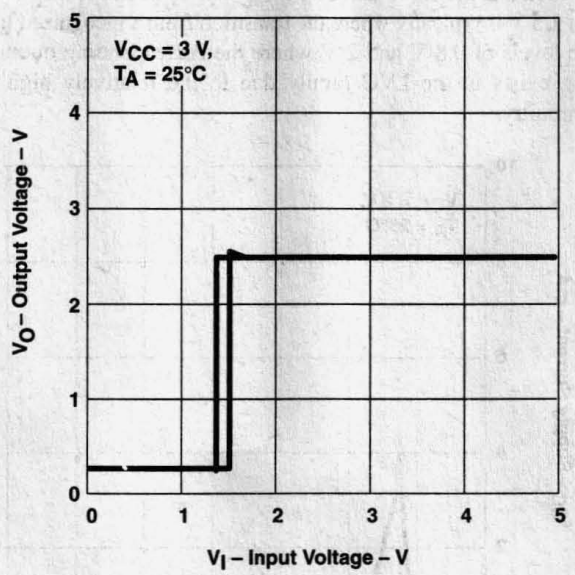


Figure 9. Output Voltage Versus Input Voltage

Figure 10 is a graph of I_I versus V_I. The inputs of all LVC devices are 5-V tolerant and have a recommended operating condition range from 0 V to 5.5 V. If the input voltage is within this range, the functionality of the device is ensured.

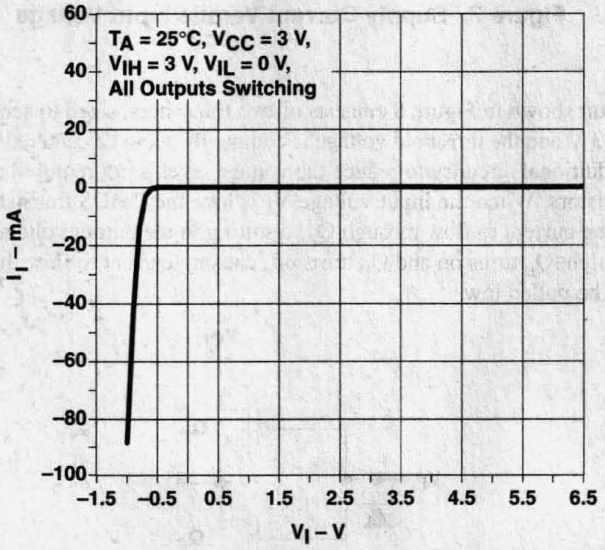


Figure 10. Input Current Versus Input Voltage

Input Current Loading

Minimal loading of the system bus occurs when using the LVC family due to the EPIC™ submicron process CMOS input structure; the only loading that occurs is caused by leakage current and capacitance. Input current is low, typically less than 100 pA, as shown in Figure 11 and Table 1. Capacitance for transceivers can be as low as 3.3 pF for C_i and 5.4 pF for C_{io}. Since both of the variables that can affect bus loading are relatively insignificant, the overall impact on bus loading on the input side using LVC devices is minimal and, depending upon the logic family being used, bus loading can decrease as a result of using LVC parts.

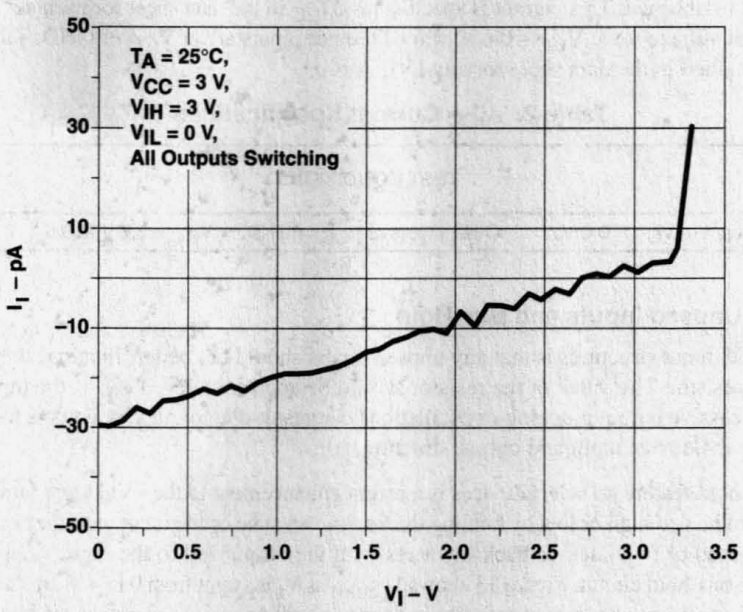


Figure 11. Input Leakage Current Versus Input Voltage

Table 1. Input Current Specifications

PARAMETER	TEST CONDITIONS		SN74LVC245A	
			MIN	MAX
I_I	V_I = 5.5 V or GND,	V_{CC} = 3.6 V		±5 µA
I_{OZ}†	V_O = V_{CC} or GND,	V_{CC} = MIN to MAX		±10 µA
I_{OZ}†	V_O = 3.6 V or 5.5 V,	V_{CC} = MIN to MAX		±50 µA

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

Supply Current Change (ΔI_{CC})

LVC devices operate using the switching standard levels shown in Figure 1. However, because the input circuitry is CMOS, an additional specification, ΔI_{CC}, is provided to indicate the amount of input current present when both p- and n-channel transistors are conducting. Although this situation exists whenever a low-to-high (or high-to-low) transition occurs, the transition usually occurs so quickly that the current flowing while both transistors are conducting is negligible. It is more of a concern, however, when a device with a TTL output drives the LVC part. Here, a dc voltage that is not at the rail, is applied to the input of the LVC device. The result is that both the n-channel transistor and the p-channel transistor are conducting and a path from V_{CC} to GND is established. This current is specified as ΔI_{CC} in the data sheet for each device and is measured one input at a time with the input voltage set at $V_{CC} - 0.6$ V, while all other inputs are at V_{CC} or GND. Table 2 provides the ΔI_{CC} specification, which is contained in the data sheet for any LVC part.

Table 2. ΔI_{CC} Current Specifications

PARAMETER	TEST CONDITIONS	SN74LVC245A	
		MIN	MAX
ΔI_{CC}	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND, V_{CC} = 2.7 V to 3.6 V		500 µA

Proper Termination of Unused Inputs and Bus Hold

A characteristic of all CMOS input structures is that any unused inputs should not be left floating; they should be tied high to V_{CC} or low to GND via a resistor. The value of the resistor should be approximately 1kΩ. If the inputs are not tied high or low but are left floating, excessive output glitching or oscillations can result due to induced voltage transients on the parasitic lead inductance inherent to the device input and output structure.

Implementation of the bus-hold feature on select devices is a recent enhancement to the LVC logic family. Bus hold eliminates the need for floating inputs to be tied high or low by holding the last known state of the input until the next input signal is present. Bus hold is a circuit composed of two back-to-back inverters with the output fed to the input via a resistor. Figure 12 is a simplified illustration of the bus-hold circuit. Figure 13 shows $I_{I(hold)}$ as V_I is swept from 0 to 4 V. Bus hold is beneficial because of the decreased expense of purchasing additional resistors, reduced overall power consumption, and because it frees up limited board space.

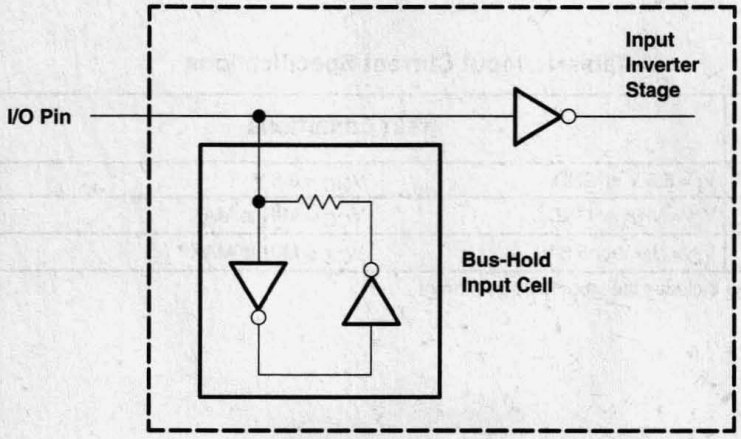


Figure 12. Bus Hold

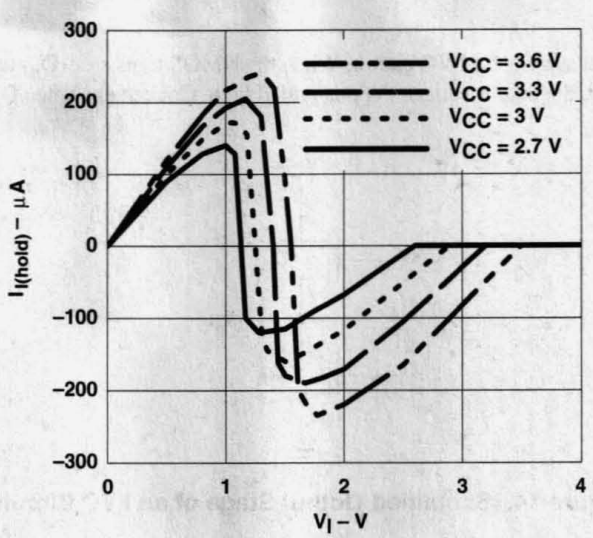


Figure 13. $I_{I(hold)}$ Versus V_I

Not all LVC devices have the bus-hold feature. Those that do are identified by the letter H added to the device name; e.g., SN74LVCH245. Additionally, any device with bus hold has an $I_{I(hold)}$ specification in the data sheet. Finally, bus hold does not contribute significantly to input current loading or output driving loading because it has a minimum hold current of 75 μA and a maximum hold current of 500 μA as shown in Table 3.

Table 3. Bus-Hold Specifications [$I_{I(hold)}$]

PARAMETER	TEST CONDITIONS		SN74LVC245	
			MIN	MAX
$\Delta I_{I(hold)}$	V_I = 0.8 V,	V_{CC} = 3 V	75 μA	
	V_I = 2 V,	V_{CC} = 3 V	−75 μA	
	V_I = 0 to 3.6 V,	V_{CC} = 3.6 V		±500 μA

Output Characteristics

The LVC family uses a pure CMOS output structure. This is true of all low-voltage families except the LVT family, which uses both bipolar and CMOS circuitry. The LVC family has the dc characteristics shown in Table 4.

Table 4. LVC Output Specifications

PARAMETER	TEST CONDITIONS		SN74LVC244A		
			MIN	TYP	MAX
V_{OH}	I_{OH} = −100 μA,	V_{CC} = MIN to MAX	V_{CC}–0.2 V		
	I_{OH} = −12 mA,	V_{CC} = 2.7 V	2.2 V		
	I_{OH} = −12 mA,	V_{CC} = 3 V	2.4 V		
	I_{OH} = −24 mA,	V_{CC} = 3 V	2.2 V		
V_{OL}	I_{OL} = 100 μA,	V_{CC} = MIN to MAX			0.2 V
	I_{OL} = 12 mA,	V_{CC} = 2.7 V			0.4 V
	I_{OL} = 24 mA,	V_{CC} = 3 V			0.55 V
I_{OZ}†	V_O = V_{CC} or GND,	V_{CC} = MIN to MAX			±10 μA
I_{OZ}†	V_O = 3.6 V to 5.5 V,	V_{CC} = MIN to MAX			±50 μA
C_o	V_O = V_{CC} or GND,	V_{CC} = 3.3 V		5 pF	

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

LVC Output Circuitry

Figure 14 shows a simplified output stage of an LVC circuit. When the NMOS transistor (Q_n) turns off and the PMOS transistor (Q_p) turns on and begins to conduct, the output voltage (V_O) is pulled high. Conversely, when Q_p turns off, Q_n begins to conduct and V_O is pulled low.

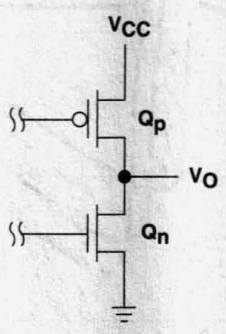


Figure 14. Simplified Output Stage of an LVC Circuit

Output Drive

Figure 15 illustrates values of I_{OL} and I_{OH} and the corresponding values of V_{OL} and V_{OH} for a typical LVC device.

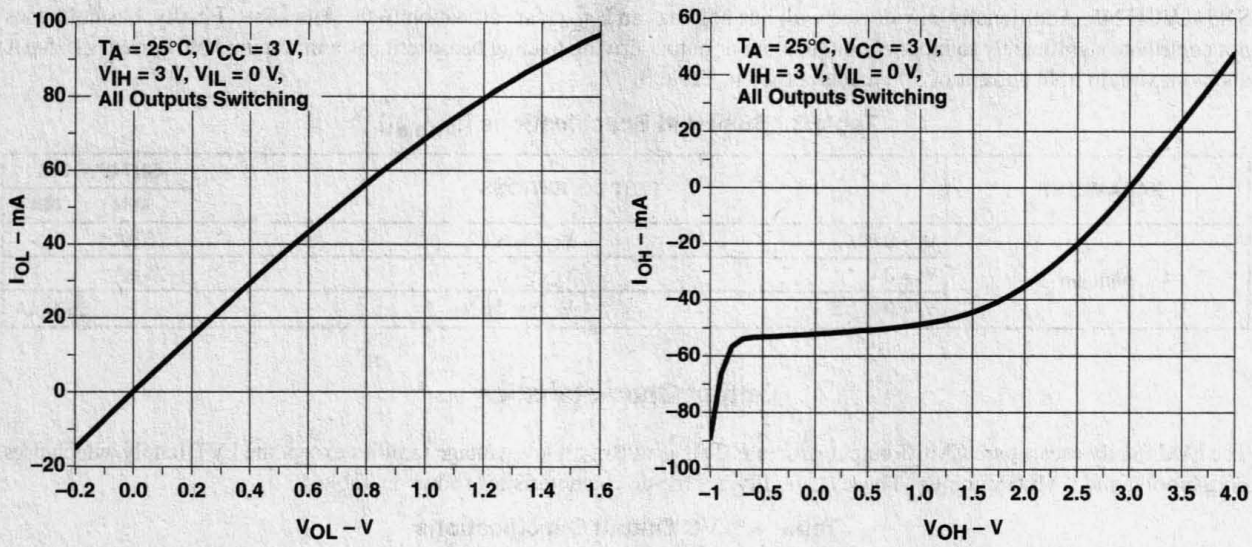


Figure 15. Typical LVC Output Characteristics

Partial Power Down

To partially power down a device, no paths from V_I to V_{CC} or from V_O to V_{CC} can exist. With the LVC family, a path from V_I to V_{CC} has never been an issue. However, early LVC devices that were not 5-V tolerant do have a path from V_O to V_{CC}. For these devices, when V_{CC} begins to diminish, a diode from V_O to V_{CC} begins to conduct and current flows, resulting in damage to the power supply and or to the device. Today, the 5-V tolerant LVC devices are designed in such a way that this path from V_O to V_{CC} is eliminated. As such, 5-V tolerant devices are capable of being partially powered down.

Proper Termination of Outputs

Depending on the trace length, special consideration may need to be given to the termination of the outputs. As a general rule, if the trace length is less than four inches, no additional components are necessary to achieve proper termination. If the trace length is greater than four inches, reflections begin to appear on the line and the system may appear noisy and generate unreliable data. The solution to this is to terminate the outputs in an appropriate manner to minimize the reflections.

Figure 16 illustrates five different techniques for terminating the outputs. The ideal situation is to identically match the impedance (Z_O) of the trace and eliminate all reflections. In practice, however, exactly matching Z_O is not always possible and settling for a close enough match that adequately minimizes the reflections may be the only option.

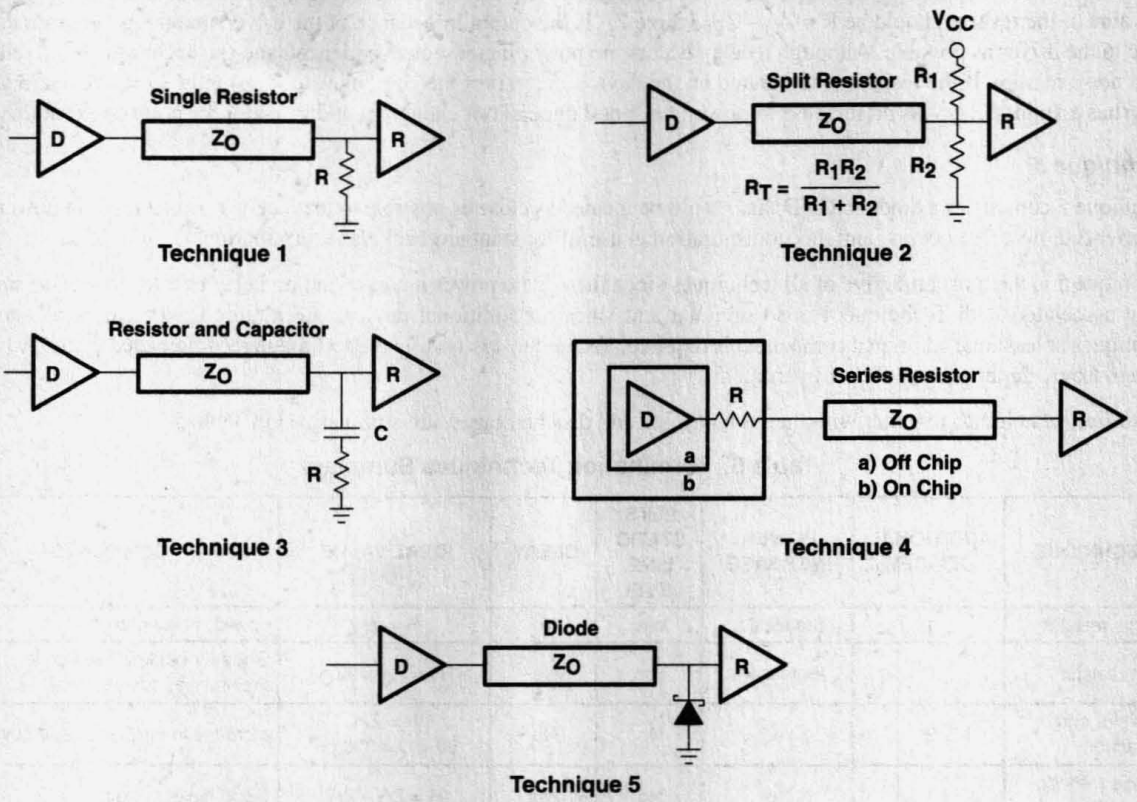


Figure 16. Termination Techniques

Technique 1

Technique 1 consists of a single resistor tied to GND. The ideal value of the resistor is $R = Z_O$, and the best placement for it is as close to the receiver as possible. A heavy increase in power occurs, but no further delay is present. There is a relatively low dc noise margin in this configuration.

Technique 2

Technique 2 involves two split resistors; one resistor (R_1) is tied to V_{CC} and the other (R_2) is tied to GND. The ideal value of the resistors is $R_1 = R_2 = 2Z_O$; $RT = (R_1 \times R_2)/(R_1 + R_2)$, and the best placement for the resistors is as close to the receiver as possible. Technique 2 results in a heavy increase in power, with no delay being experienced, and is primarily used in backplane designs where proper drive currents must be maintained.

Technique 3

Technique 3 has a capacitor in series with a resistor, both of which are running parallel to GND. The ideal value of the resistor is $R = Z_O$, and the value of the capacitor should be $60pF < C < 330$ pF. To determine the ideal value of the capacitor, it is recommended that a model simulation tool be used. The ideal placement of the resistor and capacitor is as close to the receiver as possible. Technique 3 has the highest amount of power consumed as the frequency increases, but no additional delay is experienced. Note that this termination technique can be optimized for only one given signal frequency.

Technique 4

Technique 4 consists of a resistor in series with the output of the driving device and can be divided into two alternatives, depending on whether the resistor is physically located on or off the driving device. If the resistor is not located on the device, the value of the resistor should be $R = Z_O - Z_D$, where Z_D is the output impedance of the driver, and the best placement is as close to the driver as possible. Although a delay occurs, no power increase is experienced and this technique has a relatively good noise margin. If the resistor is integrated on the device and part of the chip, its value is usually $25 = < R = < 33\ \Omega$. This setup has a slight delay, has no increase in power, has good undershoot clamping, and is useful for point-to-point driving.

Technique 5

Technique 5 consists of a diode to GND that should be located as close as possible to the receiver. An increase in power is not experienced, no delay occurs, and this configuration is useful for standard backplane terminations.

Technique 5 is the most attractive of all techniques since there is no power increase and no delay occurs. However, since the delay associated with Technique 4 is so minimal and since no additional devices are required, whereas in all the other techniques at least one additional component is required, Technique 4 is usually the technique recommended by the Advanced System Logic department of Texas Instruments.

These five techniques, together with their advantages and disadvantages, are summarized in Table 5.

Table 5. Termination Techniques Summary

TECHNIQUE	ADDITIONAL DEVICES	POWER INCREASE	SETS STATIC LINE LEVEL	DELAY	IDEAL VALUE	COMMENTS
Single resistor	1	Significant	Yes	No	$R = Z_O$	Low dc noise margin
Split resistor	2	Significant	Yes	No	$R_1 = R_2 = 2Z_O$	Good for backplanes due to maintaining drive current
Resistor and capacitor	2	Yes	No	No	$R = Z_O$ $60 < C < 330$ pF	Increase in frequency and power
Series resistor, off device	1	No	No	Yes	$R = Z_O - Z_D$	Good noise margin
Series resistor, on device	0	No	No	Small	$25 = < R = < 33\ \Omega$	Good undershoot clamping; useful for point-to-point driving
Diode	1	No	No	No	NA	Good undershoot clamping; useful for standard backplane terminations

Signal Integrity

System designers often are concerned with the performance of a device when the outputs are switched. The most common method of assessing this is by observing the impact on a single output when multiple outputs are switched.

The phenomenon of simultaneous switching can be measured with respect to GND or with respect to V_{CC}. When measuring with respect to GND, the voltage output low peak (V_{OLP}) is the impact on one quiet, logic-low output when all the other outputs are switched from high to low. The converse is true when measuring simultaneous switching with respect to V_{CC}; i.e., the voltage output high valley (V_{OHV}) is the impact on one quiet, logic-high output when all the other outputs are switched from low to high. Figure 17 shows an example of simultaneous switching with respect to V_{OLP} and V_{OHV}.

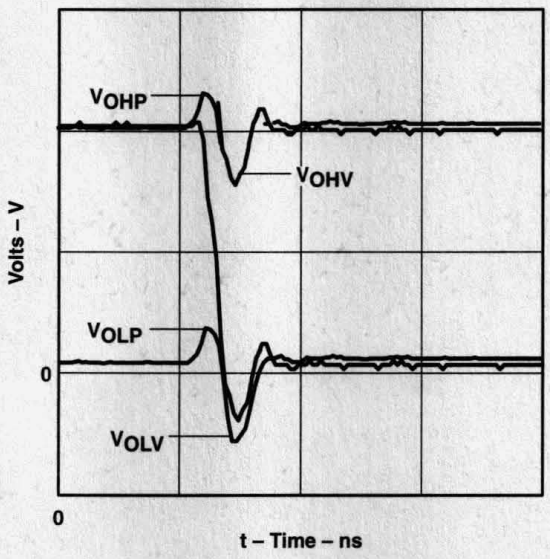


Figure 17. Simultaneous Switching Noise Waveform

One technique to reduce the impact of simultaneous switching on a device is to increase the number of power and GND pins. The strategy is to disperse them throughout the chip to reduce mutual inductances between signals (see *Advanced Packaging*). For a complete discussion of simultaneous switching, refer to TI's *Simultaneous Switching Evaluation and Testing* application report or the *Advanced CMOS Logic Designer's Handbook*, literature number SCAA001A.

Acknowledgment

This application report was written by Steven Culp, ABL applications engineering.

Mixing It Up With 3.3 Volts

SCBA005
July 1994

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Please be aware that TI products are not intended for use in life-support appliances, devices, or systems. Use of TI product in such applications requires the written approval of the appropriate TI officer. Certain applications using semiconductor devices may involve potential risks of personal injury, property damage, or loss of life. In order to minimize these risks, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards. Inclusion of TI products in such applications is understood to be fully at the risk of the customer using TI devices or systems.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1994, Texas Instruments Incorporated

Printed in the U.S.A.

Contents

Title	*Page*
Introduction	**5–49**
The Market for Low Voltage	**5–50**
Migration to 3.3 V	**5–50**
Mixed-Mode Operation	**5–51**
LVT Family Characteristics	**5–52**
Bus Hold	**5–53**
Conclusion	**5–54**
Acknowledgment	**5–54**

List of Illustrations

Figure	*Title*	*Page*
1	3-V to 5-V Power Versus Frequency Comparison	5–49
2	Comparison of 3.3-V and 5-V Interfaces	5–51
3	Simplified LVT Output Structure	5–53
4	ABT Versus LVT Output Drive Comparison	5–53

Widebus is a trademark of Texas Instruments Incorporated.

Introduction

The evolution to a 3.3-V supply voltage is being driven by a complex matrix of requirements. Leading the way are the characteristics of advanced semiconductor processing and the need to reduce system power without a corresponding tradeoff in system performance. Reduction of the horizontal and vertical feature sizes of transistors is the most common method of increasing the density of cells that can be contained in an integrated circuit. These feature sizes or geometries are typically represented as minimum process dimensions for advanced products such as dynamic random access memories (DRAMs).

DRAM manufacturers have forecasted that all 64M-bit versions will be developed for operation from a supply voltage of 3.3 ± 0.3 V. For 16M-bit DRAM products, there is no such rule of thumb as certain vendors expect to operate from 3.3 V, while others offer different product versions with differing voltage levels. An approach used by several manufacturers is to provide 5-V power-supply operation externally with internal step-down conversion to 3.3 V. For static random access memories (SRAMs), manufacturers have announced that most 16M versions will operate at 3.3 V or lower (down to 2.7 V).

Typical 1M-bit DRAM geometries are on the order of 1.2 µm and it is not a problem to apply a 5-V power supply to this type of product. However, as the feature sizes of DRAMs shrink, the stresses of 5-V operation can preclude their reliable operation due to high field-effect failures. One such effect is hot-carrier injection that over time increases the transistor's threshold, leading to eventual nonoperation. Another field-effect concern is the breakdown of the transistor's gate oxide causing internal shorts; therefore, reducing the supply voltage is one way to ensure reliable operation of devices fabricated in state-of-the-art processes.

The reduction of V_{CC} from 5 V to 3.3 V reduces the power consumed by the device, which increases system reliability while reducing costs associated with the removal of the heat. The power consumption of a device is primarily a function of its capacitive load, frequency of operation, and supply voltage. However, capacitive load and frequency have a linear effect on a device's power consumption while supply voltage has a square relationship. Because of this square relationship, a small reduction in voltage significantly reduces the power consumed, as illustrated in Figure 1, and is a driving factor to 3.3-V operation.

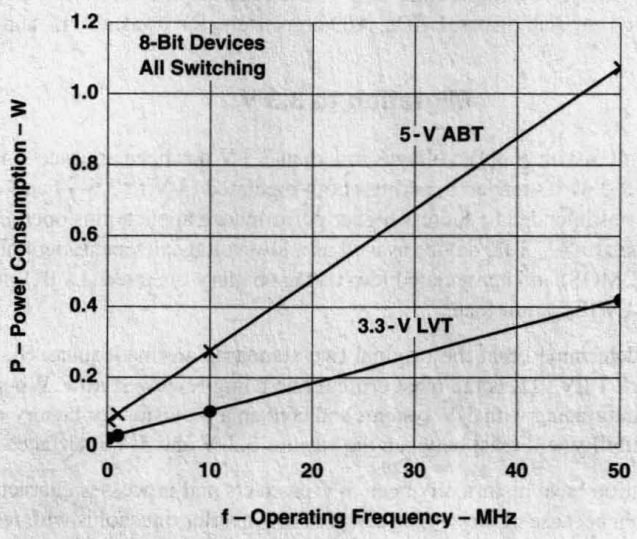


Figure 1. 3-V to 5-V Power Versus Frequency Comparison

The Market for Low Voltage

User demand for low-voltage products can be grouped into specific brackets depending on their performance-power priorities. End equipments, such as multiuser servers, engineering workstations, high-end desktop PCs, and other high-performance motherboards, favor high performance over low power, but are interested in 3.3-V products to reduce or eliminate bulky, noisy cooling fans in the attempt to shrink external case size for better desktop fit. Some end equipments favor low power at the expense of high performance such as battery-powered notebooks and palmtop computers, portable test equipment, and point-of-sale terminals. A few end equipments require equal priority for high performance and low power, such as laptop computers, automotive, and air/space products.

The universal benefits to users of low-voltage products are higher reliability and lower cost. The higher reliability is relative to standard 5-V solutions and results from lower stress gradients on device junctions and oxides, lower buildup of heat due to lower power consumption, and improved signal integrity from the reduction in ground bounce and signal noise. Lower power consumption usually yields lower costs since power costs money to generate and heat costs money to dissipate. All things considered, it is desirable to use inexpensive plastic packages instead of metal or ceramic to dissipate heat. For battery users, an added benefit of the lower power consumption of low-voltage products is one of increased battery lifetime.

Of all the end-equipment groups that can benefit from the use of low-voltage products, it appears that demand will be initially driven by battery-operated computers. This market segment is defined by notebook and palmtop computers, as well as point-of-sale terminals, which are designed to capture data at remote field sites and either store it for downloading later or transmit it real time via an on-board transmitter. The goal for these systems is to have a battery life of eight to ten hours, roughly the equivalent of one workday or the time to complete a transcontinental airplane trip.

The unregulated battery market is itself quite varied however, because different batteries exhibit very different voltage characteristics between fully charged and discharged states. Two AA batteries provide for 3-V supply when charged, decreasing to about 2.7 V after use. Three NiCad batteries provide for a baseline 3.6-V supply fully charged, but the spread actually runs from about 3.3 V up to 3.9 V. For now, the unregulated battery market demands low-voltage products that are optimized to run from 2.7 V up as high as 3.9 V. Since performance is directly related to supply voltage, it is more important for device optimization to be extended down to 2.7 V, where devices slow down appreciably.

There are some barriers for low-voltage acceptance in the short term. Specification standardization remains an issue. Also, the access to adequate supplies of 3.3-V devices can be a problem. Generally, DRAM memories are leading the way into 3.3-V operation with SRAM memories close behind. Coupled with the low-voltage microprocessors now available, systems are being implemented with the core components operating at 3.3 V. Hindering the migration to a full 3.3-V system is the availability of support products such as: disk drives, LCDs, A/D converters, RF transmitters, and EPROMS.

Migration to 3.3 V

The need to migrate to power supplies with supply voltages less than 3.3 V has been an issue since 1984 when two JEDEC standards were adopted. Standard 8.0 was intended to address both regulated (3-V to 3.6-V) and unregulated (2-V to 3.6-V) battery applications. Standard 8.1 was intended to address higher-performance applications operating from a regulated power supply that could interface to a standard 5-V TTL device as well as a low-voltage device. Essentially Standard 8.0 established regulated low-voltage CMOS (LVCMOS) and unregulated low-voltage battery-operated (LVBO) interfaces, and Standard 8.1 established the low-voltage TTL (LVTTL) interface.

Committee members have since determined that the original two standards are inadequate. Since most systems currently require a TTL interface, Standard 8.1 LVTTL is the most critical one being reviewed now. When ratified, the new LVTTL standard will present methods for interfacing with 5-V systems and contain a provision for battery-operated systems. Until this happens, a generic lack of compatibility will exist between the various 3.3-V and 5-V interfaces.

Existing solutions for 3.3-V operation have historically been 5-V products and processes characterized for 3.3-V operation. A CMOS process is typically chosen because of the scaling effect of the inverter thresholds with respect to the supply voltage. HCMOS and Advanced CMOS devices support both 5-V and 3.3-V operation by this method. One drawback is slower propagation delay when compared to parts specifically designed for 3-V operation. A limitation of many of these devices is their inability to directly interface to a 5-V system when running off a 3.3-V supply, due to diodes from the input and input/output (I/O) pins to V_{CC}. This limits input voltages to $V_{CC} + 0.5$ V and limits direct connection to a 5-V system.

Mixed-Mode Operation

This dilemma of device incompatibility between the large installed base of 5-V systems with the newly emerging 3.3-V systems is a serious industry concern. Mixed-mode operation allows for direct communication between the two systems. Devices that support this mode must be designed for maximum input voltages of 5.5 V, without any long-term reliability issues. Another concern is that the output drive must be capable of driving a standard-TTL backplane, while still providing for rail-to-rail switching for compatibility with 3-V CMOS systems.

Figure 2 compares the standard-TTL dc interface levels with two of the emerging low-voltage standards. Low-voltage CMOS (LVCMOS) is a pure CMOS specification that specifies low current rail-to-rail output drive along with input voltage levels, V_{IH} and V_{IL}, which are ratios of V_{CC}. Low-voltage TTL (LVTTL) utilizes the standard-TTL input levels of 0.8 V and 2 V, as well as specifying a higher dc output drive than LVCMOS. To ensure interoperability between these three varied standards, a multipurposed low-voltage interface device must meet all of the requirements of the three different specifications.

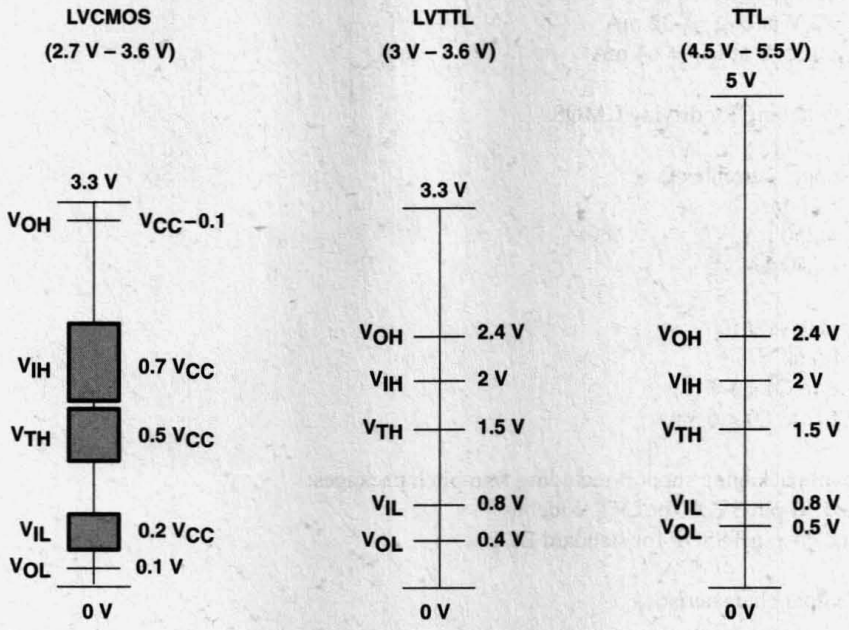


Figure 2. Comparison of 3.3-V and 5-V Interfaces

LVT Family Characteristics

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic devices capable of mixed-mode operation. The LVT series of devices rely on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT devices and provides the following family characteristics:

5.5-V maximum input voltage

Specified 2.7-V to 3.6-V supply voltage

I/O structures that support power-on (live) insertion

Standard TTL output drives of:
V_{OH} = 2 V at I_{OH} = –32 mA
V_{OL} = 0.55 V at I_{OL} = 64 mA

Rail-to-rail switching for driving CMOS

Maximum supply currents of:
I_{CCL} = 15 mA
I_{CCH} = 250 μA
I_{CCZ} = 250 μA

Propagation delays of:
t_{pd} < 4.6 ns
t_{pd} (LE to Q) < 5.1 ns
t_{pd} (CLK to Q) < 6.3 ns

Surface-mount packaging support including fine-pitch packages:
48- and 56-pin SSOP for LVT Widebus™
20- and 24-pin TSSOP for standard LVT

LVT input/output characteristics

Figure 3 shows a simplified LVT output and illustrates the mixed-mode signal drive designed into the output stage. This combination of a high-drive TTL stage with the rail-to-rail CMOS switching gives the LVT series of product extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices, as shown in Figure 4, providing the dc drive needed for existing 5-V backplanes and allowing for a simple solution to reduce system power via the migration to 3.3-V operation.

Not only can LVT devices operate as 3-V-to-5-V level translators by supporting input or I/O voltages of 5.5 V with V_{CC} = 2.7 V to 3.6 V, the inputs can withstand 5.5 V even when V_{CC} = 0 V. This allows for the devices to be used under partial system power-down applications or when live insertion is required.

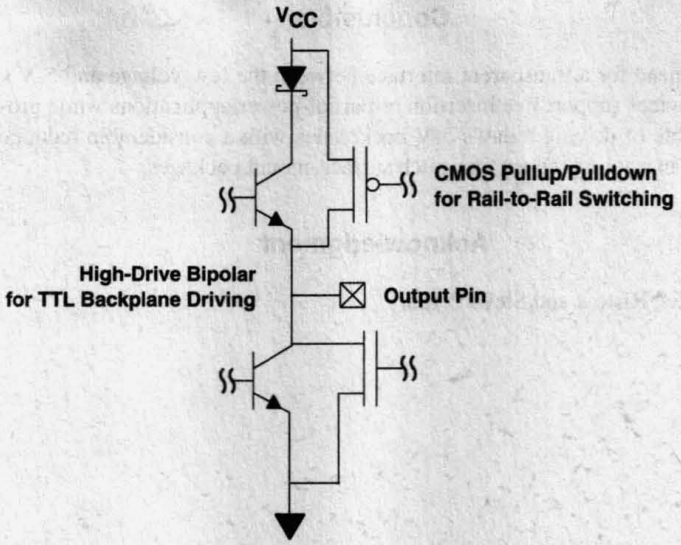


Figure 3. Simplified LVT Output Structure

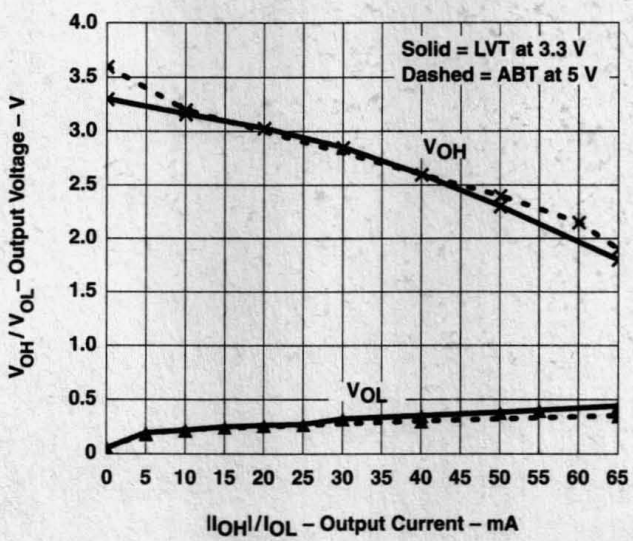


Figure 4. ABT Versus LVT Output Drive Comparison

Bus Hold

Many times devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor is typically used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporate active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, ±100 μA, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately ±500 μA, to toggle the state of the input. This current is negligible when compared to the magnitude of current that is needed to charge a capacitive load and does not affect the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent interface between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live insertion or partial-power applications while providing low-input leakage currents. The outputs are capable of driving today's 5-V backplanes with a considerable reduction in the device's power consumption and are packaged in state-of-the-art fine-pitch surface-mount packages.

Acknowledgment

The authors of this report are Ken Ristow and Steve Perna.

CMOS Power Consumption and C_{pd} Calculation

SCAA035A
March 1997

Texas Instruments

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**5–59**
Power-Consumption Components	**5–59**
Static Power Consumption	**5–59**
Dynamic Power Consumption	**5–61**
Transient Power Consumption	5–61
Capacitive-Load Power Consumption	5–62
Power-Dissipation Capacitance (C_{pd}) in CMOS Circuits	**5–63**
Testing Considerations	5–63
Test Conditions	5–64
Calculating C_{pd}	5–64
C_{pd} Measurement Procedures	5–64
Determination of C_{pd} (Laboratory Testing)	5–65
Comparison of Supply Current Versus Frequency	**5–67**
Power Economy	**5–70**
Conclusion	**5–70**
Acknowledgment	**5–70**

List of Illustrations

Figure	*Title*	*Page*
1	CMOS Inverter Mode for Static-Power Consumption	5–60
2	Model Describing Parasitic Diodes Present in CMOS Inverter	5–60
3	Hex Inverter AHC04	5–64
4	Several Circuits Switching, AHC374	5–65
5	I_{CC} vs Frequency for AHC00	5–65
6	Input Waveform	5–66
7	Power Consumption With All Outputs Switching	5–68
8	Power Consumption With a Single Output Switching	5–69

Introduction

Reduction of power consumption makes a device more reliable. The need for devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies. As a result, CMOS devices are best known for low power consumption. However, for minimizing the power requirements of a board or a system, simply knowing that CMOS devices may use less power than equivalent devices from other technologies does not help much. It is important to know not only how to calculate power consumption, but also to understand how factors such as input voltage level, input rise time, power-dissipation capacitance, and output loading affect the power consumption of a device. This application report addresses the different types of power consumption in a CMOS logic circuit, focusing on calculation of power-dissipation capacitance (C_{pd}), and, finally, the determination of total power consumption in a CMOS device.

The main topics discussed are:

- Power-consumption components
- Static power consumption
- Dynamic power consumption
- Power-dissipation capacitance (C_{pd}) in CMOS circuits
- C_{pd} comparison among different families
- Power economy
- Conclusion

Power-Consumption Components

High frequencies impose a strict limit on power consumption in computer systems as a whole. Therefore, power consumption of each device on the board should be minimized. Power calculations determine power-supply sizing, current requirements, cooling/heatsink requirements, and criteria for device selection. Power calculations also can determine the maximum reliable operating frequency.

Two components determine the power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

CMOS devices have very low static power consumption, which is the result of leakage current. This power consumption occurs when all inputs are held at some valid logic level and the circuit is not in charging states. But, when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption.

This application report addresses power consumption in CMOS logic families (5 V and 3.3 V) and describes the methods for evaluating both static and dynamic power consumption. Additional information is also presented to help explain the causes of power consumption, and present possible solutions to minimize power consumption in a CMOS system.

Static Power Consumption

Typically, all low-voltage devices have a CMOS inverter in the input and output stage. Therefore, for a clear understanding of static power consumption, refer to the CMOS inverter modes shown in Figure 1.

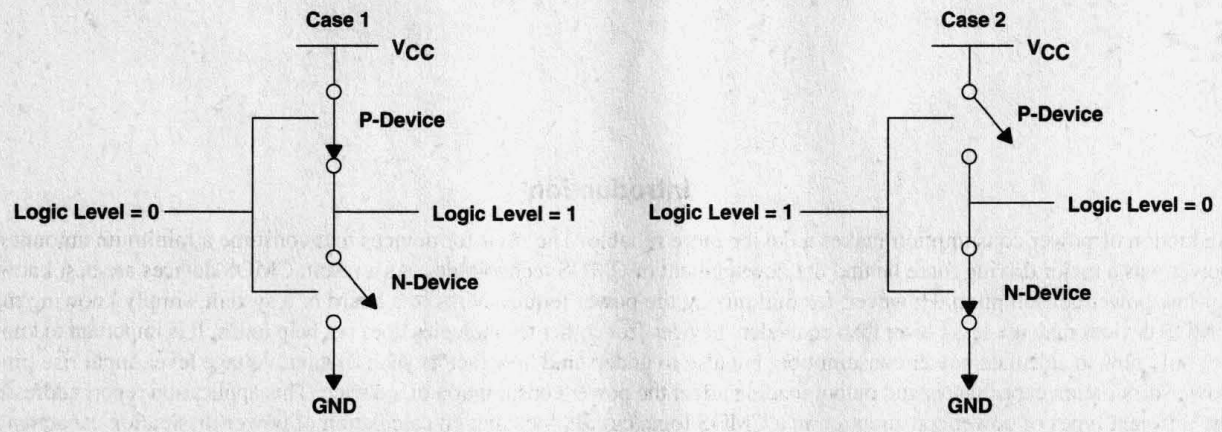


Figure 1. CMOS Inverter Mode for Static Power Consumption

As shown in Figure 1, if the input is at logic 0, the n-MOS device is OFF, and the p-MOS device is ON (Case 1). The output voltage is V_{CC}, or logic 1. Similarly, when the input is at logic 1, the associated n-MOS device is biased ON and the p-MOS device is OFF. The output voltage is GND, or logic 0. Note that one of the transistors is always OFF when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no dc current path from V_{CC} to GND, the resultant quiescent (steady-state) current is zero, hence, static power consumption (P_q) is zero.

However, there is a small amount of static power consumption due to reverse-bias leakage between diffused regions and the substrate. This leakage inside a device can be explained with a simple model that describes the parasitic diodes of a CMOS inverter, as shown in Figure 2.

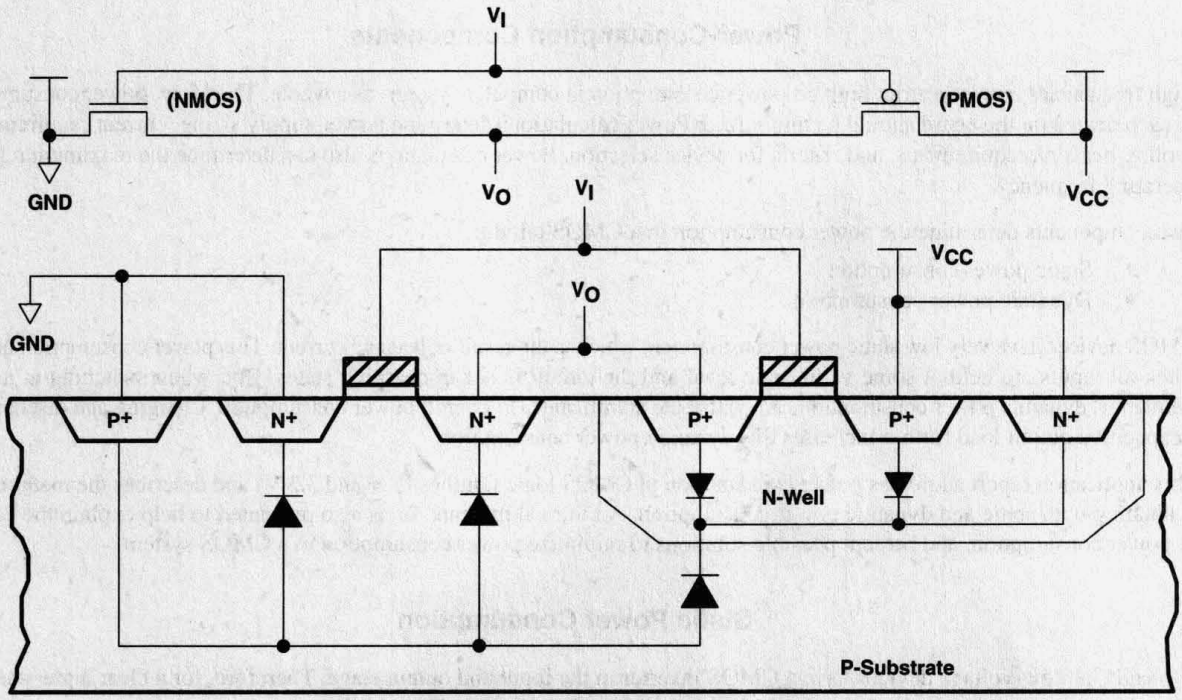


Figure 2. Model Describing Parasitic Diodes Present in CMOS Inverter

The source drain diffusion and N-well diffusion form parasitic diodes. In Figure 2, the parasitic diodes are shown between the N-well and substrate. Because parasitic diodes are reverse biased, only their leakage currents contribute to static power consumption. The leakage current (I_{lkg})of the diode is described by the following equation:

$$I_{lkg} = i_s\left(e^{qV/kT} - 1\right) \quad (1)$$

Where:

i_S = reverse saturation current
V = diode voltage
k = Boltzmann's constant (1.38×10^{-23} J/K)
q = electronic charge (1.602×10^{-19} C)
T = temperature

Static power consumption is the product of the device leakage current and the supply voltage. Total static power consumption, P_S, can be obtained as shown in equation 2.

$$P_S = \Sigma \text{ (leakage current)} \times \text{(supply voltage)} \quad (2)$$

Most CMOS data sheets specify an I_{CC} maximum in the 10-µA to 40-µA range, encompassing total leakage current and other circuit features that may require some static current not considered in the simple inverter model.

The leakage current I_{CC} (current into a device), along with the supply voltage, causes static power consumption in the CMOS devices. This static power consumption is defined as quiescent, or P_S, and can be calculated by equation 3.

$$P_S = V_{CC} \times I_{CC} \quad (3)$$

Where:

V_{CC} = supply voltage
I_{CC} = current into a device (sum of leakage currents as in equation 2)

Another source of static current is ΔI_{CC}. This results when the input levels are not driven all the way to the rail, causing the input transistors to not switch off completely.

Dynamic Power Consumption

The dynamic power consumption of a CMOS IC is calculated by adding the transient power consumption (P_T), and capacitive-load power consumption (P_L).

Transient Power Consumption

Transient power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This is a result of the current required to charge the internal nodes (*switching current*) plus the *through current* (current that flows from V_{CC} to GND when the p-channel transistor and n-channel transistor turn on briefly at the same time during the logic transition). The frequency at which the device is switching, plus the rise and fall times of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible compared to the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the IC and the charge and discharge current of the load capacitance.

Transient power consumption can be calculated using equation 4.

$$P_T = C_{pd} \times V_{CC}^2 \times f_I \times N_{sw} \quad (4)$$

Where:

P_T = transient power consumption
V_{CC} = supply voltage
f_I = input signal frequency
N_{SW} = number of bits switching
C_{pd} = dynamic power-dissipation capacitance

In the case of single-bit switching, N_{SW} in equation 4 is 1.

Dynamic supply current is dominant in CMOS circuits because most of the power is consumed in moving charges in the parasitic capacitor in the CMOS gates. As a result, the simplified model of a CMOS circuit consisting of several gates can be viewed as one large capacitor that is charged and discharged between the power-supply rails. Therefore, the power–dissipation capacitance (C_{pd}) is often specified as a measure of this equivalent capacitance and is used to approximate the dynamic power consumption. C_{pd} is defined as the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance. Depending on the output switching capability, C_{pd} can be measured with no output switching (output disabled) or with any of the outputs switching (output enabled). C_{pd} is discussed in greater detail in the next section.

Capacitive-Load Power Consumption

Additional power is consumed in charging external load capacitance and is dependent on switching frequency. The following equation can be used to calculate this power if all outputs have the same load and are switching at the same output frequency.

$$P_L = C_L \times V_{CC}^2 \times f_O \times N_{sw} \ (C_L \text{ is the load per output}) \quad (5)$$

Where:

P_L = capacitive-load power consumption
V_{CC} = supply voltage
f_O = output signal frequency
C_L = external (load) capacitance
N_{SW} = total number of outputs switching

In the case of different loads and different output frequencies at all outputs, equation 6 is used to calculate capacitive-load power consumption.

$$P_L = \Sigma(C_{Ln} \times f_{On}) \times V_{CC}^2 \quad (6)$$

Where:

Σ = sum of n different frequencies and loads at n different outputs
f_{On} = all different output frequencies at each output, numbered 1 through n (Hz)
V_{CC} = supply voltage (V)
C_{Ln} = all different load capacitances at each output numbered 1 through n.

Therefore, dynamic power consumption (P_D) is the sum of these two power consumptions and can be expressed as shown in equation 7, equation 8 (single-bit switching), and equation 9 (multiple-bit switching with variable load and variable output frequencies).

$$P_D = P_T + P_L \tag{7}$$

$$P_D = \left(C_{pd} \times f_I \times V_{CC}^2\right) + \left(C_L \times f_O \times V_{CC}^2\right) \tag{8}$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma\left(C_{Ln} \times f_{On}\right)\right] \times V_{CC}^2 \tag{9}$$

Where:

C_{pd} = power-consumption capacitance (F)
f_I = input frequency (Hz)
f_{On} = all different output frequencies at each output, numbered 1 through n (Hz)
N_{SW} = total number of outputs switching
V_{CC} = supply voltage (V)
C_{Ln} = all different load capacitances at each output, numbered 1 through n.

Total power consumption is the sum of static and dynamic power consumption.

$$P_{tot} = P_{(static)} + P_{(dynamic)} \tag{10}$$

Power-Dissipation Capacitance (C_{pd}) in CMOS Circuits

C_{pd} is an important parameter in determining dynamic power consumption in CMOS circuits. It includes both internal parasitic capacitance (e.g., gate-to-source and gate-to-drain capacitance) and *through currents* present while a device is switching and both n-channel and p-channel transistors are momentarily conducting.

Testing Considerations

Proper setup is vital to achieving proper correlation. Some of the more important issues in performing the measurement are discussed in this section.

Input Edge Rates

When measuring C_{pd}, the input edge rate should be $t_r = t_f = 1$ ns from 10% to 90% of the input signal. Power-dissipation capacitance is heavily dependent on the dynamic supply current, which, in turn, is sensitive to input edge rates. As previously noted, while an input is switching, there is a brief period when both p-channel and n-channel transistors are conducting, which allows *through current* to flow from V_{CC} to GND through the input stage. The amount of dynamic *through current* measured is directly proportional to the amount of time the input signal is at some level other than V_{CC} or GND.

Bypassing

Any circuit must be properly bypassed to function correctly at high frequencies. The bypass capacitor between V_{CC} and GND serves to reduce power-supply ripple and provides a more accurate measure of the current being drawn by the device under test. Improper bypassing can result in erratic voltage at the V_{CC} pin and can disrupt the test. Texas Instruments (TI) uses a 0.1-μF bypass capacitor (from V_{CC} to GND) on the test board.

Pin Combination

Different pin combinations are valid and may be chosen to best suit the application at hand. For example, it is valid to test a device with the outputs either enabled or disabled. For multisection devices, set the device so that the minimum number of sections is active. Virtually any pin combination that causes at least one output to switch at a known frequency is acceptable.

Test Conditions

The test conditions for C_{pd} calculation for any device requires the following information (an LVC device is used as an example):

V_{CC}	5 V
Ambient temperature, T_A	25°C
AC bias levels	0 V, 3.3 V
DC bias level	0 V, 3.3 V
Input edge rates	$t_r = t_f = 1$ ns (smallest possible)
Input frequencies	0.1, 1, 2, 3, ...20, 25, 30, ...75 MHz
C_{pd} frequency	10 MHz
Duty Cycle	50%

Similarly, the test conditions for I_{CC} versus frequency are also applicable to determine the C_{pd} for CMOS devices. An AHC00 device is considered as an example for test conditions to calculate C_{pd} through I_{CC} versus frequency data and using the C_{pd} equation described in the next section (*Calculating C_{pd}*).

V_{CC}	5 V
Ambient temperature, T_A	25°C
AC bias levels	0 V, 5V
DC bias level	5 V
Input edge rates	$t_r = t_f = 2$ ns (smallest possible)
Input frequencies	0.1, 1, 2, 3, ...20, 25, 30, ...75 MHz
Duty Cycle	50%

For nontransceiver devices with 3-state outputs, testing is performed with the outputs enabled and disabled. When disabled, pullup resistors are not required. For a transceiver with 3-state outputs, testing is also performed with outputs enabled and disabled. However, in the disabled mode, 10-kΩ pullup resistors to the V_{CC} power supply or to GND must be added to all inputs and outputs.

Calculating C_{pd}

C_{pd} is calculated by putting the device in the proper state of operation and measuring the dynamic I_{CC} using a true RMS multimeter. Testing is done at an input frequency of 1 MHz to reduce the contribution of the dc supply current to the point that it can be ignored. Measurements for all devices are made at $V_{CC} = 5$ V or 3.3 V, $T_A = 25$°C. The test frequency must be low enough to allow the outputs to switch from rail to rail. For this reason, devices with 3-state outputs are measured at 10 MHz.

C_{pd} Measurement Procedures

For devices that have several gates in the same package (for example, AHC04 has six individual inverter circuits as shown in Figure 3), the total C_{pd} is specified in the data sheet.

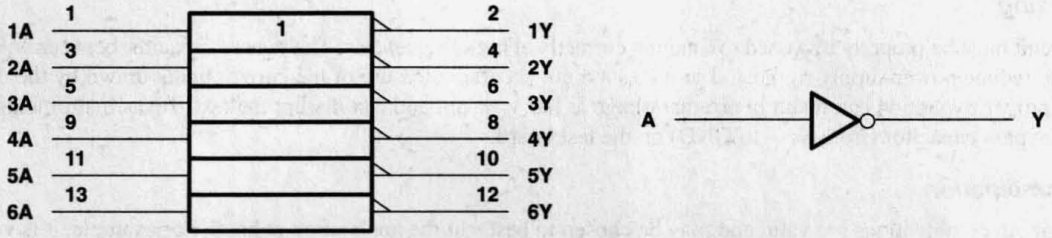


Figure 3. Hex Inverter AHC04

For devices that have several circuits switching simultaneously from a single clock or input (such as the AHC374 in Figure 4), switch all outputs and deduct P_L for each output. In the case of multiple-output switching at different frequencies (i.e., divide counters with parallel outputs) each P_L will have a different frequency factor.

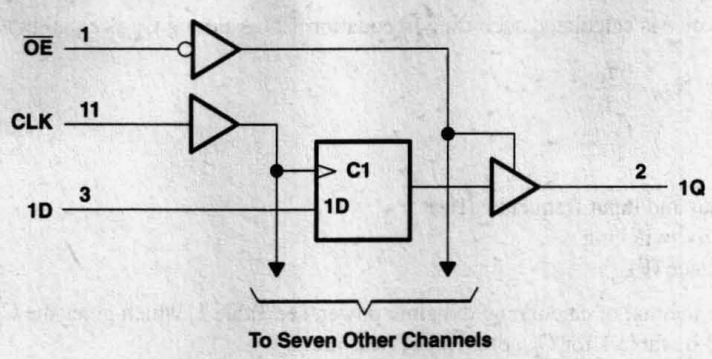


Figure 4. Several Circuits Switching, AHC374

In the case of devices such as ALVC, LVC, and LV, test and calculate C_{pd} for both the enable and disable mode. Typically, C_{pd} in the enable mode is greater than C_{pd} in the disable mode ($C_{pd_EN} > C_{pd_DIS}$).

Determination of C_{pd} (Laboratory Testing)

In the laboratory, determine C_{pd} for any device, such as AHC00, by measuring the I_{CC} being supplied to the device under the conditions in the *Test Conditions* section. Figure 5 provides the I_{CC} and frequency data for the AHC00 that can be used to calculate C_{pd} for the device, using equation 6 with a no-load condition.

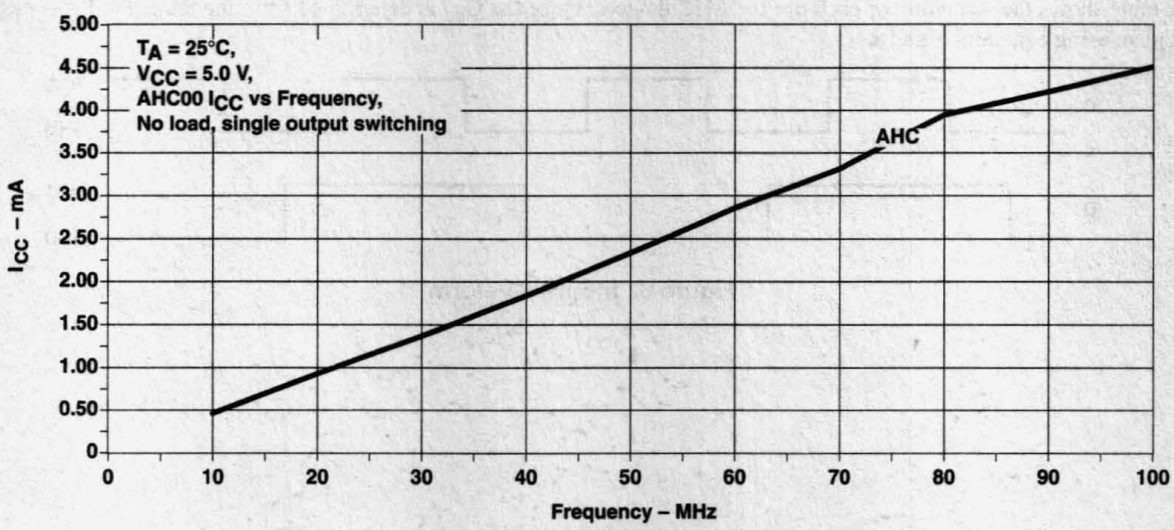


Figure 5. I_{CC} vs Frequency for AHC00

Note that the total capacitance for the switching output must be measured under open-socket conditions for accurate calculations. Considering these conditions, the data sheet C_{pd} is calculated using equation 11. Due to the automatic test equipment constraints, C_{pd} is not assigned a maximum value in the data sheet.

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_I} - C_{L(eff)} \quad (11)$$

Where:

f_I = input frequency (Hz)
V_{CC} = supply voltage (V)
$C_{L(eff)}$ = effective load capacitance on the board (F)
I_{CC} = measured value of current into the device (A)

The effective load capacitance is calculated according to equation 12 (assuming C_L is equal in all outputs).

$$C_{L(eff)} = C_L \times N_{SW} \times \frac{f_O}{f_I} \quad (12)$$

Where:

f_O/f_I = ratio of output and input frequency (Hz)
N_{SW} = number of bits switching
C_L = load capacitance (F)

To explain the C_{pd} and the method of calculating dynamic power, see Table 1, which gives the C_{pd} test conditions for AHC devices. The symbols used in Table 1 for C_{pd} of AHC devices are:

V = V_{CC} (5 V)
G = ground (GND) (0 V)
1 = high logic level = V_{CC} (5 V)
0 = low logic level = ground (0 V)
X = irrelevant: 1 or 0, but not switching
C = 50% duty cycle input pulse (1 MHz), (see Figure 6)
D = 50% duty cycle input (1/2 frequency) out-of-phase input pulse (see Figure 6)
S = standard ac output load (50 pF to GND)

The table shows the switching of each pin for AHC devices. Once the C_{pd} is determined from the table, the P_D is easy to calculate using equations 8 and 9.

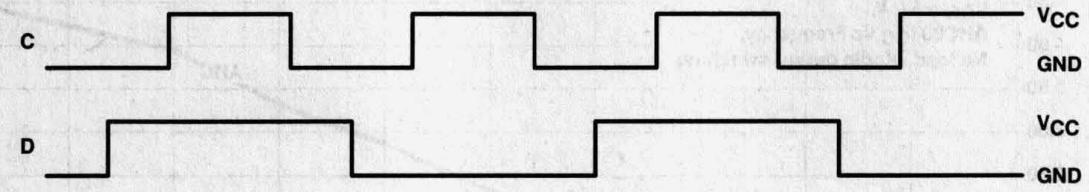


Figure 6. Input Waveform

Table 1. C_{pd} Test Conditions With One- or Multiple-Bit Switching

TYPE	PIN																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AHC00	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC02	S	C	0	S	X	X	G	X	X	S	X	X	S	V						
AHC04	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC08	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC10	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC11	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC14	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC32	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC74	1	D	C	1	S	S	G	S	S	X	X	X	1	V						
AHC86	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC138	C	0	0	0	0	1	S	G	S	S	S	S	S	S	S	V				
AHC139	0	C	0	S	S	S	S	G	S	S	S	S	X	X	X	V				
AHC240	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC244	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC245	1	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC373†	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC374‡	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC540	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC541	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC573†	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V
AHC574‡	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V

† All bits switchings, but with no active clock signal
‡ All bits switching

Comparison of Supply Current Versus Frequency

C_{pd} and dynamic power consumption can be measured through supply-current-versus-frequency plots. Supply current is critical because it indicates the amount of power consumed by the device. A small value for I_{CC} is desirable because reducing the amount of power consumed yields many benefits. Less power consumed means less heat is generated and the problems of dissipating the heat are reduced. The reliability of a system is also improved, because lower stress gradients are present on the device and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. Figures 7 and 8 illustrate I_{CC} versus frequency data for TI's '245 device in different families for both 5 V and 3.3 V.

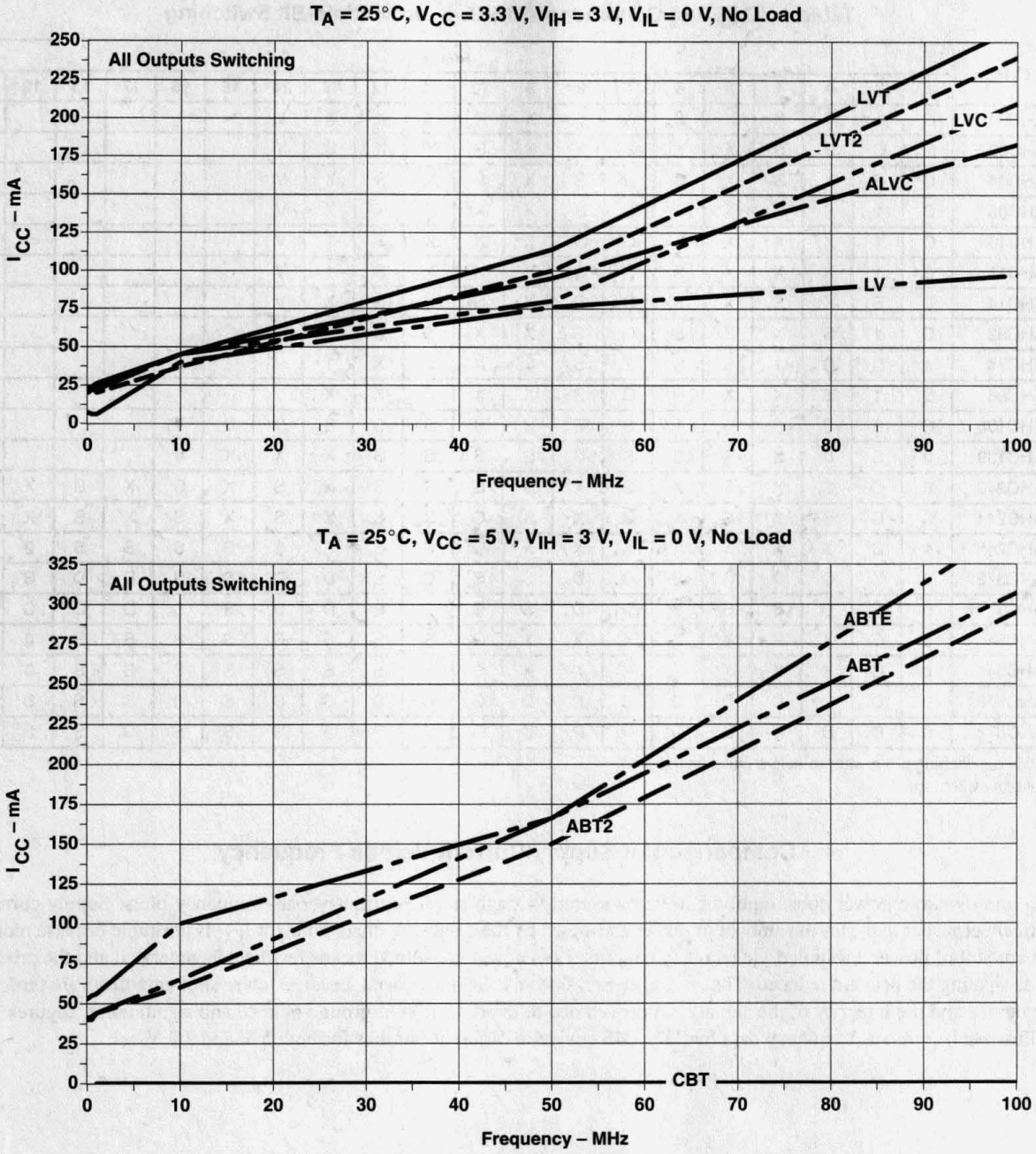


Figure 7. Power Consumption With All Outputs Switching

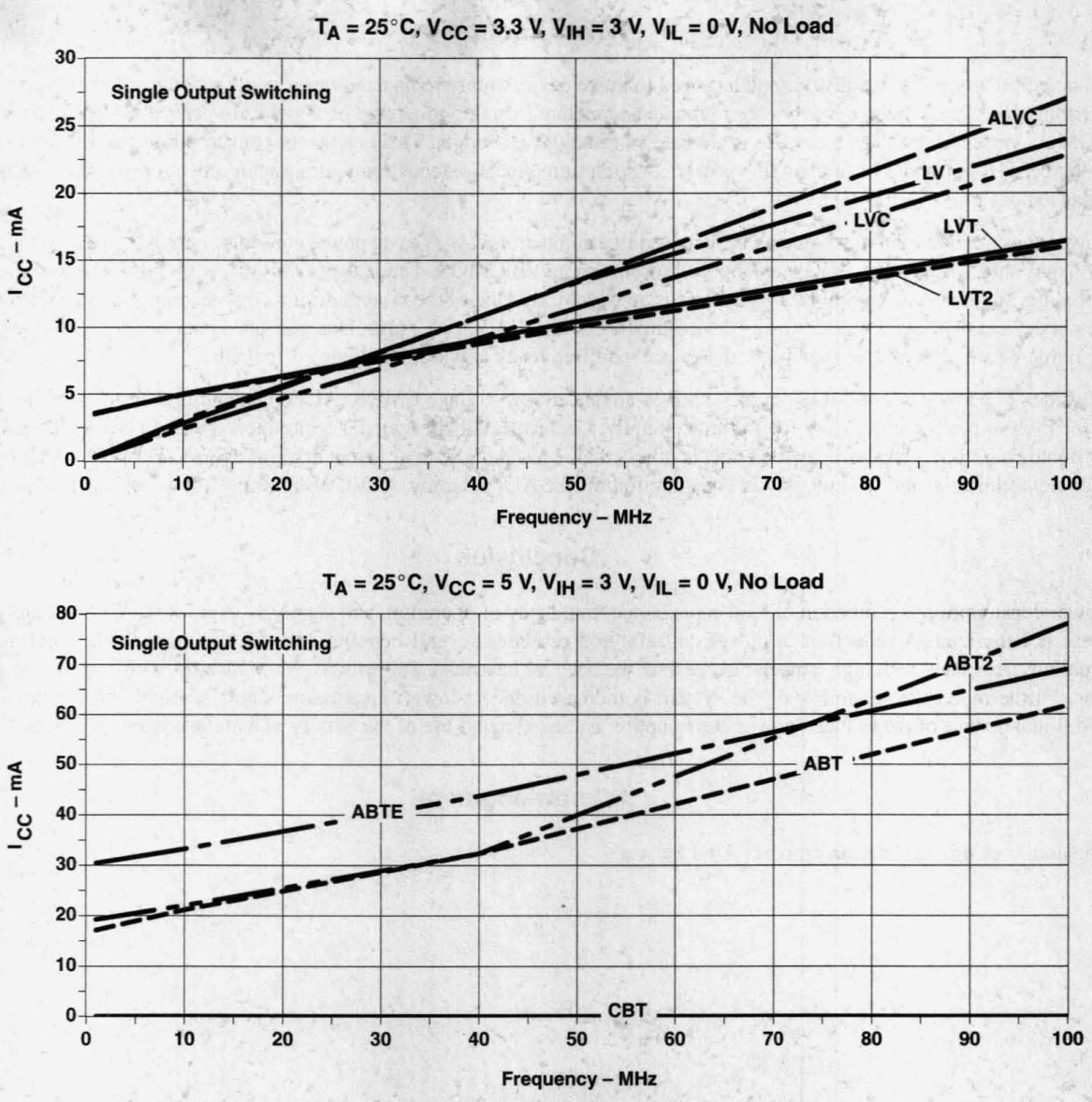


Figure 8. Power Consumption With a Single Output Switching

Power Economy

As noted previously, the industry trend has been to make devices more robust and faster while reducing their size and power consumption. This section describes the rationale and methods used to minimize power consumption in a CMOS circuit. For a CMOS system design, each module is allocated a fixed power budget. This is a power consumption that the module must not exceed. It is important to meet this power consumption allocation constraint, along with other constraints, to achieve a balanced design.

Power consumption minimization may be achieved in a number of ways. The dc power consumption can be reduced to leakage by using only CMOS logic gates, as opposed to bipolar and BiCMOS. The leakage, in turn, is proportional to the area of diffusion, so the use of minimum-size devices is an advantage. One of the system design considerations is the choice of low power devices, with systems today using devices in the 1.5-V to 3.3-V V_{CC} range. Dynamic power consumption may be limited by reducing supply voltage, switched capacitance, and frequency at which the logic is clocked.

Consider TI's low-power CMOS devices, such as advanced low-voltage CMOS (ALVC) technology as an example. ALVC is the highest performance 3.3-V bus-interface family. These specially designed 3-V products are processed in 0.6-μ CMOS technology, giving typical propagation delays of less than 3 ns, along with a current drive of 24 mA. This low supply voltage reduces both static and dynamic power consumption for the ALVC family. ALVC also has ultra-low standby power.

Conclusion

Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heatsinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower temperature-stress gradients on the device. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

Acknowledgment

The author of this application report is Abul Sarwar.

General Design Considerations 1
Backplane Design 2
Device-Specific Design Aspects 3
5-V Logic Design 4
3.3-V Logic Design 5
Clock-Distribution Circuits (CDC) 6
Boundary-Scan IEEE Std 1149.1 (JTAG) Logic 7
Packaging 8
Index 9

Contents

	Page
Application and Design Considerations for the CDC5XX Platform of Phase-Lock Loop Clock Drivers	6–3
Clock Distribution in High-Performance PCs	6–23
EMI Prevention in Clock-Distribution Circuits	6–33
Minimizing Output Skew Using Ganged Outputs	6–49
Phase-Lock Loop-Based (PLL) Clock Driver: A Critical Look at Benefits Versus Costs	6–59

Application and Design Considerations for the CDC5XX Platform of Phase-Lock Loop Clock Drivers

SCAA028
April 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title *Page*

Introduction **6–7**

Definitions **6–7**
Output Skew 6–7
Process Skew 6–7
Limit Skew 6–7
Jitter 6–7

Features and Functional Description **6–8**
Features 6–8
Functional Description 6–10

Design Considerations **6–11**
Configuring the CDC586, CDC2586, CDC582, and CDC2582 6–11
Zero-Propagation-Delay Operation 6–14
Jitter 6–16
Driver Output Impedance 6–18

Power Supply and Decoupling Considerations **6–21**

Acknowledgment **6–21**

References **6–21**

List of Illustrations

Figure *Title* *Page*

1 CDC586 Functional Block Diagram 6–10
2 CDC586 1× Configuration 6–11
3 CDC586 1/2× Configuration 6–12
4 CDC586 2× Configuration 6–13
5 Zero-Propagation-Delay Application 6–14
6 CDC586 and CDC2586 Typical Phase Error 6–15
7 Jitter Measurement Methodology and Test Setup 6–16
8 CDC586 Typical Jitter Performance 6–17
9 Series Termination Examples 6–18
10 CDC586 Transmission-Line Analysis 6–19
11 CDC586 and CDC2586 Typical V/I Curves 6–20
12 Analog Power Filter 6–21

List of Tables

Table	*Title*	*Page*
1	Device Features	6–9
2	Device Configuration	6–11

Introduction

Today's high-speed system designs require stringent propagation and skew parameters. With system clock frequencies exceeding 50 MHz, the designer must consider clock skews to maintain desired system performance. Clock skew reduces the usable amount of time in each clock cycle and can force designers to ensure restrictive setup- and hold-time requirements for clocked components.

To meet the designer's need for high-performance clock system components, Texas Instruments (TI) has developed the CDC5XX platform of phase-lock loop (PLL) clock drivers. These clock drivers operate at 3.3-V V_{CC} and offer excellent performance with respect to skew and jitter. The CDC5XX platform of PLL products includes the CDC586, CDC2586, CDC582, CDC2582, CDC536, and CDC2536.

The CDC586 provides a TTL-compatible clock input and 12 LVTTL-compatible outputs, while the CDC582 provides a differential low-voltage pseudo-ECL (LVPECL) clock input and 12 TTL-compatible outputs. The CDC2586 and CDC2582 provide the same functions as the CDC586 and CDC582, respectively, but also include internal series-damping resistors to improve signal integrity without increasing component count for applications that require series termination. The CDC536 is a scaled version of the CDC586, providing TTL-compatible inputs and six LVTTL-compatible outputs. The CDC2536 is the series-damped version of the CDC536.

This application report details the functions and features of the CDC5XX platform of PLL clock drivers. Topics such as device configuration, board layout, and other design considerations are discussed to aid the clock distribution network designer.

Definitions

Output Skew

Output skew, $t_{sk(o)}$, is the difference between two concurrent propagation delay times that originate from a single input, or multiple inputs switching simultaneously and terminating at different outputs.

This parameter is useful when considering the distribution of a clock signal to multiple targets.

Process Skew

Process skew, $t_{sk(pr)}$, is the difference between identically specified propagation delay times on any two samples of an integrated circuit at identical operating conditions.

This parameter quantifies the skew-induced variations in the integrated circuit (IC) manufacturing process, but not by variations in supply voltage, ambient temperature, output loading, input frequency and edge rate, etc.

Limit Skew

Limit skew, $t_{sk(l)}$, is the difference between the greater of the maximum specified propagation delay times, t_{PLH} and t_{PHL}, and the lesser of the minimum specified propagation delay times, t_{PLH} and t_{PHL}.

Limit skew is not directly observable on a device, but, rather, it is a calculated value from the data sheet limits of t_{PLH} and t_{PHL}. This parameter quantifies the variation in propagation delay times over the entire range of supply voltages, ambient temperature, output loading, and all other specified operating conditions, such as input frequency, input duty cycle, and edge rates. All other device skew specifications, $t_{sk(o)}$, $t_{sk(p)}$, and $t_{sk(pr)}$, are subsets of the limit skew, and therefore are never greater than $t_{sk}(l)$.

Jitter

Cycle-to-Cycle Jitter

Cycle-to-cycle jitter is the difference in the period of successive cycles of a continuous clock pulse.

Peak-to-Peak Jitter

Peak-to-peak jitter, sometimes referred to as period or long-term jitter, is the absolute maximum difference in the periods of any two cycles of a continuous clock pulse. Peak-to-peak jitter defines an upper bound on the cycle-to-cycle jitter.

RMS Jitter

RMS jitter is a statistical method of measuring device jitter performance. It is calculated as the standard deviation of a large sample set of period measurements. If a PLL exhibits a Gaussian distribution with respect to jitter, the peak-to-peak jitter can be calculated as six times the RMS jitter.

Features and Functional Description

Features

The CDC5XX platform of PLL clock drivers provides the designer with many key features and ease of use. All of the 3.3-V PLL CDCs share a common set of core features, such as:

- 3.3-V supply operation
- On-chip loop filter
- External feedback
- Distributed V_{CC} and GND pins to reduce switching noise
- 1×, 1/2×, or 2× configurable outputs
- Low-phase-error, output-skew, and jitter specifications

In addition, a variety of device-specific features provides the designer with choice and flexibility. Some of these features are:

- LVTTL or LVPECL inputs
- On-chip series-damping resistors
- Six or 12 outputs

The key features of the CDC5XX platform of PLL clock drivers are summarized in Table 1.

The core features provide many benefits to the designer. Low-phase-error, output-skew, and jitter specifications ensure reliable clock distribution, even when using multiple devices. The on-chip loop filter allows for easy implementation of the PLL and reduces overall component count necessary for traditional PLLs. The external feedback provides many options to the designer. While the feedback may be implemented directly from an output of the PLL, it can be selected from any point within the system to zero the propagation delay from the clock to that point. In addition, the external feedback, coupled with the two select inputs, provides for a variety of output configurations. Although the bank of outputs from which the feedback is derived is always at the same frequency as the input clock, the other outputs can be configured to provide either 1/2× or 2× frequency outputs. In addition, the design of these PLLs ensures an output duty cycle of 50% ± 5% regardless of input duty cycle, which can be critical for many of today's high-speed microprocessor systems.

Table 1. Device Features

DEVICE	FEATURES
CDC586 (CDC2586)	3.3-V supply operation On-chip loop filter External feedback Up to nine outputs configurable as 1/2× or 2× TTL-compatible inputs Twelve LVTTL-compatible outputs On-chip series-damping resistor option (CDC2586) Maximum phase error of ±500 ps (any output to CLKIN) Maximum outputs skew of 500 ps Maximum process skew of 1 ns Maximum jitter of 200 ps (peak to peak)
CDC582 (CDC2582)	3.3-V supply operation On-chip loop filter External feedback Up to nine outputs configurable as 1/2× or 2× LVPECL compatible clock inputs TTL-compatible control inputs Twelve LVTTL-compatible outputs On-chip series-damping resistors option (CDC2582) Maximum phase error of ±500 ps (any output to CLKIN) Maximum outputs skew of 500 ps Maximum process skew of 1 ns Maximum jitter of 200 ps (peak-to-peak)
CDC536 (CDC2536)	3.3-V supply operation On-chip loop filter External feedback Three outputs configurable as 1/2× or 2× TTL-compatible inputs 12 LVTTL-compatible outputs On-chip series damping-resistors option (CDC2536) Maximum phase error of ±500 ps (any output to CLKIN) Maximum outputs skew of 500 ps Maximum process skew of 1 ns Maximum jitter of 200 ps (peak-to-peak)

Functional Description

A functional block diagram of the CDC586 is shown in Figure 1. An integrated PLL synchronizes the feedback input with the input reference clock. The synchronized clock is distributed externally via four banks of three output buffers.

The voltage-controlled oscillator (VCO) operates at either two or four times the frequency of the reference input. This is determined by the output chosen for use as feedback and the configuration of the select inputs, i.e., SEL(0:1). Output banks 1Y(1:3), 2Y(1:3), and 3Y(1:3) can be configured to distribute either one-half or one-quarter the VCO operating frequency, while output bank 4Y(1:3) is fixed to operate at one-half the VCO operating frequency. The output that is used for feedback is forced to operate at the same frequency as the reference input. This also means that all other outputs in that bank are at the same frequency as the input reference clock, i.e., 1×. It is important that the VCO is operating within the specified stable frequency range (i.e., a VCO frequency of 100 MHz to 200 MHz) to ensure device performance. This topic is discussed in greater detail in the next section.

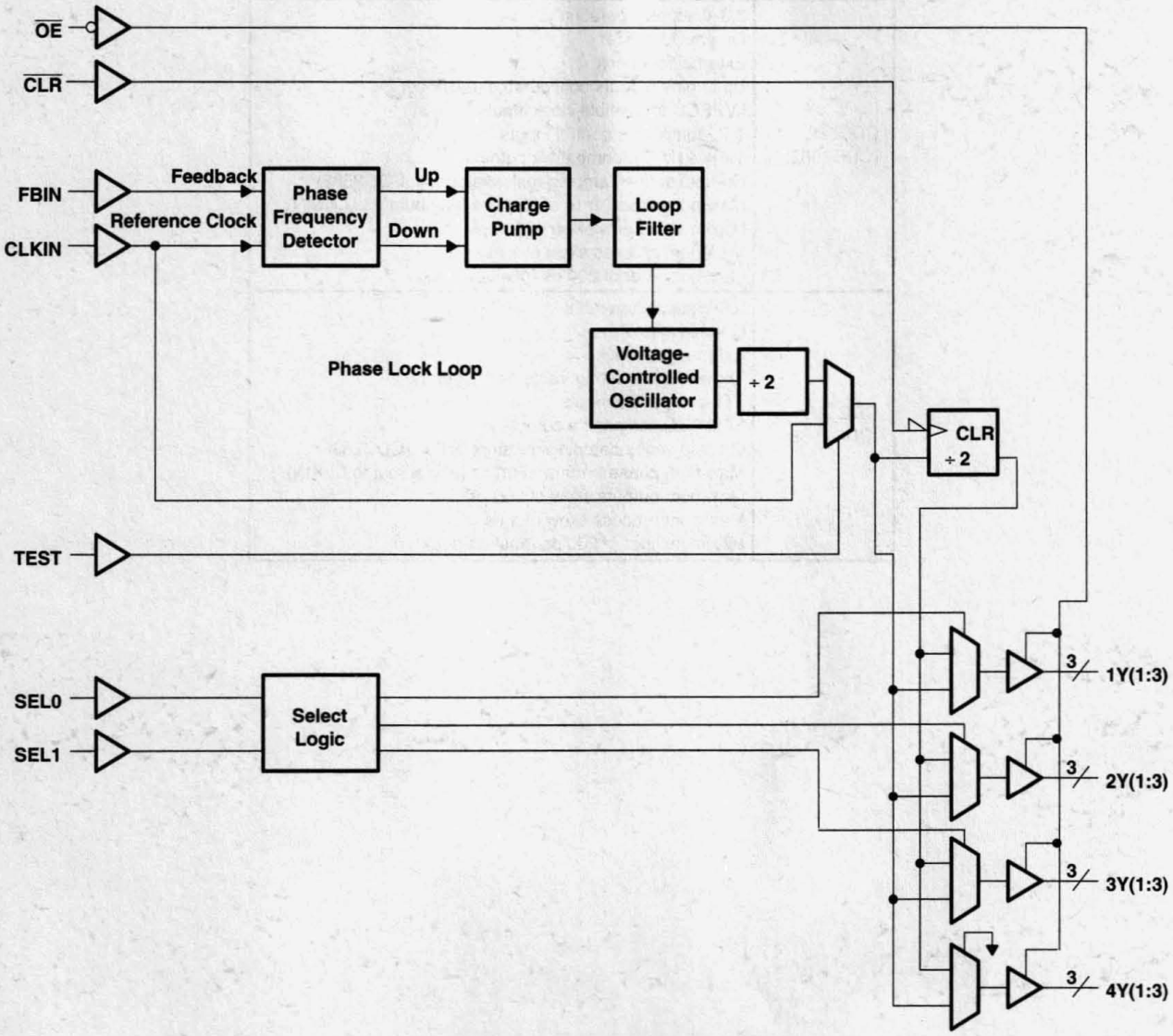


Figure 1. CDC586 Functional Block Diagram

Design Considerations

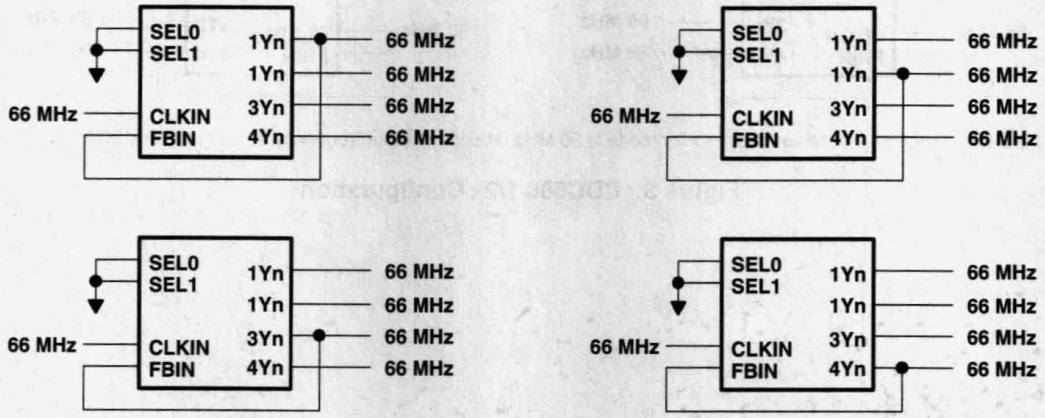
Configuring the CDC586, CDC2586, CDC582, and CDC2582

The CDC586 can be configured to provide several different output frequency relationships. All device outputs may be configured for 1× operation, and up to nine outputs may be configured for 1/2× or 2× operation. The output configuration is dependent upon the state of the SEL(0:1) inputs and the output used as the feedback.

Table 2 shows the possible output frequency relationships referenced to the VCO operating frequency. The output bank, which is used for feedback, switches at the same frequency as the input clock, which is one-half or one-fourth the frequency of the VCO as shown in Table 2. When using a VCO/2 output for feedback, the outputs can be configured to switch at the same frequency or one-half the frequency of the clock input; when using a VCO/4 output for feedback, the outputs can be configured to switch at the same frequency or twice the frequency of the clock input. Examples of all possible output configurations are shown in Figures 2 through 4.

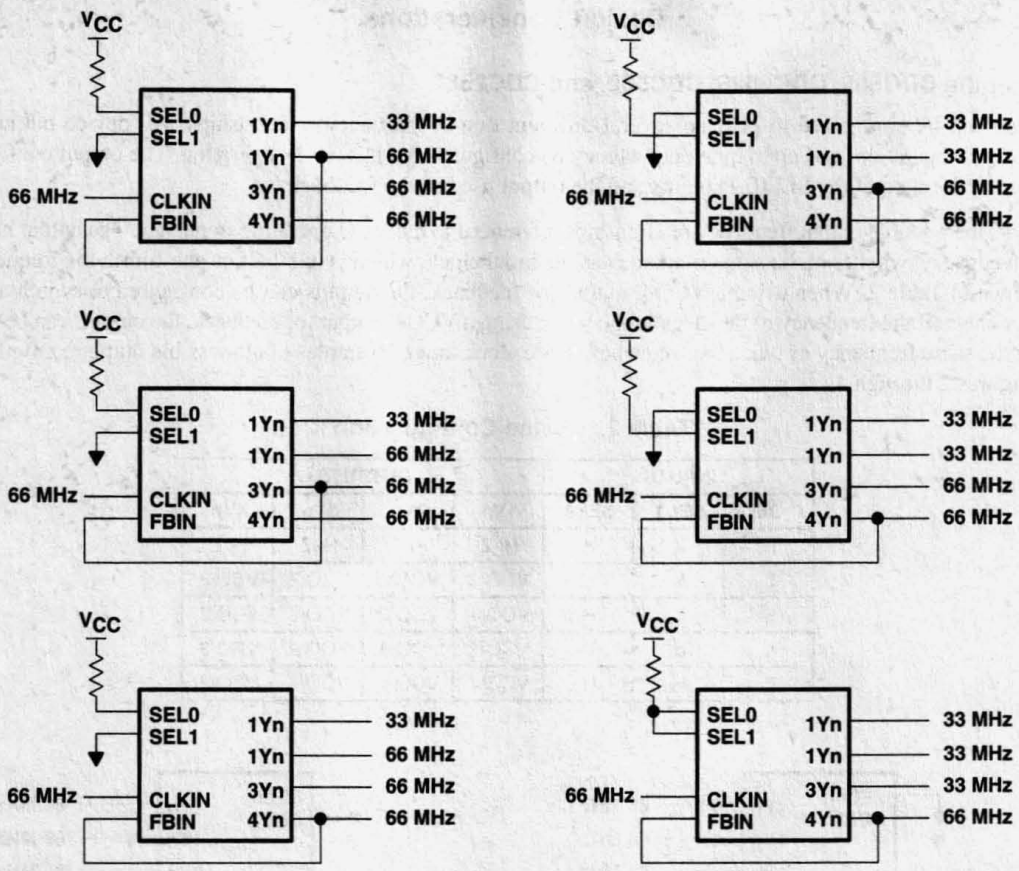
Table 2. Device Configuration

INPUTS			OUTPUTS			
$\overline{OE}$	SEL1	SEL0	1Yn	2Yn	3Yn	4Yn
H	X	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z
L	L	L	VCO/2	VCO/2	VCO/2	VCO/2
L	L	H	VCO/4	VCO/2	VCO/2	VCO/2
L	H	L	VCO/4	VCO/4	VCO/2	VCO/2
L	H	H	VCO/4	VCO/4	VCO/4	VCO/2



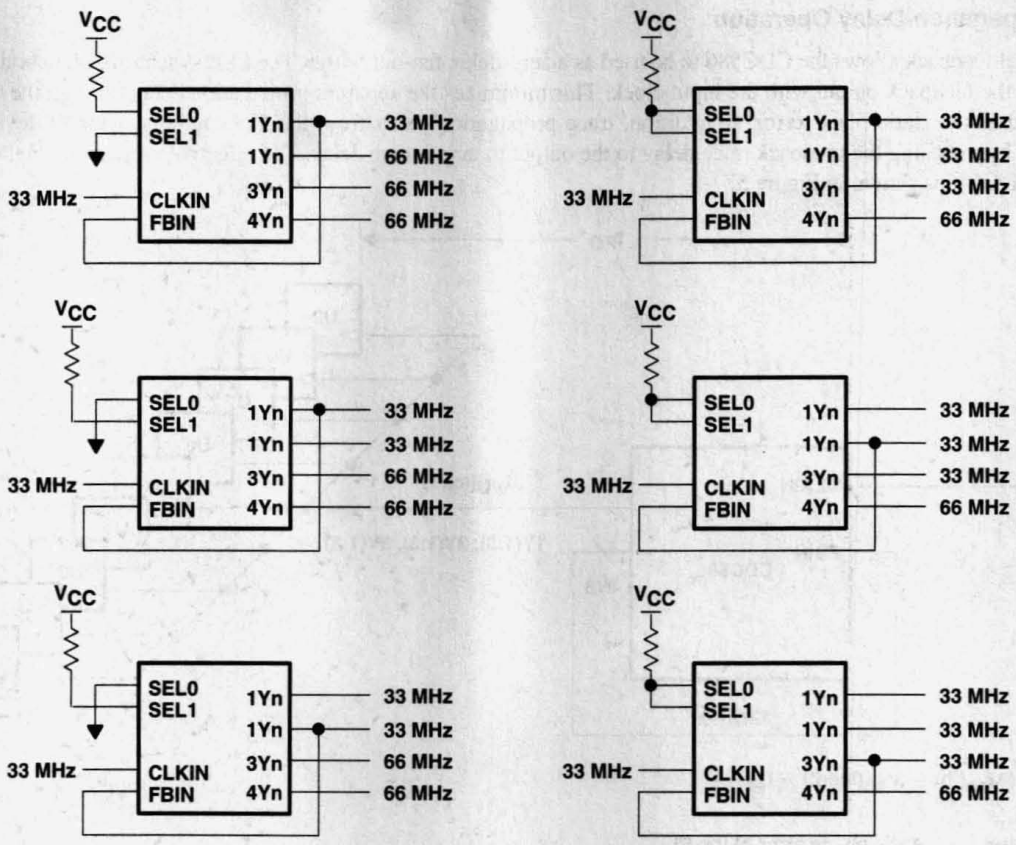
NOTE: Minimum input frequency in 1× mode is 50 MHz. Maximum input frequency in 1× mode is100 MHz.

Figure 2. CDC586 1× Configuration



NOTE: Minimum input frequency in 1/2× mode is 50 MHz. Maximum input frequency in 1/2× mode is100 MHz.

Figure 3. CDC586 1/2× Configuration



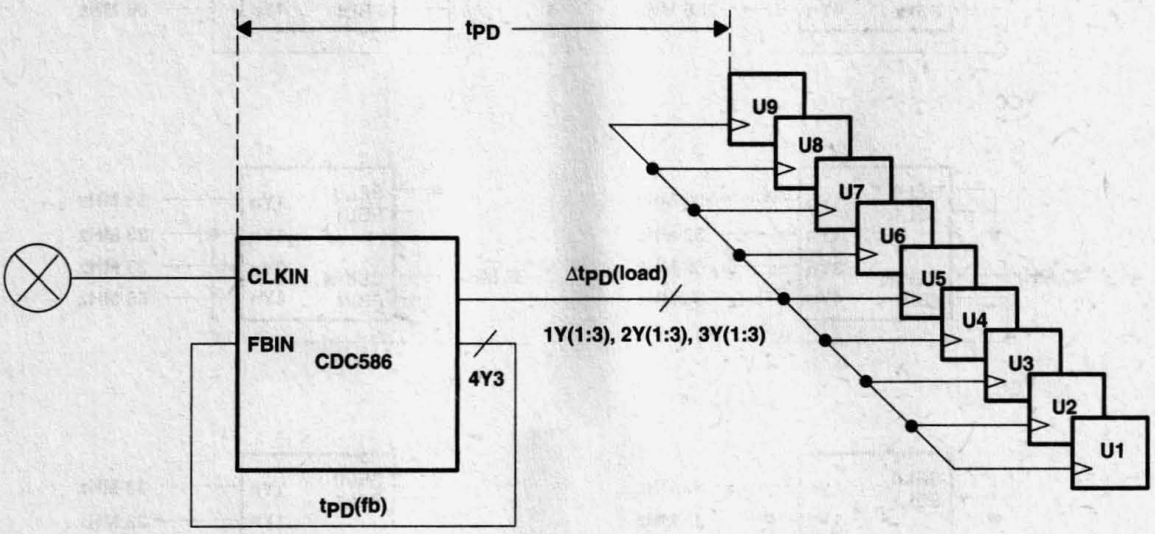
NOTE: Minimum input frequency in 2× mode is 25 MHz. Maximum input frequency in 2× mode is 50 MHz.

Figure 4. CDC586 2× Configuration

When using the CDC586, the designer must ensure that the VCO is operating within its recommended frequency range. Stable operation of the PLL is guaranteed within the specified operating frequencies. Degraded performance, such as higher jitter, can be observed when operating outside the specified operating frequencies. The CDC586 VCO is designed for optimal operation within the frequency range of 100 MHz to 200 MHz. This implies that when operating with a feedback output configured for VCO/2, the input frequency range is 50 MHz to 100 MHz; when operating with a feedback output configured for VCO/4, the input frequency range is 25 MHz to 50 MHz.

Zero-Propagation-Delay Operation

The external feedback allows the CDC586 to be used as a zero-delay fan-out buffer. The PLL synchronizes, in both phase and frequency, the feedback output with the input clock. This minimizes the apparent propagation delay through the device, and is specified as the static phase error. In addition, trace propagation delay from the PLL outputs to target devices can be eliminated by matching the feedback trace delay to the output to target trace delay. The effective propagation delay of a PLL with the CDC586 is shown in Figure 5.



$t_{PD} = [\Delta t_{PD}(fb) - \Delta t_{PD}(load)] + t_{PE}$

Where:

t_{PE} = **static phase error of the PLL**

Figure 5. Zero-Propagation-Delay Application

The static phase error of the CDC586 is specified at ±500 ps across the recommended temperature and supply voltage operating conditions. Typical static phase offset for the CDC586 and CDC2586 from characterization is shown in Figure 6.

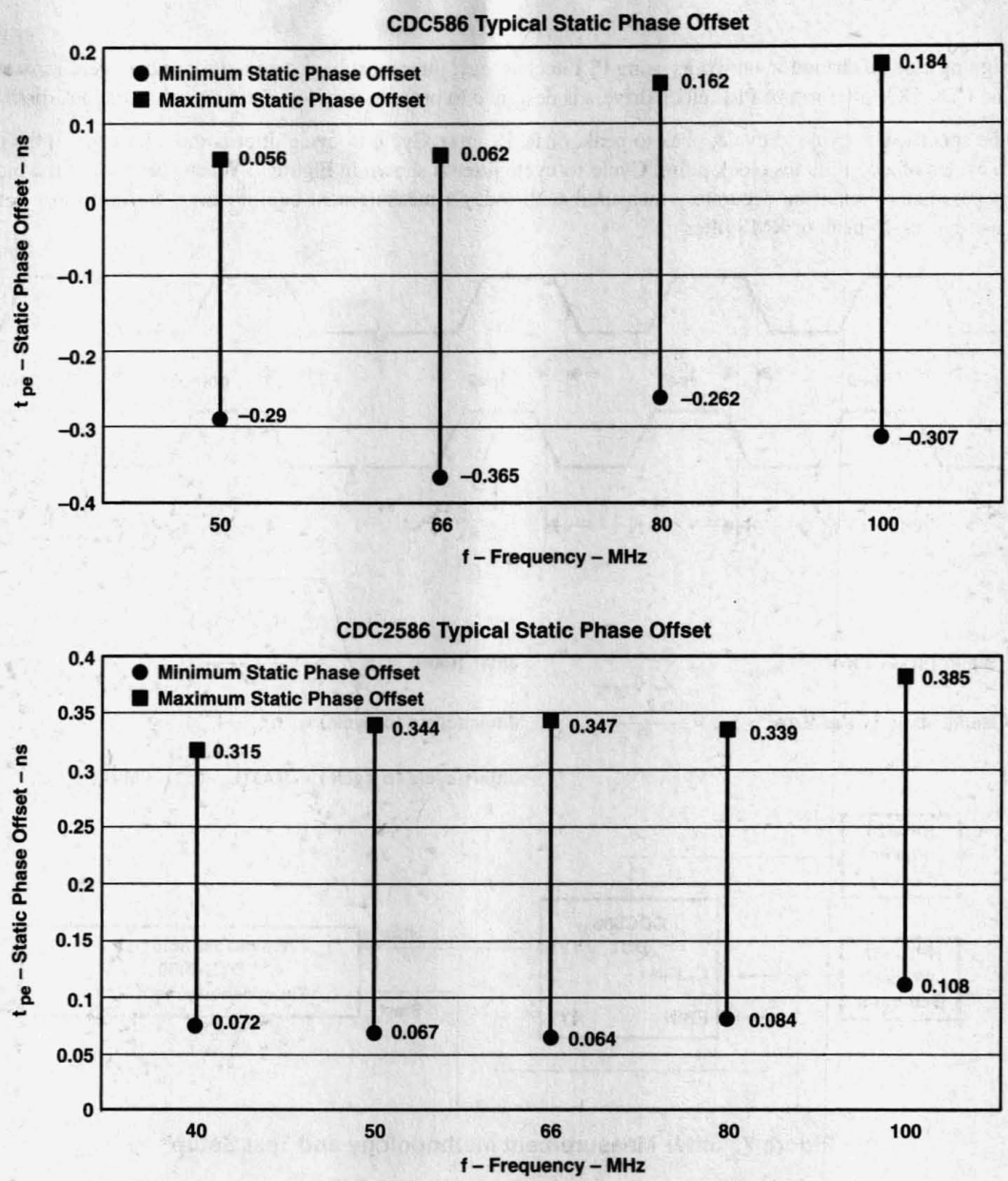


Figure 6. CDC586 and CDC2586 Typical Phase Error

The skew between multiple devices with a common clock input is the difference between the maximum and minimum phase error of the devices. Therefore, regardless of device operating conditions, the absolute maximum skew (i.e., limit skew) across multiple devices is 1 ns, plus 200-ps jitter.

Jitter

When designing clock distribution networks using PLL technology, jitter must be accounted for in the overall system timing budget. The CDC5XX platform of PLL clock drivers is designed to provide very low jitter for reliable clock distribution.

Jitter can be specified as cycle to cycle, peak to peak, or RMS jitter. Cycle-to-cycle jitter is the difference in the period of successive cycles of a continuous clock pulse. Cycle-to-cycle jitter is shown in Figure 7. When specified in the picosecond range, this parameter cannot be accurately measured with today's measurement equipment; therefore, most devices are specified using peak-to-peak or RMS jitter.

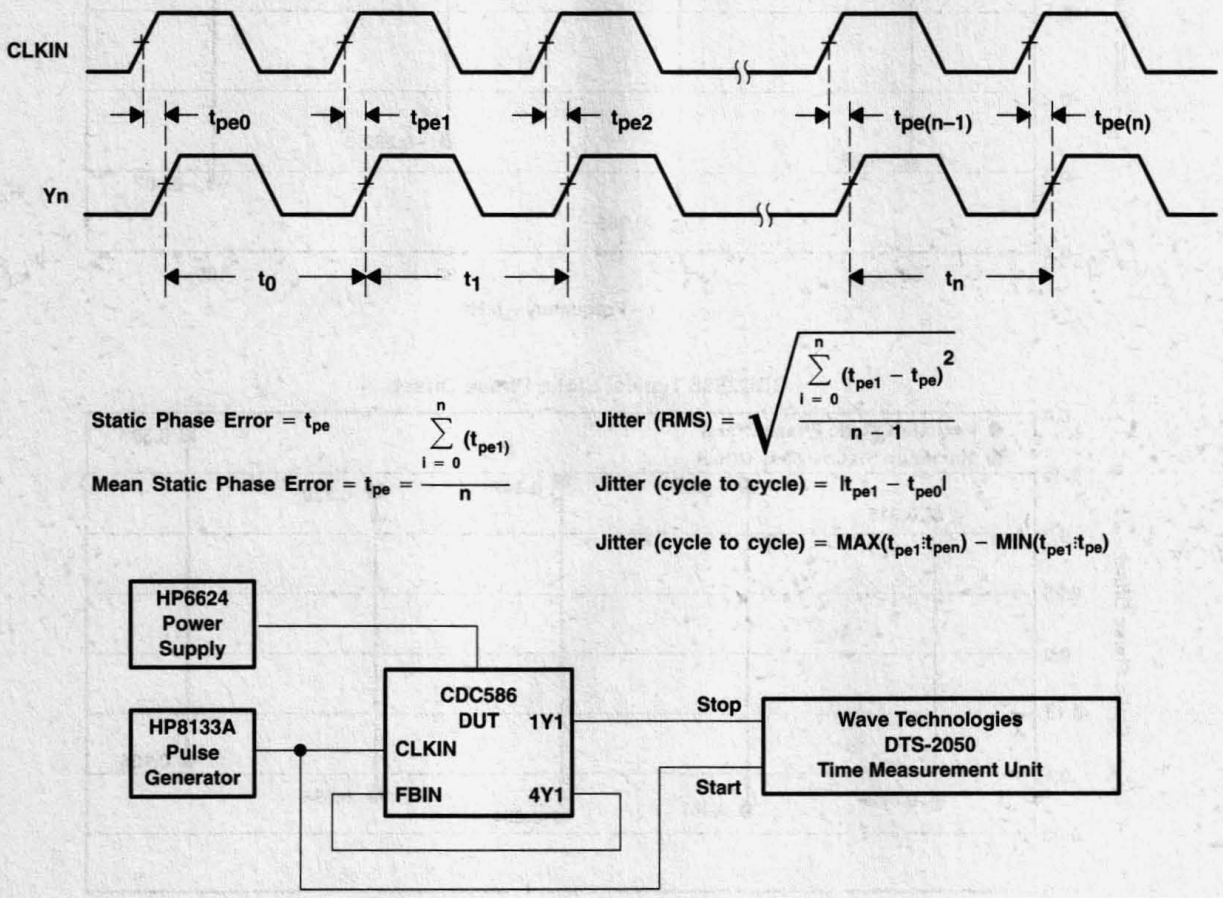


Figure 7. Jitter Measurement Methodology and Test Setup

Peak-to-peak jitter, sometimes referred to as period or long-term jitter, is the absolute maximum difference in the periods of any two cycles of a continuous clock pulse. The peak-to-peak jitter defines an upper bound on the cycle-to-cycle jitter; however, due to the nature of the PLL, it is unlikely that the maximum variation in the output period occurs between consecutive cycles.

RMS jitter is a statistical method of measuring device jitter performance. It can be calculated as the standard deviation of a large sample set of period measurements. If a PLL exhibits a Gaussian distribution with respect to jitter, the peak-to-peak jitter is computed as six times the RMS jitter.

The RMS jitter can be determined by measuring the phase of the output with respect to a stable reference signal, typically the input reference clock generated from a very low jitter source, and calculating the standard deviation of the distribution. Jitter for the CDC586 platform of devices was characterized using this method. The test setup is shown in Figure 7.

When measuring jitter using this method, a very low jitter-pulse generator must be used so that its contribution to the measurement is negligible. The HP8133A provides an output signal with 1-ps to 1.5-ps RMS jitter, which is about 10 times lower than the measured jitter of the device under test (DUT), and can be ignored.

Figure 8 shows typical jitter performance of the CDC586. The data is presented as RMS jitter. As shown, better performance is achieved with a supply voltage greater than 3.3 V. VCO operating frequency also has an effect on the jitter performance, with lower jitter typically corresponding to higher VCO operating frequencies.

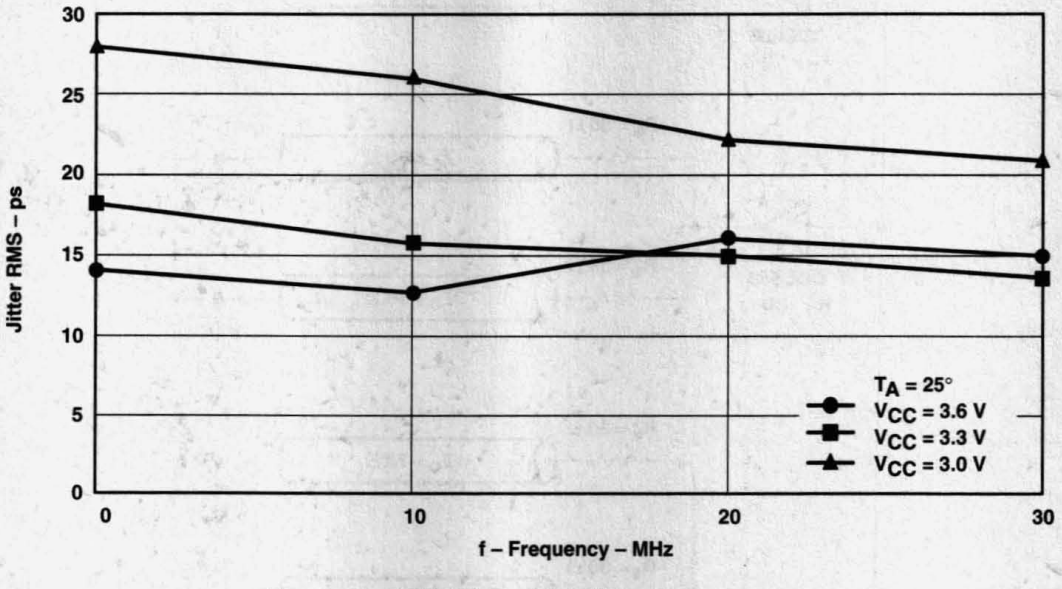


Figure 8. CDC586 Typical Jitter Performance

Driver Output Impedance

The CDC586, CDC582 and CDC536 were designed with high-drive, low-impedance output drivers. Typical output impedance of the CDC5XX devices is 10 Ω. This provides sufficient driver strength to drive properly terminated 50-Ω parallel transmission lines.

For point-to-point clock-distribution applications, series termination is recommended. Series termination provides excellent signal integrity without the additional dc current consumption required for parallel termination. Several examples of series termination are shown in Figure 9.

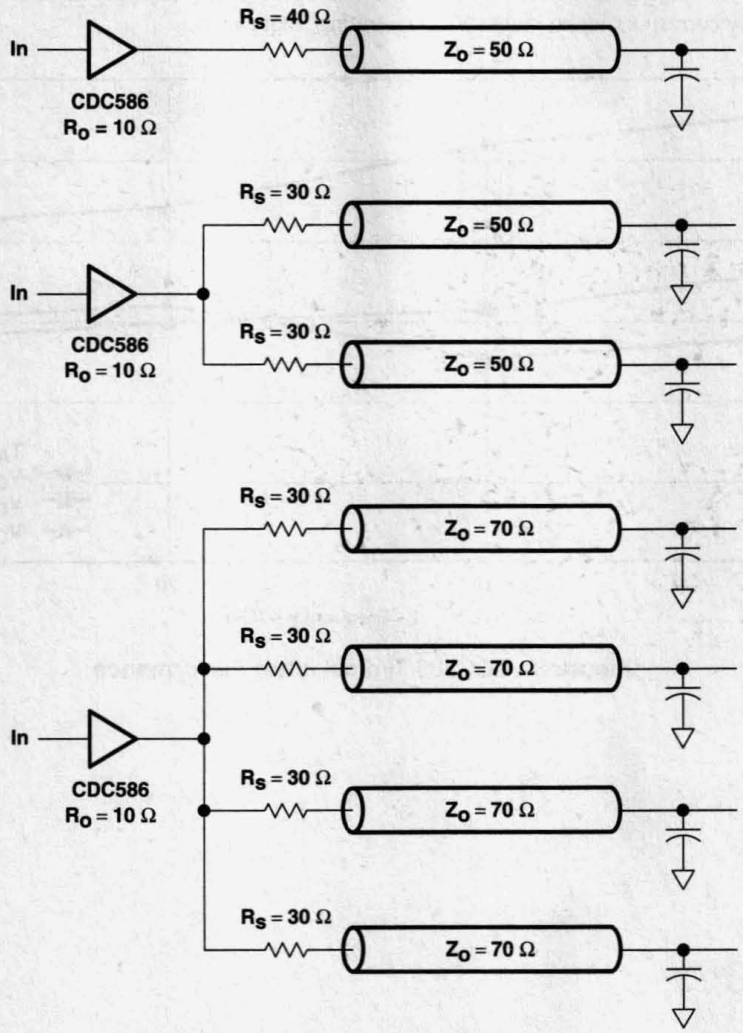


Figure 9. Series Termination Examples

Figure 10 shows the simulation results of a CDC586 output buffer driving a single series-terminated 50-Ω transmission line, a CDC586 output buffer driving two series-terminated 50-Ω transmission lines in parallel, and a CDC586 output buffer driving four series-terminated 70-Ω transmission lines in parallel. For the point-to-point example, the series resistor, R_S, can be determined by $Z_O = R_O + R_S$, where Z_O is the characteristic impedance of the transmission line and R_O is the output impedance of the driving buffer. For the case where multiple lines are driven, the series resistor can be determined by $Z_{(eff)} = R_O + R_{S(eff)}$, where $Z_{(eff)}$ is the parallel combination of the characteristic impedance of the transmission lines and $R_{S(eff)}$ is the parallel combination of the series resistors, R_S.

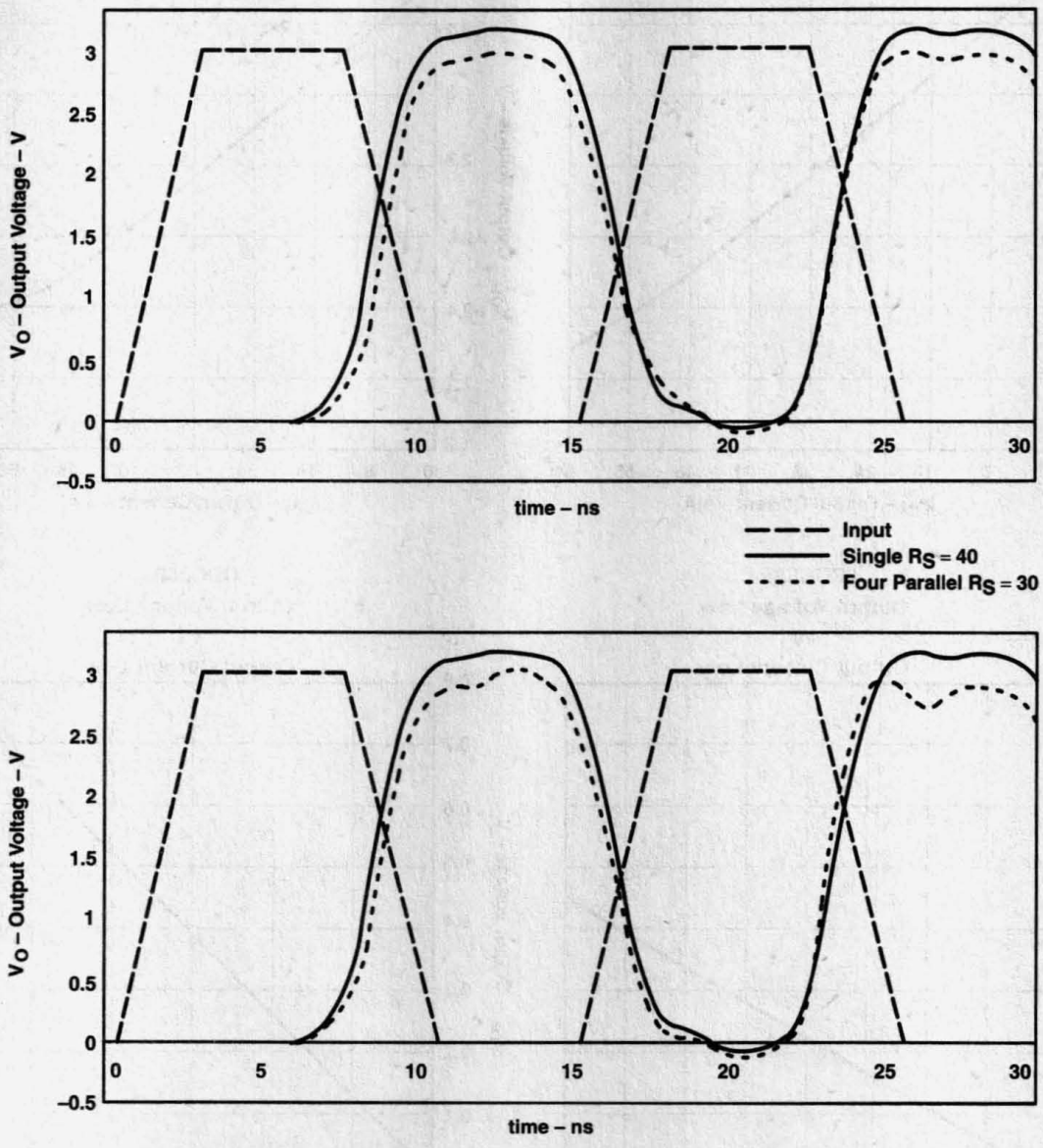


Figure 10. CDC586 Transmission-Line Analysis

The typical output impedance of the CDC25XX devices is 40 Ω. In many point-to-point clock-distribution applications, the CDC25XX devices will provide sufficient damping of reflected waveforms to meet the desired signal integrity without the need for an external series resistor. However, the system designer should evaluate signal integrity through the use of simulation, such as SPICE. TI provides input and output buffer HSPICE models for CDC devices, on customer request.

Typical V/I characteristics for both the CDC5XX and CDC25XX are shown in Figure 11.

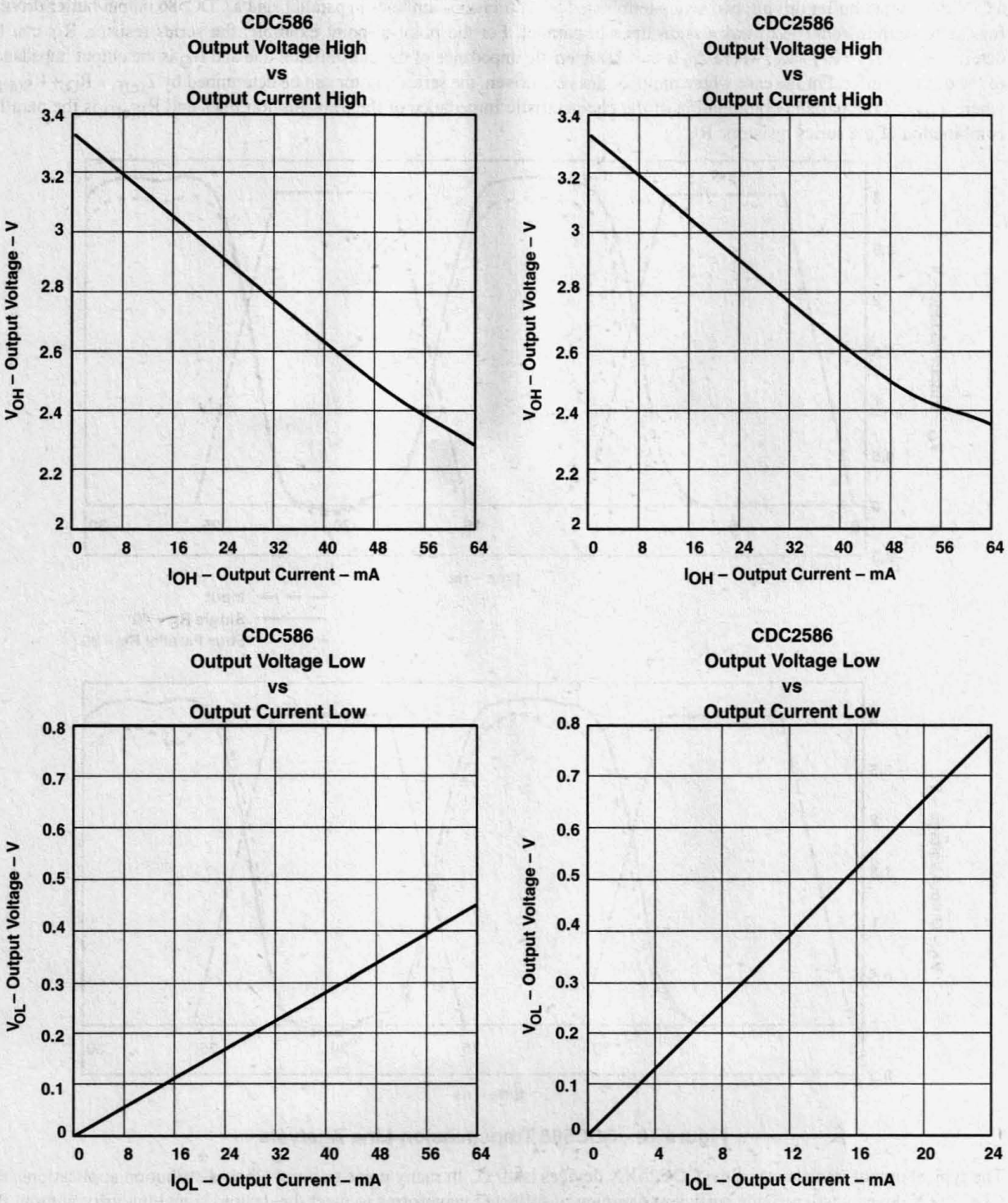


Figure 11. CDC586 and CDC2586 Typical V/I Curves

Power Supply and Decoupling Considerations

The CDC586 platform of clock drivers uses an integrated analog PLL to synchronize the outputs with the input reference clock. The performance of the analog portion of the circuit (i.e., the PLL) can be sensitive to noise on the supply voltage. Noise on the supply voltage can dramatically increase the jitter of the PLL. Since jitter must be accounted for in the overall system skew budget, this increase in jitter can cause system stability problems.

For best performance results, noise should be minimized on the analog power and ground pins of the CDC5XX and CDC25XX devices by using a filter. The CDC5XX platform of devices provides separate analog V_{CC} and GND pins, which allows the user to isolate the PLL from noisy voltage planes. For the CDC586/2586/582/2582, pins 43 and 46 are the analog V_{CC} pins for the PLL, while pins 47 and 49 are the analog grounds for the PLL. These devices are most susceptible to noise within the 10-kHz to 1-MHz range; therefore, the filter should be designed to attenuate this frequency range. A low-pass filter and local decoupling, as shown in Figure 12, can be used to isolate the PLL from noise sources.

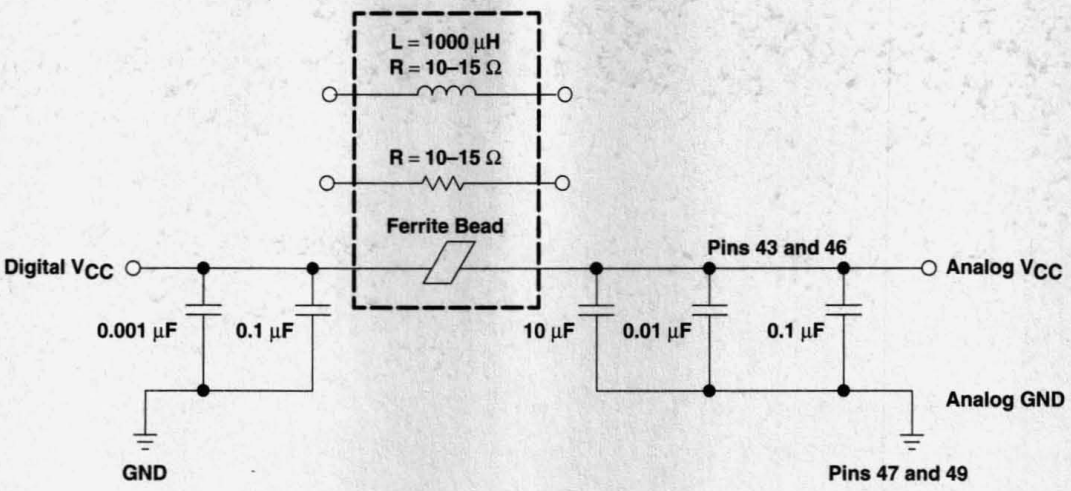


Figure 12. Analog Power Filter

The filter can be designed using a choke, a low-ohm resistor, or a ferrite bead. The choke should provide the best overall filter performance; however, a lower cost filter can be implemented using a ferrite bead or resistor. Ferrite beads that are primarily resistive are recommended for the best attenuation. If a single bead does not provide sufficient attenuation, two to three beads can be connected in series to improve filter performance. A low-ohm resistor, i.e., 10 Ω to 15 Ω, can be used instead of the ferrite to provide better low-frequency attenuation at a lower cost than using a choke. The analog circuits of the CDC586 typically consume about 1 mA of current, with a worst-case consumption of 5 mA. The dc voltage drop across the analog filter should be considered when evaluating filter options. For a ferrite bead, the dc voltage drop is nominally zero, and for a 15-Ω resistor, the maximum dc voltage drop is 75 mV.

The 0.1-µF and 0.001-µF capacitors provide local decoupling of the analog supply. In addition, the digital supply pins should also be decoupled using 0.001-µF to 0.1-µF capacitors. For decoupling, low-inductance ceramic-chip capacitors are recommended. For best results, all components (both decoupling capacitors and filter components) should be placed as close as possible to supply pins of the device.

Acknowledgment

The author of this document is Grant E. Ley.

References

Letter B JC–10–90–119A, Terms, Symbols, and Definitions for Skew Parameters.

Blood, William R., Jr., MECL System Design Handbook, 1983, Motorola Inc.

Clock Distribution in High-Performance PCs

SCAA030A
February 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**6–27**
What is Skew?	**6–28**
Output Skew	6–28
Input Skew	6–28
Pulse Skew	6–28
Process Skew	6–28
Limit Skew	6–29
Power Dissipation	**6–30**
High-Speed Design Considerations	**6–31**
Summary	**6–32**
Acknowledgment	**6–32**

List of Illustrations

Figure	*Title*	*Page*
1	Clock Network	6–27
2	Example of a Gate With Input Skew	6–28
3	Skew Definitions	6–29
4	CDC337 Power Dissipation	6–31

EPIC and EPIC-IIB are trademarks of Texas Instruments Incorporated.

Introduction

Personal computer and workstation designers are pushing the operating speeds of new equipment to ever-higher frequencies with technological advances in areas such as RISC/CISC microprocessors, high-speed SRAMs, and cache memories. At higher frequencies, the timing delays and uncertainties associated with clock-signal generation and distribution in a system become critical factors in determining the system's overall performance and reliability. System performance is optimized by carefully considering the attributes of the components used in designing the clock circuit. The clocking network is the heart of any system. There are two main aspects to this network: clock generation and clock distribution. Clock generation is accomplished by taking the output of some source (a crystal oscillator, for example) and manipulating it to obtain pulses with a specific frequency, duty cycle, and amplitude. These signals are then fanned out to the various system components by a clock-distribution network (see Figure 1). As system speeds rise to 33, 40, or 50 MHz and clock periods grow shorter, the uncertainties of meeting setup, hold, and pulse duration requirements become critical due to a narrowing time window. A clocking system that does not fully consider these uncertainties will suffer degraded performance and reliability.

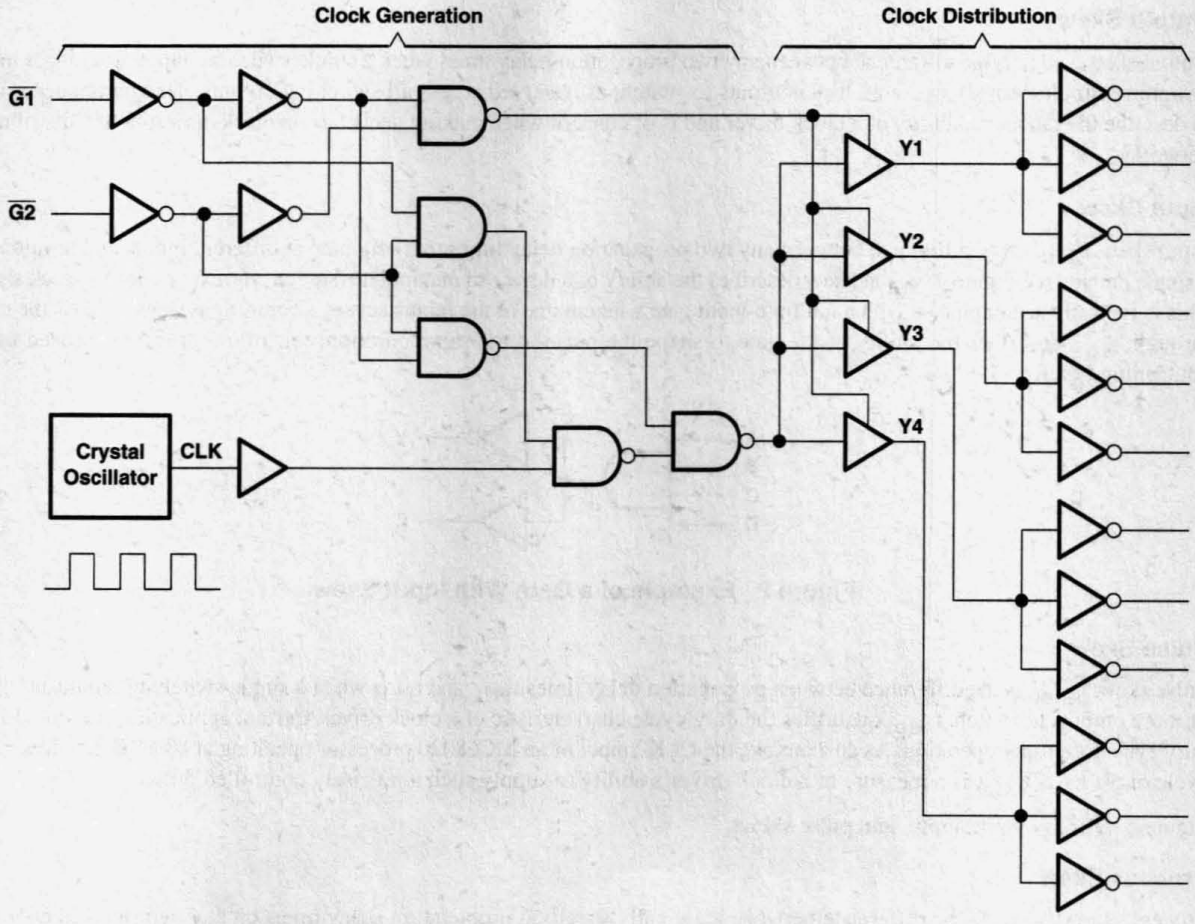


Figure 1. Clock Network

Texas Instruments (TI), as well as several of the other major integrated-circuit (IC) vendors, offers the designer a choice of clock generation and distribution circuits commonly referred to as clock drivers. Clock-driver ICs are able to provide clock generation functions (frequency multiplication, division, and duty-cycle control) as well as clock-distribution functions (buffering and fanout) with timing specifications unavailable on older CMOS and TTL logic families. Advances in process technology have allowed IC vendors to offer circuits with tight specifications on switching speeds and skew parameters. The high speed, fast edge rates, and tight skew specifications offered on clock-driver data sheets give the designer additional flexibility, but component selections must be closely tied to proper board-layout techniques. The purpose of this application report is to discuss considerations in the design of clocking networks for high-performance systems wherein proper clock generation and distribution are essential.

What Is Skew?

Any discussion of clock-driver attributes ultimately centers around skew. Simply defined, skew is the difference between the expected and actual arrival time of a clock pulse. In an ideal clock circuit, propagation delays remain fixed and equal for high-to-low and low-to-high transitions over the entire ranges of supply voltage, operating temperature, and output loading and are independent of the number of outputs switching. However, the world is not ideal, and definitions have evolved to help the designer deal with the various types of skew that can be encountered. Clock-driver performance can be described in terms of five types of skew as defined in JEDEC Standard 99, clause 2.3.5.

Output Skew

Output skew, $t_{sk(o)}$, is the difference between any two propagation-delay times when a single switching input or multiple inputs switching simultaneously cause multiple outputs to switch, as observed across all switching outputs. This parameter is used to describe the fanout capability of a clock driver and is of concern when making decisions on clock buffering and distribution networks.

Input Skew

Input skew, $t_{sk(i)}$, is the difference between any two propagation delay times that originate at different inputs and terminate at a single output (see Figure 2). Input skew describes the ability of a device to manipulate (stretch, shrink, or chop) a clock signal. This is typically accomplished with a multiple-input gate wherein one of the inputs acts as a controlling signal to pass the clock through. $t_{sk(i)}$ describes the ability of the gate to shape the pulse to the same duration, regardless of the input used as the controlling input.

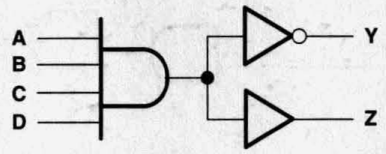


Figure 2. Example of a Gate With Input Skew

Pulse Skew

Pulse skew, $t_{sk(p)}$, is the difference between propagation delay times t_{PHL} and t_{PLH} when a single switching input causes one or more outputs to switch. $t_{sk(p)}$ quantifies the duty-cycle characteristic of a clock driver. Certain applications require a fixed duty cycle for proper operation. As an example, the CLK2 input of an MC68020 processor operating at 40 MHz requires a duty cycle of 50 ±5%. $t_{sk(p)}$ is a measure of a clock driver's ability to supply such a precisely controlled pulse.

Figure 3 defines output, input, and pulse skews.

Process Skew

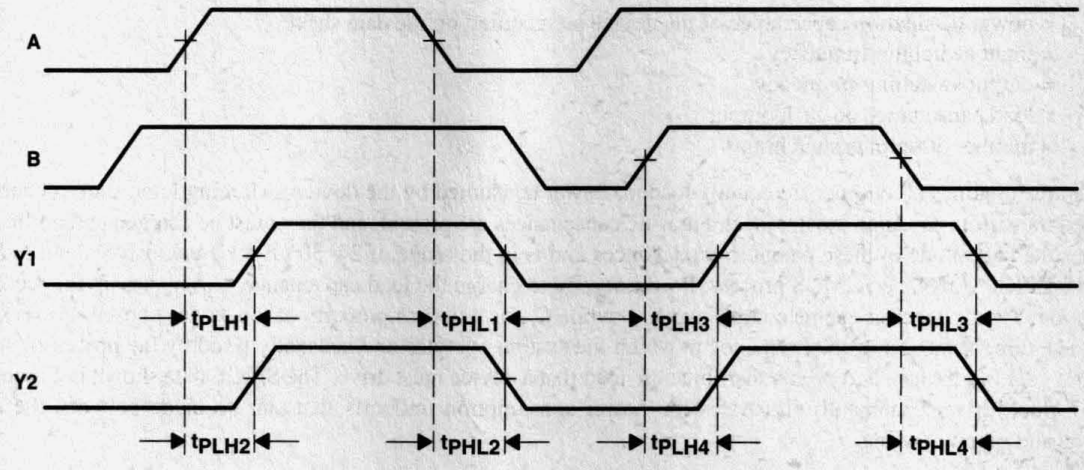
Process skew, $t_{sk(pr)}$, is the difference between identically specified propagation-delay times on any two like ICs operating under identical conditions. $t_{sk(pr)}$ quantifies the skew induced by variations in the IC manufacturing process but not by variations in supply voltage, operating temperature, output loading, input edge rate, input frequency, etc. Process skew is commonly specified and production tested under fixed conditions (e.g., V_{CC} = 5.25 V, T_A = 70°C, C_L = 50 pF, all inputs switching simultaneously).

Limit Skew

Limit skew, $t_{sk(l)}$, is the difference between the greater of the maximum specified values of t_{PLH} and t_{PHL} and the lesser of the minimum specified values of t_{PLH} and t_{PHL}. Limit skew is not observed directly on a device, but is calculated from the data sheet limits for t_{PLH} and t_{PHL}. $t_{sk(l)}$ quantifies for the designer how much variation in propagation delay time will be induced by operation over the entire ranges of supply voltage, temperature, output load, and other specified operating conditions. Specified as such, $t_{sk(l)}$ also accounts for process variation. In fact, all other skew specifications ($t_{sk(o)}$, $t_{sk(i)}$, $t_{sk(p)}$, and $t_{sk(pr)}$) are subsets of $t_{sk(l)}$; they will never be greater than $t_{sk(l)}$.

In general, not all skew parameters of a device are of interest, but their discussion is included for illustration. The designer's goal is to minimize skew to an acceptably small fraction of the system clock period. A design rule of thumb is that clock skew should be less than 10% of the system clock period.

The desired operating frequency determines the designer's *skew budget*, or the maximum amount of skew allowed. For example, a system operating at 33 MHz has a period of 30.3 ns, and using the 10% rule, the allowable skew budget is 3 ns. At 50 MHz, the period is reduced to 20 ns and the permissible skew is now a scant 2 ns. Components in the clock network must be carefully selected to meet the shrinking skew budget as operating frequencies increase.



$t_{sk(o)}$ is calculated from the following expressions: $|t_{PLH1} - t_{PLH2}|$, $|t_{PHL1} - t_{PHL2}|$, $|t_{PLH3} - t_{PLH4}|$, $|t_{PHL3} - t_{PHL4}|$

$t_{sk(l)}$ is calculated from the following expressions: $|t_{PLH1} - t_{PLH3}|$, $|t_{PHL1} - t_{PHL3}|$, $|t_{PLH2} - t_{PLH4}|$, $|t_{PHL2} - t_{PHL4}|$

$t_{sk(p)}$ is calculated from the following expressions: $|t_{PLH1} - t_{PHL1}|$, $|t_{PLH2} - t_{PHL2}|$, $|t_{PLH3} - t_{PHL3}|$, $|t_{PLH4} - t_{PHL4}|$

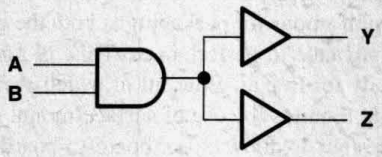


Figure 3. Skew Definitions

Power Dissipation

Power consumption becomes an important consideration as operating frequencies rise, but is often overlooked as a designer tackles other issues. A much-touted aspect of devices fabricated in CMOS and BiCMOS technologies is low power consumption, especially when compared to equivalent devices fabricated in a purely bipolar process. At lower frequencies, this generalization holds true, but power consumption at higher frequencies becomes less a function of process technology and more a function of output loading. To illustrate this point, the dynamic power (P_d) consumed by a CMOS device will be examined. The dynamic power consumed consists of two components:

- Power used by the device as it switches states
- Power required to charge any load capacitance

P_d is easily calculated using the following expression:

$$P_d = \left(C_{pd} \times V_{CC}{}^2 \times f_i\right) + n(C_L \times V_{CC} \times f_o) \quad (1)$$

Where:

C_{pd} = power dissipation capacitance of the device as specified on the data sheet
f_i = input switching frequency
f_o = output switching frequency
C_L = load capacitance on each output
n = number of outputs switching

This example assumes all outputs are equally loaded. Power consumed by the device switching logic states occurs because fabricated transistors on a chip are not ideal. Parasitic capacitances are present, and they must be charged and discharged. C_{pd} quantifies the magnitude of these parasitic capacitances and is in the range of 24–30 pF for clock-driver devices fabricated using TI's EPIC™ Advanced CMOS process. Power needed to charge the load capacitance, C_L, makes up the second half of the equation. The designer has some control over C_L, while C_{pd} is strictly a property of the device chosen. Power consumed by both is a direct function of the frequency at which the system operates and is usually fixed by the processor speed. The designer's goal is to reduce and evenly distribute the load that a device must drive. The SPICE data shown in Figure 4 for the CDC337 clock driver graphically illustrates the power-consumption tradeoffs that can be made between the switching frequency and output loading.

The CDC337 is fabricated in TI's EPIC-IIB™ BiCMOS process and contains four buffered outputs that switch at the clock frequency and four divide-by-two outputs that toggle at one-half the clock frequency. It is specifically designed for applications requiring synchronized output signals at both the clock frequency and one-half the clock frequency. Power consumption also has implications for packaging at both the component and system levels. The general trend is that the system box shrinks with each advance in performance. This, in turn, requires smaller power supplies, closer board-to-board spacing, and reduced capacity for free air flow, all of which are not compatible with power-hungry designs. Increased system packaging density usually requires the use of surface-mount components that do not have the higher heat dissipation properties of larger DIP devices but do allow closer board-to-board spacing and component placement on both sides of the circuit board. All of these factors can drive up system operating temperature and cost. Power consumption can make or break a system design and should not be treated lightly.

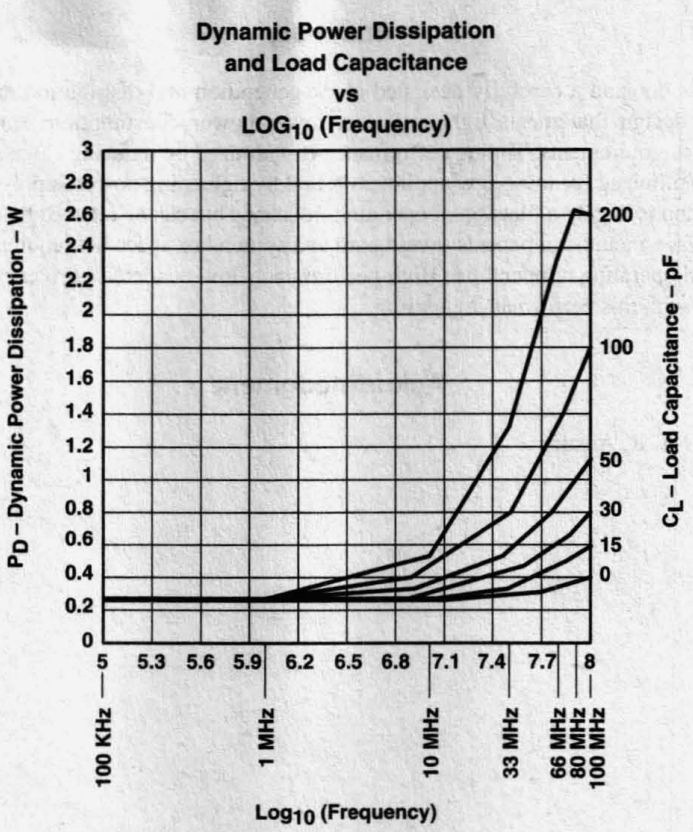


Figure 4. CDC337 Power Dissipation

High-Speed Design Considerations

A number of tightly specified, high-speed, high-drive clock-driver circuits are available to aid the designer in developing a system-clocking network. By carefully following established high-speed circuit design techniques, the designer can achieve superior performance from standard components and not incur the high cost of custom components. Transmission-line effects take over in high-speed, high-drive designs, and attention to detail during board layout is critical. A sound high-speed design uses all of the following techniques and rules of thumb:

- Keep output loading as light as possible. This reduces power consumption, allows switching at higher frequencies, and reduces skew.
- Equally load all outputs where possible
- Use short, equal-length etch runs
- Avoid sharp corners that may induce unwanted reflections, ringing, and overshoot due to discontinuities
- Properly decouple all device V_{CC} pins as close to the pins as possible. The best high-frequency filtering is often accomplished with a combination of capacitors. An effective combination is 0.1 µF in parallel with 0.01 µF or 0.005 µF. Use RF-quality (low-inductance) capacitors.
- Use a multilayer board with low-impedance power and ground planes to minimize circuit noise
- Select components with low-noise characteristics. Components optimized for low noise usually have multiple V_{CC} and GND pins interspersed among the device outputs to help reduce noise.

Summary

High-performance systems demand a carefully designed clock-generation and distribution network. The designer has the challenge of outlining a design that meets tighter timing, lower power consumption, smaller space, lower operating temperature, and lower cost requirements. Timing performance is optimized by reducing clock skew. Skew can be minimized by selecting components optimized for low-skew applications and by tightening power-supply requirements to ±5% instead of ±10%. Power consumption is largely a function of operating frequency but can be reduced by making output loading as light as possible. The use of surface-mount components saves board and system box space but requires analyzing tradeoffs in power consumption, air flow, and operating temperature. High-performance, low-cost clock-driver components are now available that can help the designer with this performance juggling.

Acknowledgment

The author of this report is A. R. Austin.

EMI Prevention in Clock-Distribution Circuits

SCAA031
June 1994

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1994, Texas Instruments Incorporated

Contents

Title	Page
Introduction	**6–37**
Higher Harmonic Components of Digital Waveforms	**6–37**
Transmission Line and Radiated Emissions	6–40
The Antenna Effect	6–42
Spectrum Analyzer Results	6–43
Effects of Impedance Matching	6–44
Summary of Methods for EMI Prevention	**6–48**
Characteristic Impedance of the Transmission Line	6–48
PCB Shielding Effects	6–48
Impedance Matching	6–48
Conclusion	**6–48**
Acknowledgment	**6–48**

List of Illustrations

Figure	Title	Page
1	Triangle Wave	6–37
2	Spectrum Envelope for Triangle Wave of Figure 1	6–37
3	Square Wave	6–38
4	Spectrum Envelope for Square Wave Shown in Figure 3	6–38
5	Square Wave, Duty Cycle = 50%	6–39
6	Spectrum Envelope for Square Wave Shown in Figure 5	6–39
7	Square Wave, Duty Cycle = 50%	6–39
8	Spectrum Envelope for Square Wave Shown in Figure 7	6–39
9	Transmission Line With a Driver and a Receiver	6–40
10	Transmission Line With a Termination Resistor Value Less than Z_o	6–41
11	Impedance Matching Through a Pulldown Resistor	6–41
12	Impedance Matching Through Parallel Resistors (Thevenin's Termination)	6–42
13	Impedance Matching Through a Damping Resistor	6–42
14	Antenna Effect of Transmission Lines	6–42
15	Block Diagram of Test Setup for Measuring Radiated Emissions	6–43
16	Emission Level vs Frequency	6–44
17	Test Setup With Unterminated Transmission Lines	6–44
18	Test Setup With 56-Ω Damping Resistor Terminations	6–45
19	EMI Evaluation Results (Device Under Test = CDC208)	6–46
20	EMI Evaluation Results (Device Under Test = CDC204)	6–46
21	EMI Evaluation Results (Device Under Test = ABT240)	6–47
22	EMI Evaluation Results (Device Under Test = CDC303)	6–47

Introduction

Although the importance of electromagnetic interference (EMI) has been recognized, most system designers have tended to handle the problem by shielding via metal cabinets or through RC networks to limit the rise and fall times of digital pulse waveforms. These design practices were motivated by 1) a lack of EMI-prevention design rules and by 2) designers' tendencies to prioritize apparent system performance only to have that performance subsequently degraded through the later addition to the system of EMI-prevention devices such as metal chassis or RC networks.

With the current trend towards lighter, more compact personal computers and engineering workstations, system designers can no longer rely upon after-the-fact EMI shielding techniques; rather, they must learn to build in EMI protection at the design stage. This application report discusses EMI protection for a clock distributor, an application characterized by multiple simultaneously switching bits and relatively long transmission lines.

Higher-Harmonic Components of Digital Waveforms

In general, the decay rate of a Fourier-spectrum envelope is greater for a waveform with slow rise and fall times than for a waveform with fast rise and fall times. Figures 1 and 2 show a triangular waveform and its spectrum envelope. The 12 dB/octave decay rate shown in Figure 2 means that if two x-axis values of 1X frequency and 2X frequency are considered, the corresponding y-axis values are 1X and 1/4X amplitude, respectively.

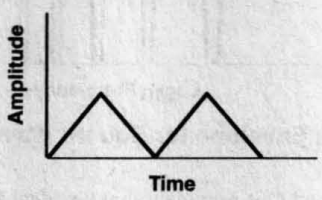


Figure 1. Triangle Wave

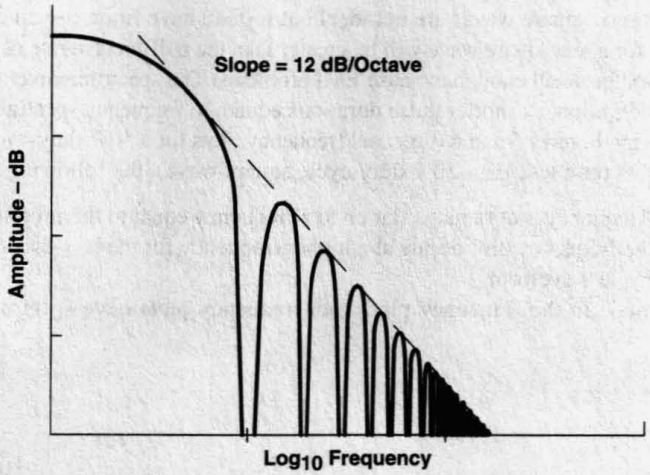


Figure 2. Spectrum Envelope for Triangle Wave of Figure 1

Figures 3 and 4 show an ideal square waveform (0-ns rise and fall times) and its spectrum envelope. Comparing 1X frequency and 2X frequency x-axis values, the corresponding y-axis values are 1X and 1/2X, respectively.

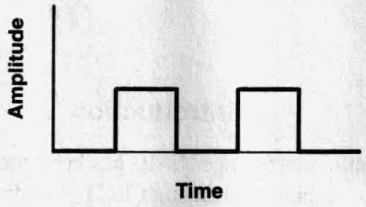


Figure 3. Square Wave

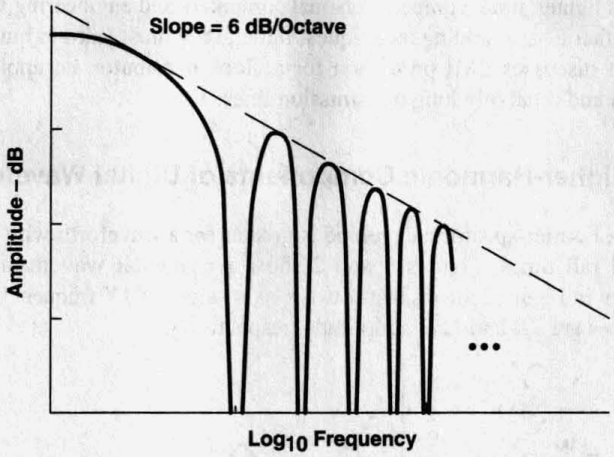


Figure 4. Spectrum Envelope for Square Wave Shown in Figure 3

By comparing Figures 1 and 2 with Figures 3 and 4, it is evident that the ideal square wave, with its sharp discontinuities (0-ns rise and fall times), contains many more higher harmonics than does the triangle wave. Hence, an electronic circuit stimulated by an ideal square wave would require employment of more EMI-protection design techniques than a circuit stimulated by a triangle wave of the form shown in Figure 1.

In real digital-circuit applications, square waves are not ideal but instead have finite rise and fall times. Although the decay rate of the spectrum envelope for a real square wave will be greater than the 6 dB/octave rate of the ideal square-wave spectrum envelope, its decay rate will still be small enough to cause EMI problems. The spectrum-envelope decay rate for a square wave is also dependent on its pulse duration, as shorter pulse durations equate to frequency spectra exhibiting higher amplitudes at higher frequencies. In comparing Figures 5 and 6 (time and frequency plots for a 50% duty-cycle square wave) with Figures 7 and 8 (time and frequency plots for a less-than-50% duty-cycle square wave), the following may be observed:

- The amplitude-vs-frequency plot remains flat up to a frequency equal to the inverse of the pulse duration, or $1/t_w$. This first node in the frequency plot occurs at a higher frequency for the less-than-50% duty-cycle waveform than for the 50% duty-cycle waveform.
- Beyond this first node in the frequency plot, both frequency plots have spectrum envelopes that decay at the 6 dB/octave rate.

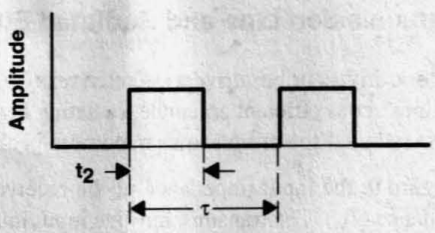


Figure 5. Square Wave, Duty Cycle = 50%

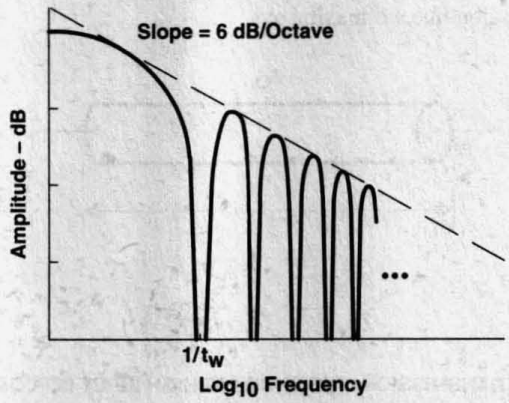


Figure 6. Spectrum Envelope for Square Wave Shown in Figure 5

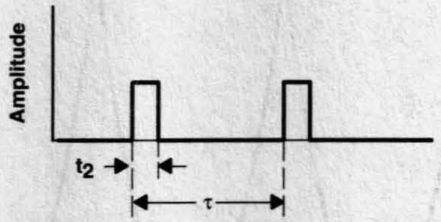


Figure 7. Square Wave, Duty Cycle < 50%

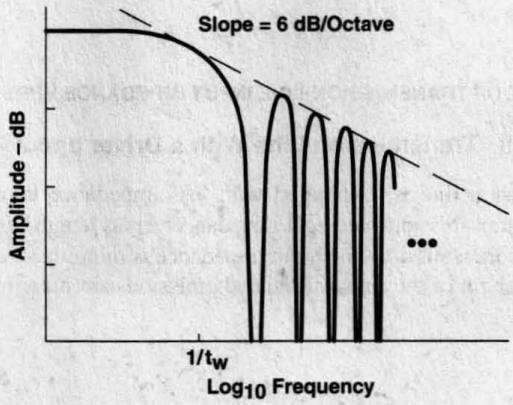
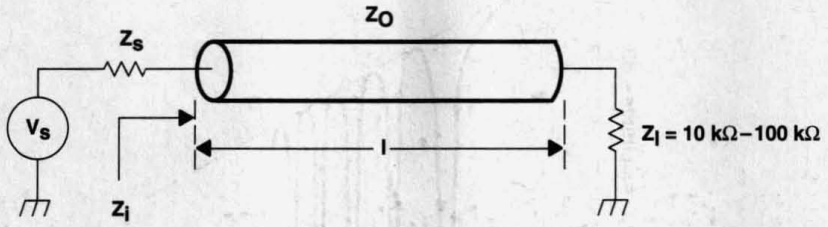


Figure 8. Spectrum Envelope for Square Wave Shown in Figure 7

Transmission Line and Radiated Emissions

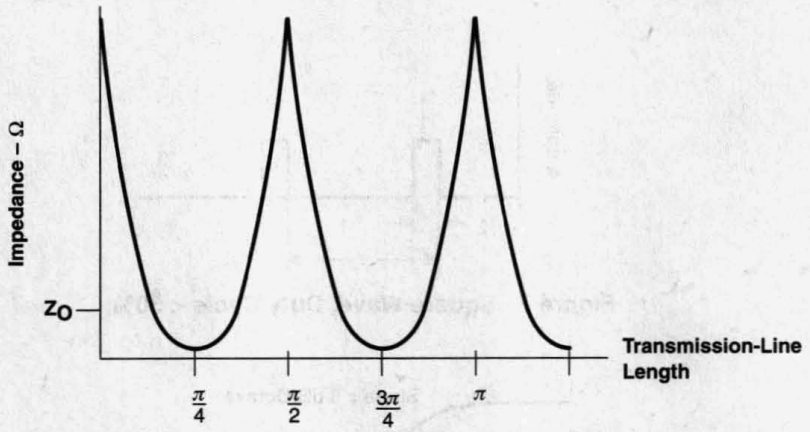
The transmission lines connected to clock drivers or bus drivers are often relatively long. When transient currents flow on such transmission lines, the transmission lines act as efficient antennae, radiating high-frequency electromagnetic waves. If such a transmission line is unterminated, its radiated spectrum shows maximum peak voltage.

In the transmission line shown in Figure 9, the input impedance of the receiver is high (10 kΩ to 100 kΩ) relative to the transmission-line characteristic impedance (Z_O). The transmission-line input impedance versus length can be represented by a cotangent function. For a particular signal frequency, the transmission-line input impedance is at a minimum when the transmission-line length is an odd multiple of 1/4 of the wavelength of the signal. When the frequency spectrum of the output waveform of the driver shown in Figure 9 contains such frequency components, current through the transmission line and radiated emissions from the transmission line are maximized.



$$Z_i = -jZ_o \cot\left(\frac{2\pi l}{\pi}\right)$$

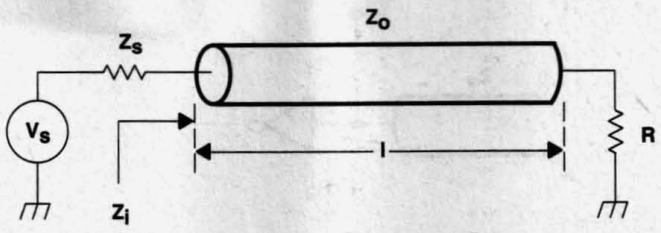
(a) MODEL OF TRANSMISSION LINE SHOWING HIGH INPUT IMPEDANCE OF RECEIVER



(b) PLOT OF TRANSMISSION-LINE INPUT IMPEDANCE VERSUS LENGTH

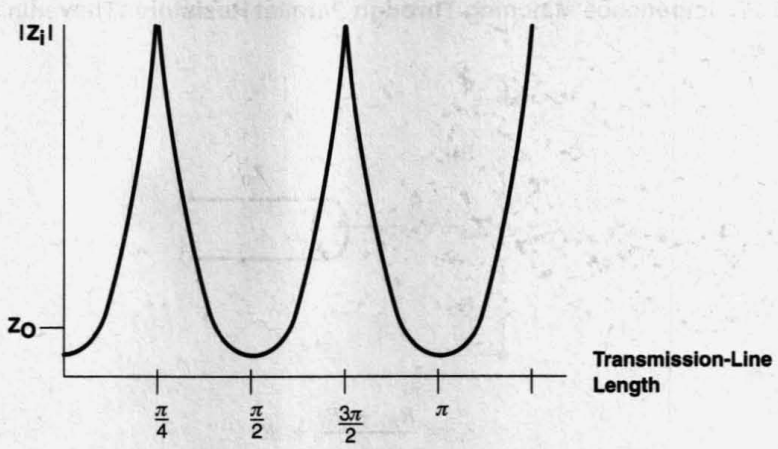
Figure 9. Transmission Line With a Driver and a Receiver

On the other hand, if the transmission line is terminated with less impedance than the transmission-line characteristic impedance (Z_O) (see Figure 10), the transmission-line input impedance versus length can be represented by a tangent function. For a particular signal frequency, the transmission-line input impedance is minimized when the transmission-line length is an integer multiple of 1/2 of the wavelength of the signal. Radiated emissions are maximized at these frequencies.



$$Z_i = -jZ_o tan\left(\frac{2\pi l}{\pi}\right)$$

(a) MODEL OF TRANSMISSION LINE SHOWING TERMINATION RESISTOR R < Z_O

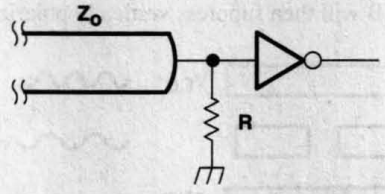


(b) PLOT OF TRANSMISSION-LINE INPUT IMPEDANCE VERSUS LENGTH

Figure 10. Transmission Line With a Termination Resistor Value Less Than Z_O

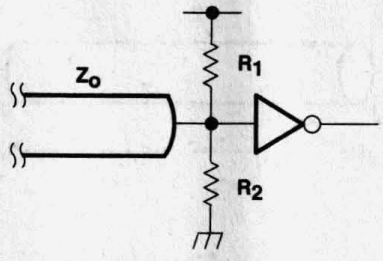
In summary, impedance mismatching causes a maximum current flow on the transmission line, thus maximizing radiated emissions. It is obviously desirable to assure impedance matching to minimize radiated emissions. There are two basic methods of assuring impedance matching: 1) termination at a line end point, and 2) termination at a line start point.

Terminating the end of a transmission line can be done either by use of a pulldown resistor (see Figure 11) or through parallel resistors (the so-called Thevenin's termination; see Figure 12). Termination at a transmission-line start point is done via a damping resistor (see Figure 13).



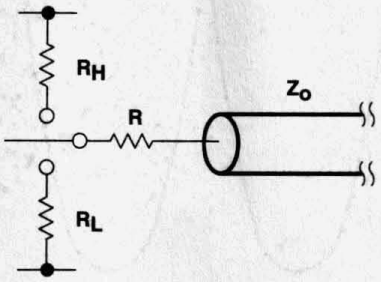
$$Z_o = R$$

Figure 11. Impedance Matching Through a Pulldown Resistor



$$Z_o = \frac{R_1 \times R_2}{R_1 + R_2}$$

Figure 12. Impedance Matching Through Parallel Resistors (Thevenin's Termination)



$$Z_o = \frac{R_H + R_L}{2} + R$$

Figure 13. Impedance Matching Through a Damping Resistor

For a clock-distribution circuit, in which transmission is restricted to a single direction, termination at the transmission-line start point (i.e., through a damping resistor) is recommended as this approach minimizes power consumption (albeit at the cost of a slight increase in the clock signal rise and fall times). In contrast, a Thevenin (end-of-transmission-line) termination is recommended for bus interface circuits wherein bidirectional signal flow is assumed.

The Antenna Effect

When relatively long transmission lines have a high characteristic impedance, they tend to mimic antennae, both receiving and radiating noise easily, so it is desirable to design transmission lines with as low a characteristic impedance as possible. When a multilayered printed-circuit board (PCB) is used, transmission lines can be laid out on an intermediate layer; the shielding effects of the V_{CC} and GND planes of the PCB will then suppress vertically polarized waves.

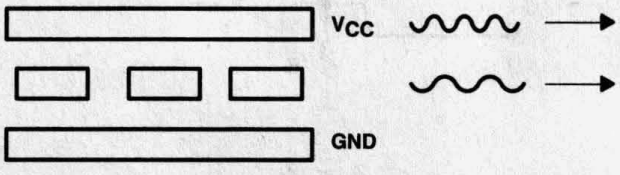
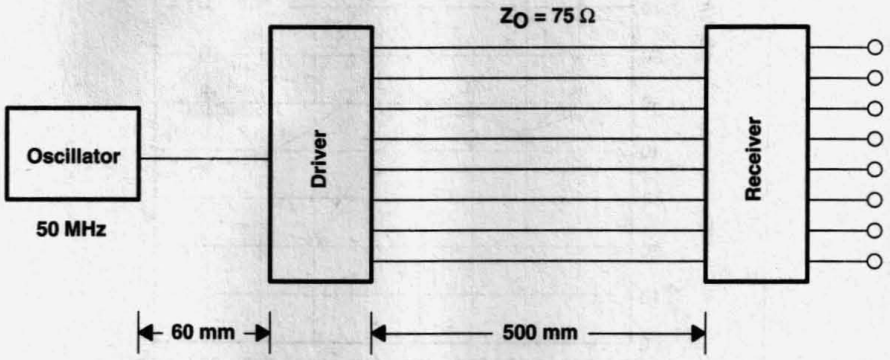


Figure 14. Antenna Effect of Transmission Lines

Spectrum Analyzer Results

Data from the test setup shown in Figure 15 was examined via a spectrum analyzer to determine which element of the test setup was most critical relative to radiated emissions (the oscillator, the shielded line, the driver, the transmission lines, or the receiver) and to observe the effects of line terminations. The data as plotted in Figure 16 showed that the oscillator exhibits a maximum value of 47dBμV/m at 150 MHz and that the oscillator has high shielding capability. Table 1 gives the mean and maximum values for the four plots in Figure 16. It is clear from Figure 16 that the transmission line is the most significant contributor to radiated emissions.



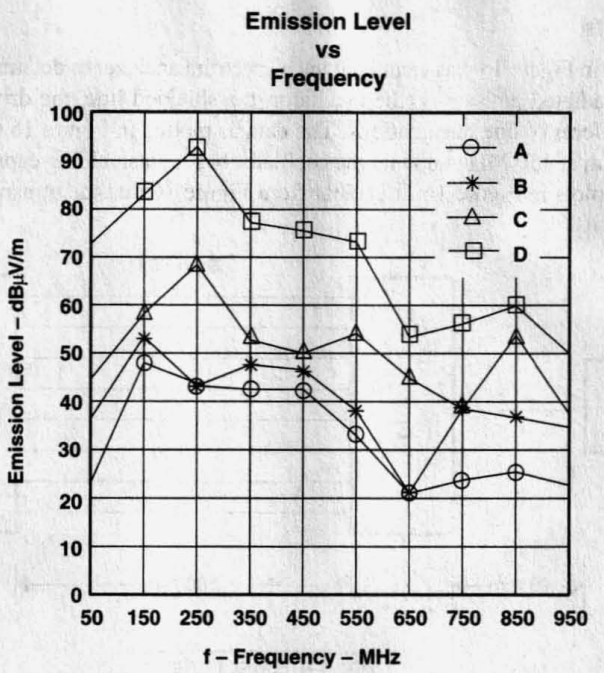
DRIVER	RECEIVER
CDC209	CDC204
CDC204	CDC204
CDC303	AS245
ABT240	ABT240

Figure 15. Block Diagram of Test Setup for Measuring Radiated Emissions

Table 1. Comparison of Radiated Emissions

	MEAN	MAX
A	33	47
B	38	54
C	49	68
D	67	93

Units: dBμV/m
Driver: CDC208
Receiver: CDC204



A = Oscillator
B = Oscillator + Shielded Line
C = Oscillator + Shielded Line + Driver
D = Oscillator + Shielded Line + Driver + Transmission Line + Receiver

Figure 16. Emission Level vs Frequency

Effects of Impedance Matching

Practically speaking, impedance matching is the easiest way to minimize radiated emissions. Figures 17 and 18 show test setups (transmitter = CDC208; receiver = CDC204) with unterminated transmission lines and with transmission lines terminated with 56-Ω damping resistors, respectively. The oscilloscope display for the transmitted waveform from the test setup of Figure 17 showed significant overshoot and undershoot due to signal reflections, and a spectrum analyzer showed a maximum value of 90 dBμV/m. In contrast, the transmitted waveform from the test setup of Figure 18 showed no overshoot and undershoot, and the amplitudes of higher-harmonic components were reduced.

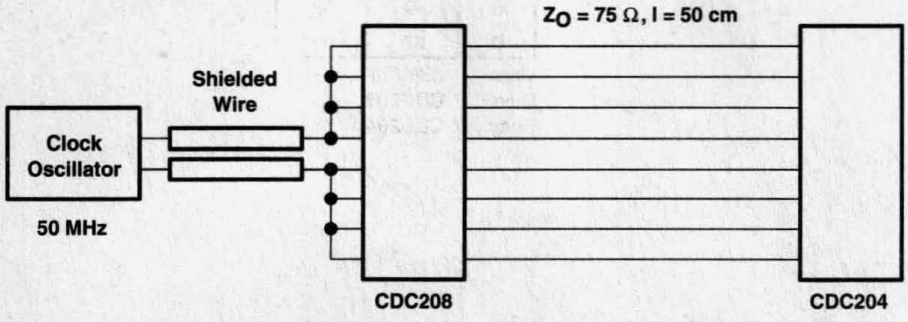


Figure 17. Test Setup With Unterminated Transmission Lines

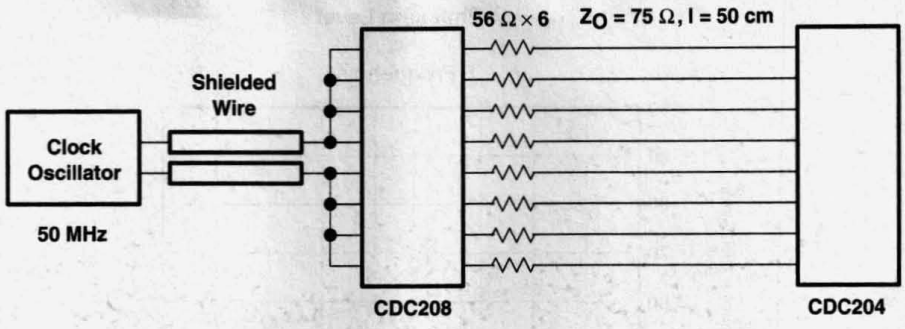


Figure 18. Test Setup With 56-Ω Damping-Resistor Terminations

Similar analyses were made using CDC204/CDC204 and ABT240/ABT240 transmitter/receiver pairs. The results for all three transmitter/receiver pairs for unterminated transmission lines are summarized in Table 2.

Table 2

INTERFACE	MIN	MAX
CDC208–CDC204	8.8	17
CDC204–CDC204	4.9	9.2
ABT240–ABT240	7.3	13

Units: dBμV/m
NOTE: MIN and MAX values at higher harmonics

In the case of transmission lines terminated with 56-Ω damping resistors, the data values in Table 2 could be expected to improve by 5 to 9 dBμV/m (means) and 9 to 17 dBμV/m (maximums).

Figures 19 through 22 show EMI evaluation results for CDC208, CDC204, ABT240, and CDC303 devices in both unterminated and damping-resistor-terminated configurations. The x-axis (frequency) values in these figures are odd higher harmonics for the given transmission lines. The radiated emission values in these figures are relatively high for the following reasons:

- The transmission lines were up to 500 mm in length.
- The transmission lines were laid out on a surface layer of the PCB.
- The PCBs were not shielded by metal cabinets.

Figures 19 through 22 clearly show that when signal reflections are controlled by impedance matching, the radiated emissions are reduced.

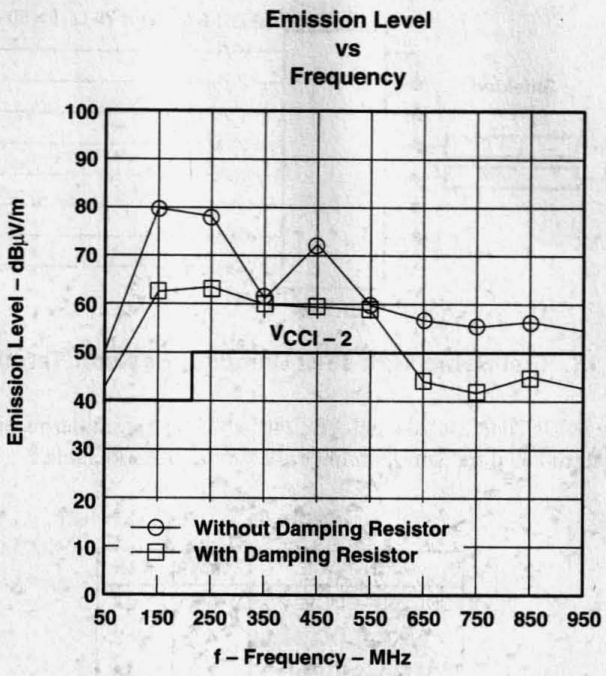


Figure 19. EMI Evaluation Results (Device Under Test = CDC208)

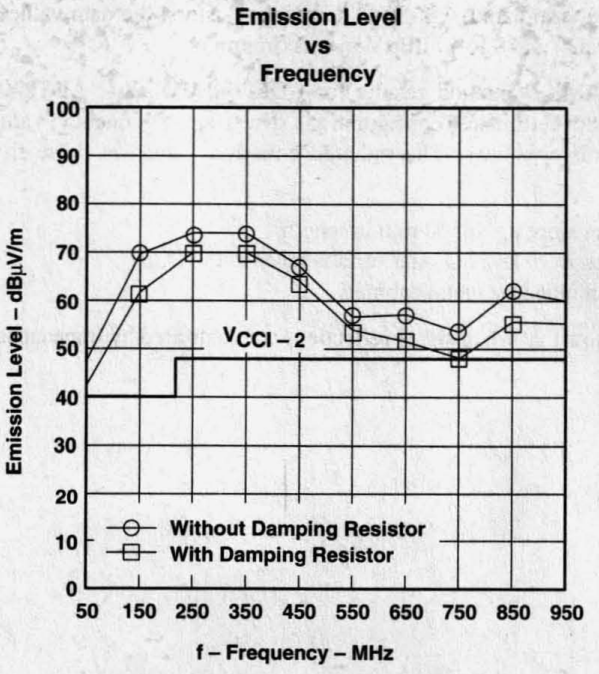


Figure 20. EMI Evaluation Results (Device Under Test = CDC204)

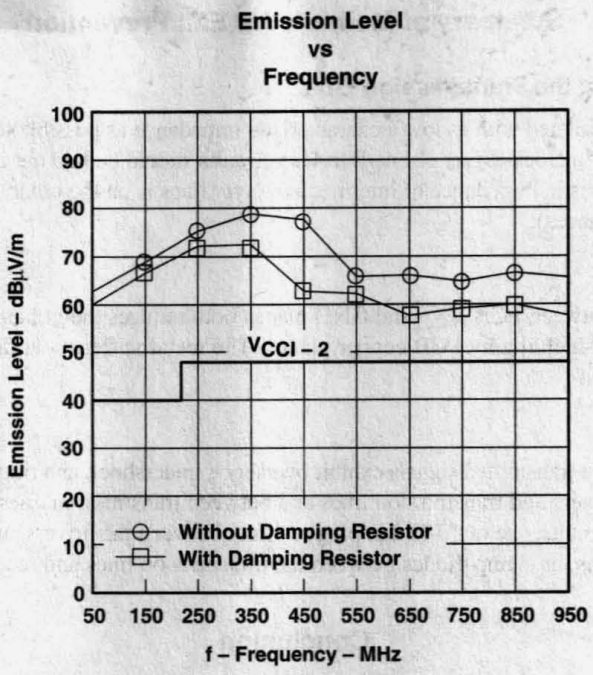


Figure 21. EMI Evaluation Results (Device Under Test = ABT240)

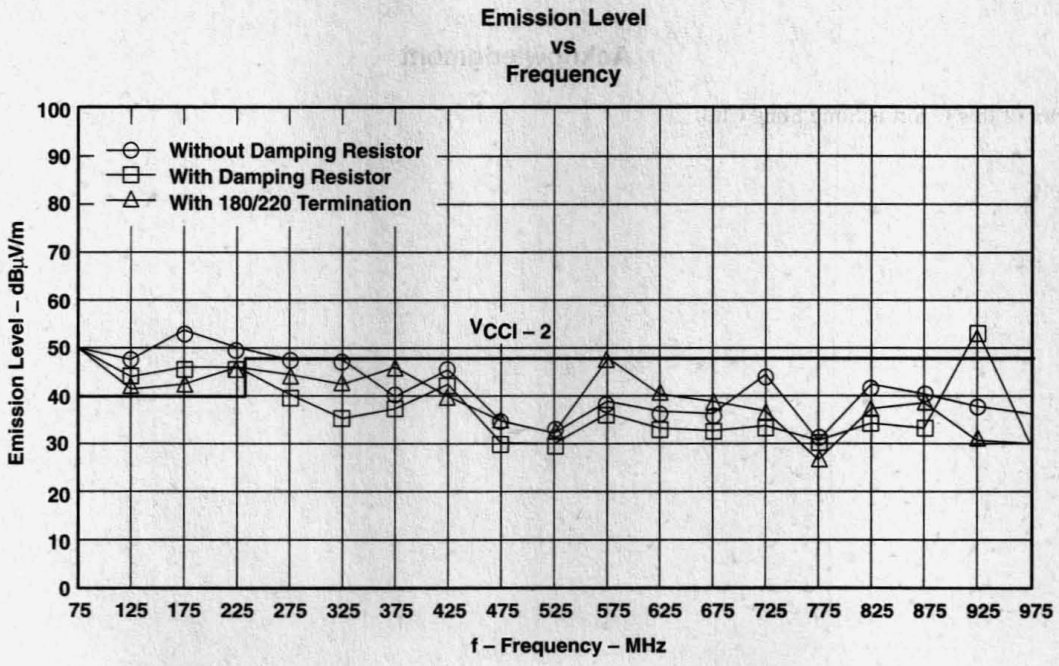


Figure 22. EMI Evaluation Results (Device Under Test = CDC303)

Summary of Methods for EMI Prevention

Characteristic Impedance of the Transmission Line

A transmission line should be designed with as low a characteristic impedance as possible to reduce the antenna effect. Long transmission lines such as those in clock-driver or bus-interface circuits should be laid out in intermediate PCB layers rather than surface layers (the characteristic impedance of intermediate-layer lines is on the order of 50 Ω, while surface-layer lines have 75-Ω characteristic impedances).

PCB Shielding Effects

Laying out transmission lines between PCB V_{CC} and GND planes both reduces their characteristic impedance and reduces horizontal polarization through shielding by PCB copper planes. The metal stiffeners at the PCB edges also shield against horizontal polarization.

Impedance Matching

Radiated emissions are high when transmitted signals exhibit overshoot, undershoot, and ringing. Careful impedance matching must be maintained between drivers and transmission lines and between transmission lines and receivers to minimize these effects. For clock-distribution circuits, use of 10-Ω damping resistors between the drivers and transmission lines or pulldown resistors, Thevenin's terminations, or clamp diodes between the transmission lines and receiver inputs is recommended.

Conclusion

As the data in this application report shows, unsuitable transmission-line terminations both contribute to radiated emissions and cause signal distortion. The evaluations described in this report seek not to measure exact values of radiated emissions but rather to demonstrate the effectiveness of impedance matching for reducing both radiated emissions and signal distortion.

Acknowledgment

The author of this report is Song Song Cho.

Minimizing Output Skew Using Ganged Outputs

SCAA032
June 1994

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1994, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**6–53**
Skew Definitions	**6–53**
Ganged Outputs	**6–53**
Performance Evaluation	**6–53**
Reliability	**6–57**
Applications	**6–57**
Acknowledgment	**6–57**

List of Illustrations

Figure	*Title*	*Page*
1	Graphics Plot CDC209 V_{OH}/I_{OH} Curves	6–54
2	Graphics Plot CDC209 V_{OL}/I_{OL} Curves	6–54
3	CDC209 Ganged Outputs	6–55
4	CDC209 t_{PLH} vs C_{LOAD}	6–55
5	CDC209 t_{PHL} vs C_{LOAD}	6–56
6	CDC209 Output Waveforms	6–56
7	Test Circuit	6–57

Introduction

The purpose of this application report is to help designers use existing clock-driver products to drive large loads and maintain a minimum amount of skew between outputs of the device. The emphasis of this report will be on using parallel, or ganged, outputs to drive loads.

Skew Definitions

Output Skew – $t_{sk(o)}$

Output skew is defined as the difference in propagation delay of the fastest and slowest paths on a single device that originate at either a single input or multiple simultaneously switched inputs. This parameter is useful when considering the distribution of a clock signal to multiple targets.

Pulse Skew – $t_{sk(p)}$

Pulse skew is defined as the difference between the propagation delay times t_{PLH} and t_{PHL} on the same pin at identical operating conditions. This parameter is useful when considering the output duty cycle characteristics of a device.

Process Skew – $t_{sk(pr)}$

Process skew is defined as the difference between propagation delay times on any two samples of an integrated circuit at identical operating conditions. This parameter addresses the difference in propagation delay times due to process variations.

Board Skew

Board skew is introduced into the clock system by unequal trace lengths and loads. It is independent of the skew generated by the clock driver. It is important to keep line lengths equal to minimize board skew.

When measuring propagation delays to determine the parameters $t_{sk(o)}$, $t_{sk(p)}$, and $t_{sk(pr)}$, the device(s) must be tested under identical operating conditions such as temperature, power supply voltage (V_{CC}), output loading, and input edge rates.

Ganged Outputs

As system frequencies increase, the need to minimize skews of clock drivers becomes critical to overall system performance. Existing non-PLL-based clock driver products deliver guaranteed output skews ($t_{sk(o)}$) in the 500-ps to 1-ns range. It is possible to use these low-skew clock drivers in a way that eliminates the output skew of the device. This can be achieved by using parallel, or ganged, outputs. Two or more outputs ganged (connected to a single transmission line) create a single clock source for all the target devices. Output skew of the clock driver is eliminated, and the drive capability is increased.

Performance Evaluation

To evaluate the impact of connecting all the outputs of a device to a single transmission line, a test board with traces of equal length to and from the inputs and outputs of the device was constructed. Using traces of equal length prevents board skew from being introduced into the system.

Various tests were performed on the CDC209 and CDC208 to evaluate their changes in performance when one output was used to drive a load versus four or eight ganged outputs. The dc-drive capability increases as more outputs are used to drive the load. Figures 1 and 2 show V_{OH}/I_{OH} and V_{OL}/I_{OL} curves displaying the difference between one, four, and eight outputs.

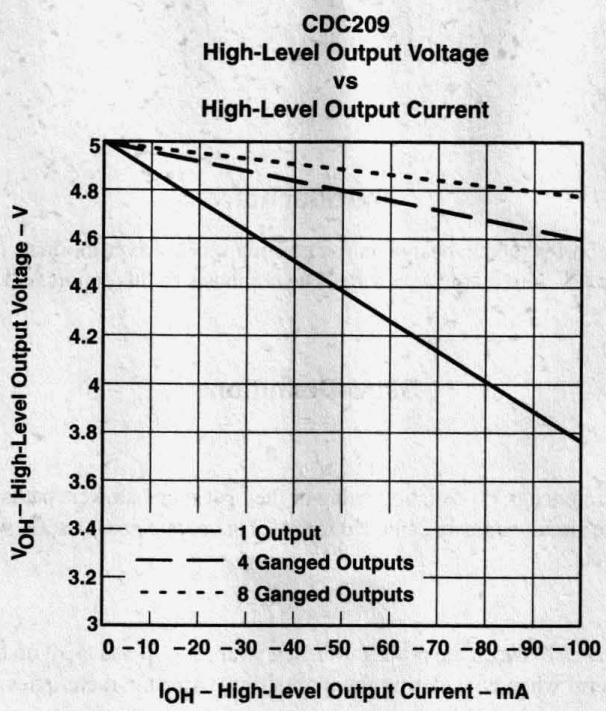


Figure 1. Graphics Plot CDC209 V_{OH}/I_{OH} Curves

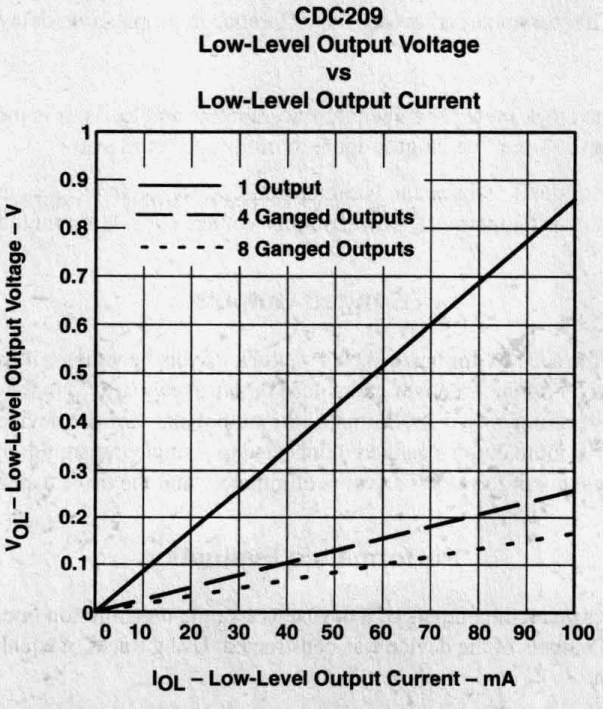


Figure 2. Graphics Plot CDC209 V_{OL}/I_{OL} Curves

Figure 3 shows the difference in supply current versus operating frequency for four and eight ganged outputs.

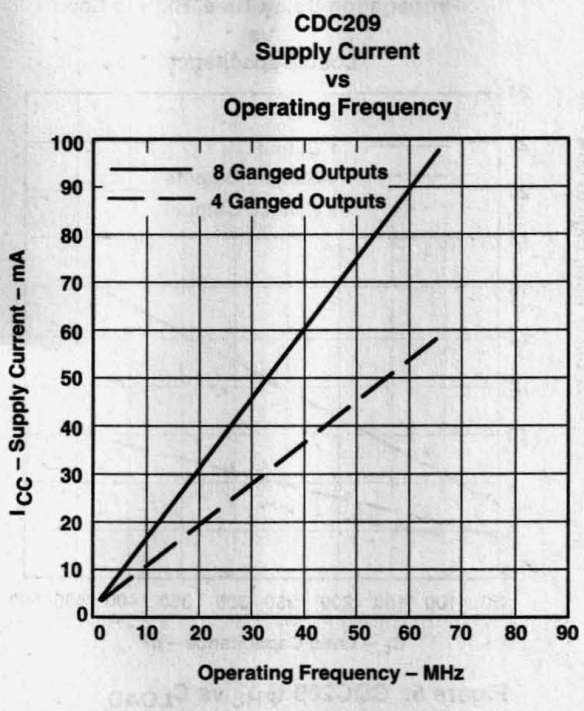


Figure 3. CDC209 Ganged Outputs

Figures 4 and 5 show the difference in t_{PLH} and t_{PHL} versus capacitive loading for one, four, and eight ganged outputs.

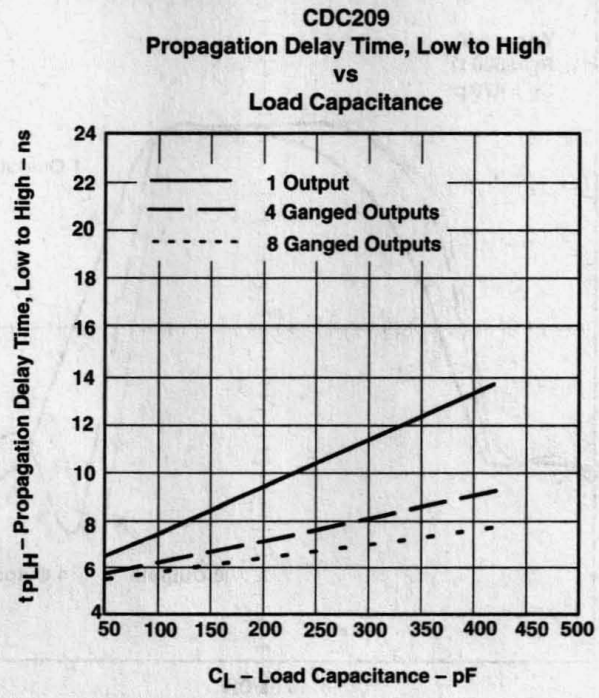


Figure 4. CDC209 t_{PLH} vs C_{LOAD}

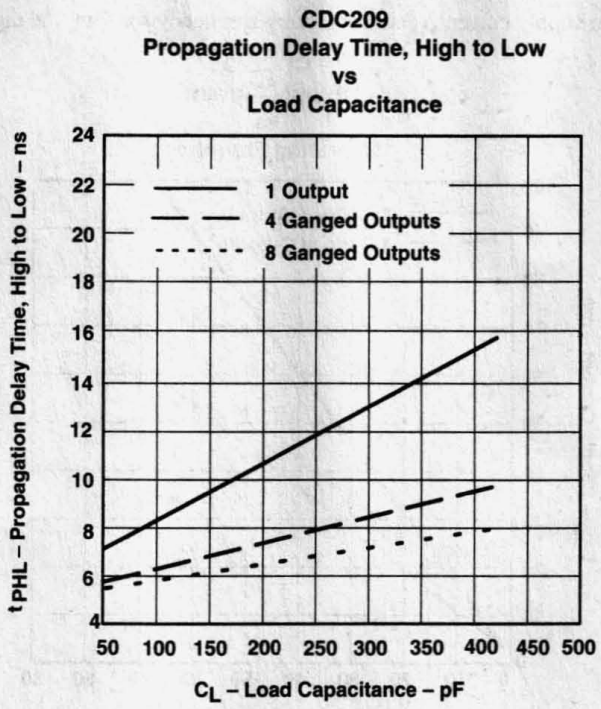


Figure 5. CDC209 t_{PHL} vs C_{LOAD}

Figure 6 shows the difference in output waveforms of a CDC209 for one, four, and eight ganged outputs driving a 470-pF load in parallel with 500 Ω.

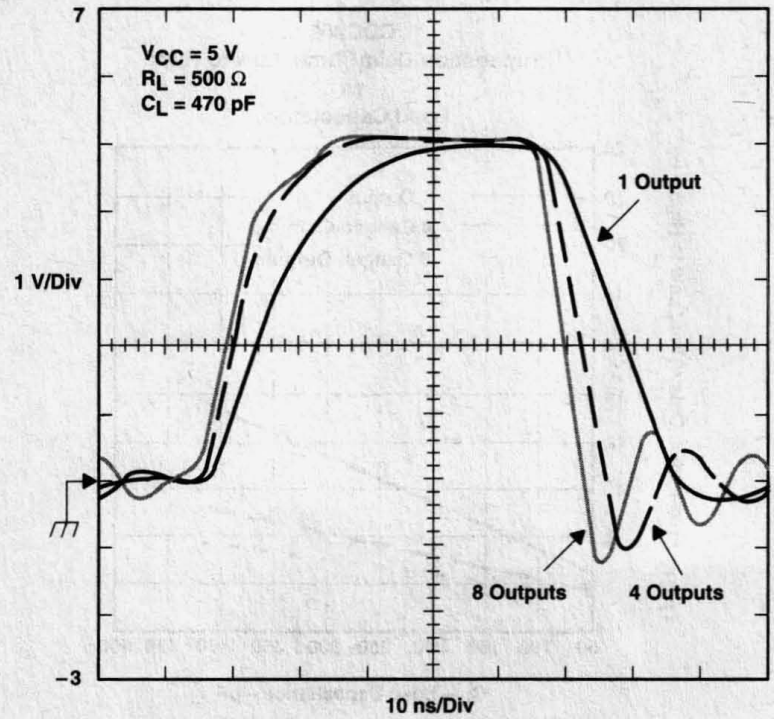
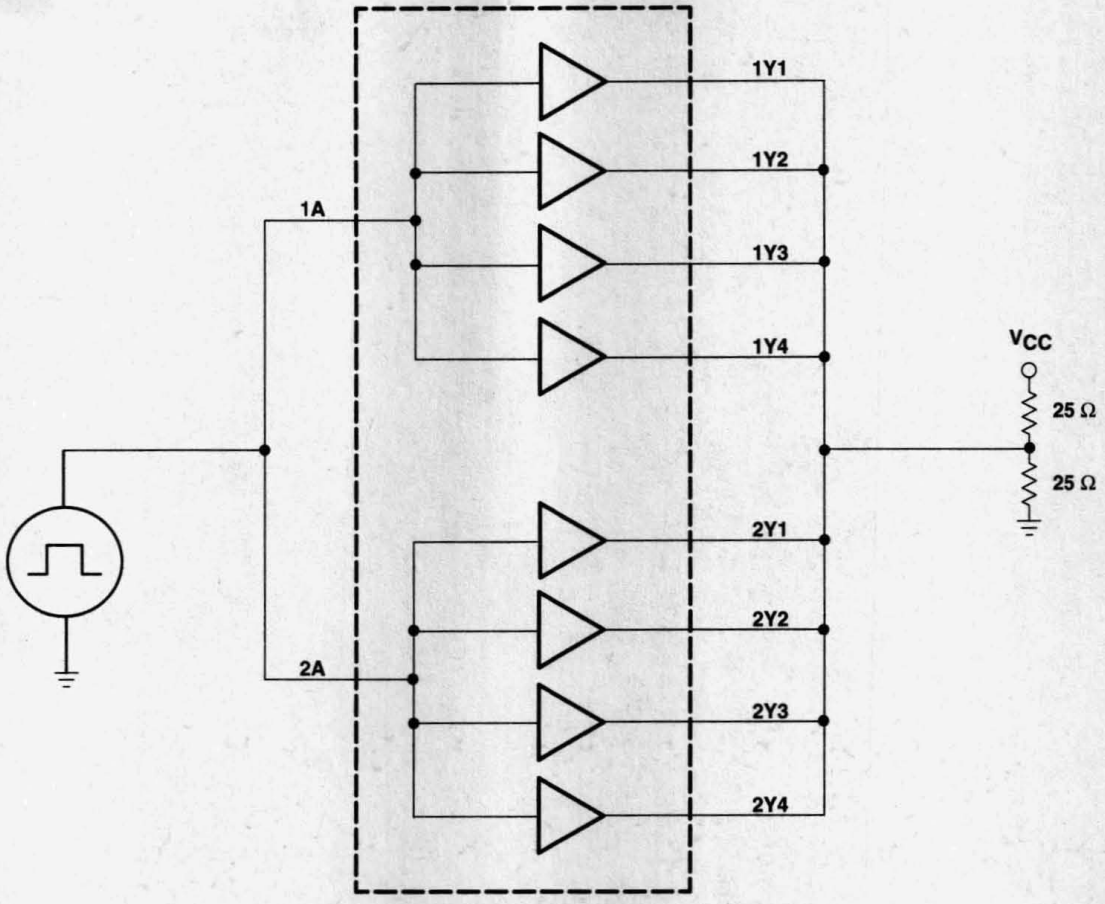


Figure 6. CDC209 Output Waveforms

Reliability

A life test of 1000 hours was also performed on 52 devices using the circuit shown in Figure 7. No failures were observed.



NOTES: A. Life test conditions: V_{CC} = 7 V, T_A = 150°C, input frequency = 10 MHz
B. It is very important to keep all of the input and output transmission lines equal length to prevent skew from being introduced.

Figure 7. Test Circuit

Applications

One application for ganged outputs is a backplane or bus on a motherboard. A backplane usually requires a single system clock capable of driving multiple plug-in boards. Ganged outputs are very effective at driving capacitive loads distributed along a single transmission line.

Great care must be taken when connecting more than one output to a single transmission line. The length and impedance of the transmission lines from each output to the point of intersection must be matched. The same attention must be given to the input traces if the outputs are driven from multiple inputs. If the lengths and impedances are not matched, a shelf may be visible in the output waveform.

Acknowledgment

The author of this report is Brett Clark.

Phase-Lock Loop-Based (PLL) Clock Driver: A Critical Look at Benefits Versus Costs

SCAA033A
March 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**6–63**
Benefits of Phase-Lock Loops (PLLs)	**6–63**
Drawbacks to Phase-Lock Loops (PLLs)	**6–66**
Conclusion	**6–66**
Acknowledgment	**6–66**
References	**6–66**

Pentium is a trademark of Intel Corporation.

Introduction

Today, system clock frequencies continue to increase and are now approaching the 66-MHz to 100-MHz range. The clock period with which systems designers must work is shrinking, as is the tolerance for high propagation delays (t_{pd}) and high output skew ($t_{sk(o)}$, $t_{sk(p)}$, and $t_{sk(pr)}$) in clock-distribution systems (see Table 1):

$t_{sk(o)}$ is output-to-output skew in the same device.

$t_{sk(p)}$ is the difference between the low-to-high and high-to-low transition for a given output terminal, that is, $t_{sk(p)} = |t_{PHL} - t_{PLH}|$

Table 1. Clock-Driver Timing Requirements

	SYSTEM CLOCK		
	50 MHz	66 MHz	100 MHz
Clock cycle time, t_c†	20 ns	15 ns	10 ns
Clock pulse duration, t_w‡	10 ns	7.5 ns	5 ns

† Clock cycle time ≥ (1/system clock frequency)
‡ Assumes a 50% duty cycle

Process skew or part-to-part skew ($t_{sk(pr)}$/$t_{sk(pv)}$) is a measure of the difference between the minimum low-to-high or high-to-low transition and the maximum high-to-low or low-to-high transition on the same terminal of two different clock drivers under the same operating conditions:

$$t_{sk(pv)} = |\min t_{pd}LH \text{ (device 1)} - \max t_{pd}HL \text{ (device 2)}| \quad (1)$$

Some manufacturers specify this parameter as:

$$t_{sk(pv)} = |\min t_{pd}LH \text{ (device 1)} - \max t_{pd}LH \text{ (device 2)}| \quad (2)$$

This is a less-stringent specification.

These timing requirements imply that the t_{PLH} and t_{PHL} through the clock buffer and the maximum allowable output skews $t_{sk(o)}$ and $t_{sk(pr)}$ in a given system need to be less than or equal to the clock-pulse duration to not violate system timing specifications:

$$\left|t_{PLH} + t_{PHL} + t_{sk(o)} + t_{sk(pr)}\right| \quad (3)$$

NOTE:
Maximum allowable $t_{sk(o)}$ for a 50% duty-cycle clock system is 10% of the clock cycle time. This is an estimate.

Benefits of Phase-Lock Loops (PLLs)

Many of the fastest gate- and buffer-based clock-distribution devices cannot meet this timing requirement. A system designer must, therefore, turn to a PLL-based clock driver as shown in Figure 1.

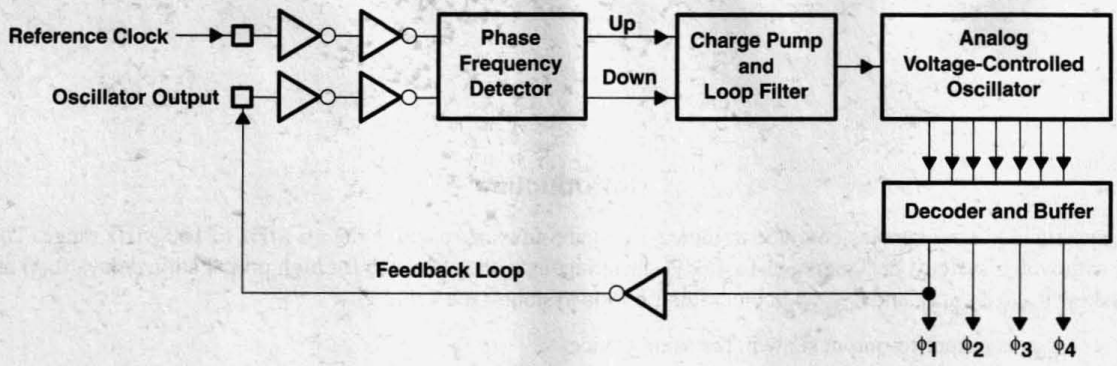


Figure 1. Block Diagram of a Clock Generator Based on a Charge-Pump PLL

The advantage of phase-lock loops is that they receive an input signal, compare this to the feedback of their internal clock generated by a voltage-controlled oscillator (VCO), and adjust the VCO by way of the charge pump to match the new input frequency and synchronize the internal and external clocks.

The analog VCO in Figure 1 is either a ring-oscillator type or a multivibrator type. The VCO can also be designed using a multistage tapped delay line that is calibrated to a precise delay per stage (a digital approach). The charge-pump design has various approaches using inverters, switches, and a passive RC low-pass filter. The phase detector is the second most-important element (see Figure 2). The input from the external clock enters the phase detector, which is a set of balancing buffers and highly balanced D-type flip-flops. The phase detector must always be active. This clock input is compared to feedback input D from the VCO.

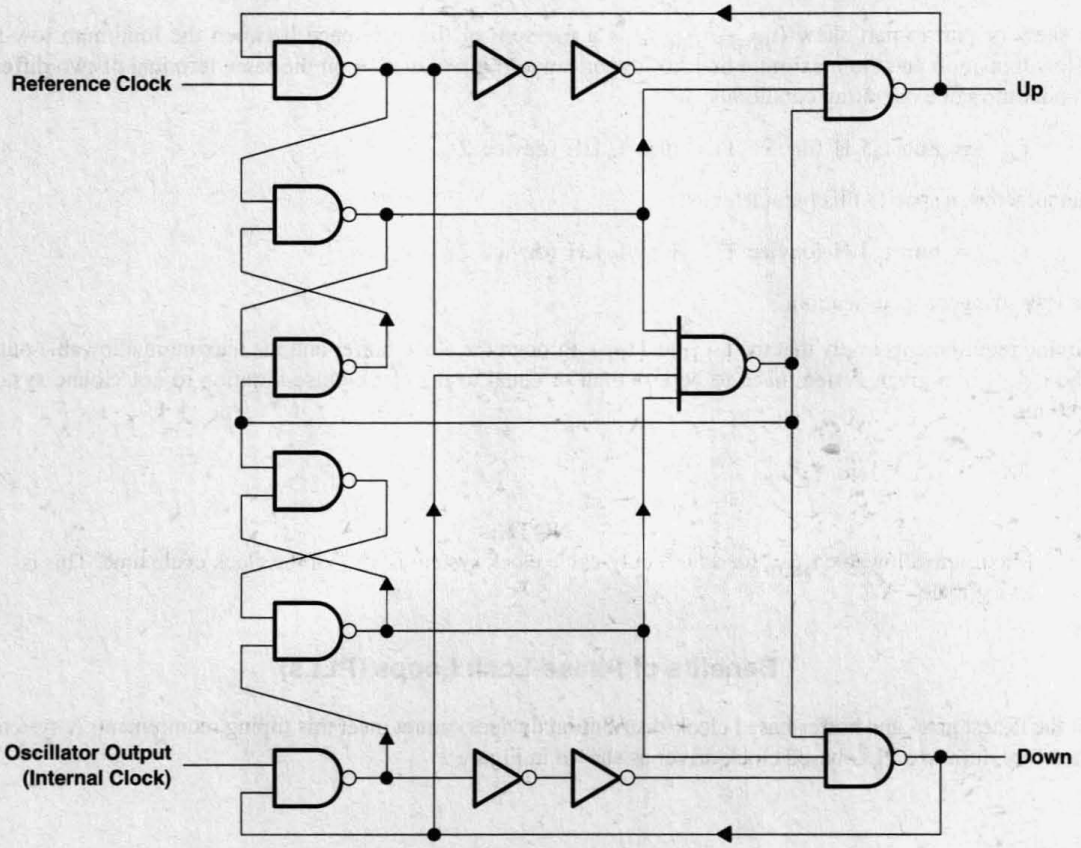


Figure 2. Phase-Detector Block

If the D input to the flip-flop is high before the rising edge of the clock, D is phase advanced, the voltage to the VCO is reduced via the charge pump, and the internal clock is slowed.

If the D input to the flip-flop is low before the rising edge of the clock, D is phase retarded and the voltage to the VCO is increased through the charge pump to speed up the VCO.

This process is repeated with every external input-clock pulse so that the feedback clock and the external clock are synchronized; the circuit then locks onto itself within a narrow frequency band. If the input clock varies slightly (within that frequency band), the PLL frequency does not vary. This narrow frequency band is known as the *dead zone* of the phase detector. Within this zone, the feedback clock and the external clock are so close in phase that there are no correction pulses out of the phase-detector circuit. Once the phase drifts out of this frequency band, the phase detector starts correcting again.

Circuit designers have tried to design nondead zone phase detectors such that the phase detector is always active and correcting. This, however, is very difficult to implement due to t_{jitter}, an important specification that results from the phase-detector circuit and noise in the VCO:

t_{jitter} of the phase detector = dead zone + correction pulse

The phase detector must be very accurate and balanced to reduce the dead zone and keep the correction pulses small. The design result is a more analog than digital implementation.

The phase-lock loop locks in a very short time (less than 50 ms). In fact, after lock, many PLL-based clock drivers are termed *zero delay*. The reality is that most have a t_{pd} of ±500 ps from the input frequencies, with a lower t_{pd} (i.e., ±150 ps) available soon. Comparing this to the 3-ns to 12-ns t_{pd} of other gate-based or divider clock drivers, there is a great advantage for a designer of high-performance systems to use a PLL-based clock driver.

Another feature of a PLL is the skew control of the device. Since the input signal is locked onto and regenerated at the output of the device, the variation of the signal from output to output is no longer a function of the chip layout and process as it is in gate- and flip-flop-based devices. PLL designs achieve maximum output skew [$t_{sk(o)}$] of 250 ps or less and process skew [$t_{sk(pr)}$] of < 1 ns, very important features from the designer's point of view.

Two other aspects of a PLL design allow for additional functionality. One of these is external feedback (not all PLL devices have this). This allows a designer to use an external gate- or flip-flop-based clock driver to drive multiple loads from one PLL output. The PLL output drives the input of the external clock driver and, by feeding one output of that external buffer back into the PLL-based clock driver through the feedback terminal, the remaining PLL outputs can be synchronized with the remaining external buffer outputs and the input clock to the PLL-based clock driver. The other aspect is output jitter (t_{jitter}). Jitter occurs when a signal deviates in phase or frequency from that of an ideal clock. This shows up as phase noise on the outputs of the device. When a PLL locks into the input frequency, there is a limited variation of that signal at the outputs. This provides for good low-t_{jitter} specifications both on individual outputs and the entire device.

Multiple-board systems derive a great benefit from this feature. A designer can use a master PLL based on a motherboard and synchronize the other boards in the system by driving the oscillator signal through the master PLL and out through the backplane, then recovering it on each of the boards via a PLL-based clock driver on each of the system boards. This works best because the master PLL has the lowest signal loss/output skew and can have high-drive outputs.

NOTE:

If one PLL is used to drive another PLL, the downstream PLL must have a greater loop bandwidth to track the output of the upstream PLL ($BW_{PLL2} > BW_{PLL1}$).

Each system board is then synchronized to the master clock, and each board individually drives the clock via its own clock driver. This application also works best when the oscillator signal is divided down, driven across the backplane, and multiplied back up through the clock recovery PLLs to the system operating frequency desired across all of the boards. By reducing the clock frequency driven across the backplane, the level of extraneous noise in the signal is also reduced.

Drawbacks to Phase-Lock Loops (PLLs)

The main drawback to the PLL-based clock driver is cost, although some PLLs are priced very competitively with buffer solutions. Due to the complexity of the circuitry and speeds at which the VCO must run, PLLs are expensive. In general, a PLL-based clock driver costs two to five times as much as a gate-based clock driver. This price is based upon the value of the product. If the accuracy and speed of the PLL is not needed, other solutions can be used.

Other disadvantages of PLLs are:

- They are inherently noise sensitive.
- Some PLLs can require expensive, high-quality external components to implement the loop-filter design.
- The external loop filter might have to be modified from part to part due to processing variations in a vendor's PLL silicon. (None of the Texas Instruments (TI) PLLs require external loop components).
- t_{jitter} can also occur due to substrate conditions. Isolation of key components such as the VCO and charge pump from the outputs and on-chip digital circuitry can reduce t_{jitter}. t_{jitter} is increased if an external feedback terminal is implemented in the design along with the reference-clock terminal. If the feedback terminal is tied to a separate V_{CC} and ground from the analog circuitry, it can increase jitter by shifting rail and ground levels between the feedback and the analog VCO and reference input. This can be remedied by tying the feedback terminals/clock input/VCO/charge pump to the same V_{CC} and ground.

Conclusion

TI has developed a group of three low-voltage, high-performance, PLL-based clock drivers. These devices are targeted at the high-performance (66–100 MHz), 3.3-V power-supply markets for RISC processors, Intel Pentium™ microprocessors, and synchronous DRAMs.

Each of these markets requires multiple outputs, 12 on each device, and a way to configure the device outputs to be one-half the input frequency, two times the input frequency, and the same frequency at the input frequency. Some of the devices also incorporate damping resistors on the outputs to reduce reflections caused by transmission-line effects and increase the integrity of the signal at the load.

The TI devices incorporate a five-stage ring oscillator VCO, and internal loop filter, and an external feedback terminal (which allows for doubling the input-clock frequency at the outputs). The VCO, charge pump, reference-clock input, and feedback terminal are all tied to the same V_{CC} and GND and fully isolated from the remaining on-chip logic and outputs of the device.

This design is inherently stable and exhibits low t_{jitter} on each of its outputs. Measured t_{jitter} in SPICE simulation is 48 ps or less, with a typical value of 23 ps.

The CDC2582, CDC2586, and CDC586 are very competitive solutions for the telecommunications, workstation, and PC-equipment clock-distribution requirements.

Acknowledgment

The author of this report, Stevan Plote, acknowledges the contribution of Ten Eyck for suggestions and design work, Brett Clark for his dedicated laboratory work, and Craig Spurlin for his design work.

Revised by Nayan Patel in March 1997.

References

Jeong, Deog-Kyoon, Gaetano Borriello, David Hodges, and Randy Katz, "Design of PLL Based Clock Generation Circuits," *IEEE Journal of Solid-State Circuits*, Vol. 22, No. 2, April 1987.

Manasce, Victor, and Steve Sadler, "A Fully Digital Phase Locked Loop," Bell Northern Research.

Young, Ian, Jeffrey Greason, and Ken Wong, "A PLL Clock Generator With 5 to 110 MHz of Lock Range for Microprocessors," *IEEE Journal of Solid-State Circuits*, Vol. 27, No. 11, November 1992.

General Design Considerations 1
Backplane Design 2
Device-Specific Design Aspects 3
5-V Logic Design 4
3.3-V Logic Design 5
Clock-Distribution Circuits (CDC) 6
Boundary-Scan IEEE Std 1149.1 (JTAG) Logic 7
Packaging 8
Index 9

Contents

	Page
Boundary Scan Speeds Static Memory Tests	7–3
Design-For-Test Analysis of a Buffered SDRAM DIMM	7–13
Hierarchically Accessing 1149.1 Applications in a System Environment	7–29
JTAG/IEEE 1149.1 Design Considerations	7–41
A Look at Boundary Scan From a Designer's Perspective	7–57
Partitioning Designs With 1149.1 Scan Capabilities	7–73
A Proposed Method of Accessing 1149.1 in a Backplane Environment	7–87
Built-In Self-Test (BIST) Using Boundary Scan	7–101
Design Tradeoffs When Implementing IEEE 1149.1	7–113
Impact of JTAG/1149.1 Testability on Reliability	7–127
System Testability Using Standard Logic	7–139
What's an LFSR?	7–155

Boundary Scan Speeds Static Memory Tests

Jim Coleman and Richard Thorpe
Texas Instruments Incorporated
Semiconductor Group

SCTA030
Reprinted with permission from Electronic Design, February 8, 1993.
Copyright 1993, Penton Publishing Inc.

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1993, Texas Instruments Incorporated

Reprinted from ELECTRONIC DESIGN February 1993

DESIGN APPLICATIONS

BOUNDARY SCAN SPEEDS STATIC MEMORY TESTS

THE BOUNDARY-SCAN STANDARD CAN SUPPLY ACCESS NEEDED TO CONTROL BUILT-IN SELF-TEST FUNCTIONS.

JIM COLEMAN and RICHARD THORPE
Texas Instruments Inc., Semiconductor Group, Test Technology Center, 6500 Chase Oaks Blvd., MS 8407, Plano, TX 75086; (214) 575-2577.

The steady increase in memory densities used in microprocessor-based systems has stretched functional test times, as large memories require time-consuming tests for adequate fault coverage. Moreover, using high-density ASICs with embedded memory limits physical test access. Wide buses and high bus fan out further complicate testing by limiting component fault isolation. Fortunately, the IEEE-1149.1 boundary-scan standard offers a solution to the problem of testing static memory.

The boundary-scan standard was initially conceived to test board interconnections without the need for physical probing. The standard requires the inclusion of boundary-scan functions on ICs, and its success is evidenced by willingness of silicon vendors to add that capability to their new products. Boundary-scan devices available now include general microprocessors, digital-signal processors, field-programmable gate arrays, ASIC libraries (standard cell and gate arrays), and bus-interface components.

Designers of microprocessor-based applications typically buffer the processor's address and data buses to solve electrical loading or isolation problems. If the bus-interface parts are IEEE-1149.1 compatible, then boundary-scan functions can be used to test the memory.

One technique uses boundary-scan instructions to scan in the address value and the data value, set a memory strobe active to perform the memory access, and set the memory strobe inactive to complete the cycle. Because these multiple-scan steps must be done for each memory address, this technique is very scan-intensive and therefore very time consuming. For extremely large memory arrays, the process could require millions of IEEE-1149.1 scan operations and take hundreds of minutes to perform.

A better solution, which can speed up test execution time by a factor of hundreds, employs IEEE-1149.1-controlled built-in self-test (BIST) with off-the-shelf components or ASIC macros. With either method, the fault detection and isolation provided by a given memory test will depend on the stimulus patterns used. To compare the two techniques, a 256-by-8-bit memory array and associated bus-interface and control logic was constructed *(Fig. 1)*. This configuration allows for explicit read/write operations using the IEEE-1149.1 Extest and Sample instructions. The IEEE-1149.1 components, which have a BIST capability controlled by boundary-scan methods, can also perform the memory read/write operations.

Two tests were run on the memory. The first explicitly scanned in the RAM array address, data, and strobe signal; the second executed IEEE-1149.1-controlled BIST, which generated the address, data, and strobe signals automatically at the test clock (TCK) rate of 6.25 MHz. The boundary-scan technique solved the problem of direct physical access, but was time consuming *(Table 1)*. The second test, however, clearly showed the advantage of IEEE-

TABLE 1: BOUNDARY SCAN VERSUS CONTROLLED BIST

Mode	256 accesses	1,000,000 accesses
IEEE 1149.1 (Extest & Sample)		
Time to apply	4.8 sec.	332.00 min.
Scans	512	2,000,000
Patterns	512	2,000,000
IEEE 1149.1 (with BIST capability)		
Time to apply	0.011 sec.	0.75 min.
Scans	7	28,000
Patterns	512	2,000,000

BOUNDARY-SCAN MEMORY TESTS

1149.1-controlled BIST. That is, by using IEEE-1149.1-controlled BIST circuitry embedded within the functional logic surrounding large memory arrays, designers can closely emulate the actual functional characteristics and timing speeds of the memory being accessed.

This article describes how to implement this solution using Texas Instruments Scope bus-interface components. These are off-the-shelf devices that offer the IEEE-1149.1-controlled BIST functionality needed to test static memory. The Scope devices also supply the electrical signal conditioning and buffering a design engineer would typically design around a microprocessor.

Generating Patterns

First, a few comments regarding deterministic and algorithmic patterns. Using algorithmically generated patterns for memory-array tests is an accepted engineering practice commonly used in software-based built-in test (BIT) code. Deterministic patterns that can't be generated with a BIST algorithmic circuit would require more memory to store the patterns than the memory array that's being tested.

Various memory-testing algorithms are available. Each technique specializes in detecting and isolating particular memory faults. Once the engineer analyzes the memory fault classes and testing approaches applicable to a given design, the appropriate BIST structures can be integrated into the processor, ASIC, or bus-interface components.

The size of the memory array is important in determining the desired width of the BIST structure bounding the address and data buses. An octal bus-interface component can generate only 256 unique patterns from its BIST circuit. So, if two 8-bit octals are used on a 16-bit bus, the BIST must be executed 256 times to cover a 64-kbit memory space.

The Scope 8-bit octal bus interface components provide flexible, generic types of BIST structures that support several memory-testing algorithms. The 8-bit biCMOS technology (BCT) devices have BIST structures for pseudo-random pattern generation (PRPG), parallel signature analysis (PSA), concurrent PSA/PRPG, and Toggle/Sample. The 8-bit advanced biCMOS technology (ABT) versions have the same capabilities as the BCT parts, and add a Count-up (256 patterns) function at the outputs. The 18- and 20-bit Widebus Scope bus interface components generate 256-kbit and 1-Mbit unique patterns, respectively, in one BIST execution. These parts also have advanced BIST capabilities, including the Count-up function of the ABT devices.

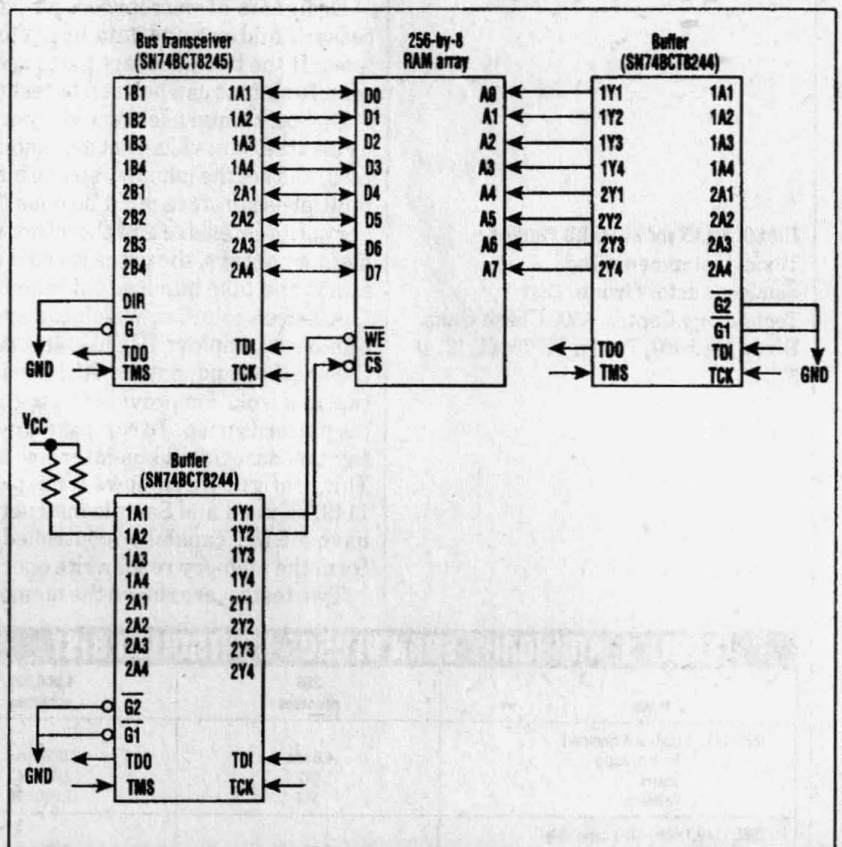
TABLE 2: SCAN SEQUENCE FOR PRPG

Step	Type	Data scanned into device	Register accessed
1	IR scan	READBN opcode	Instruction
2	DR scan	Initial seed (16 bits)	Boundary register
3	IR scan	SCANCN opcode	Instruction
4	DR scan	b'01' (PRPG)	Boundary control
5	IR scan	Runt opcode	Instruction
6	IR scan	Bypass opcode	Instruction

The example circuit uses the BCT octal bus interface components, so a review of their BIST functions is appropriate at this point. Specifically, the following descriptions of PRPG, PSA, combined PSA/PRPG, and Toggle/Sample patterns apply to the BCT8240, BCT8244, BCT8245, BCT8373, and BCT8374.

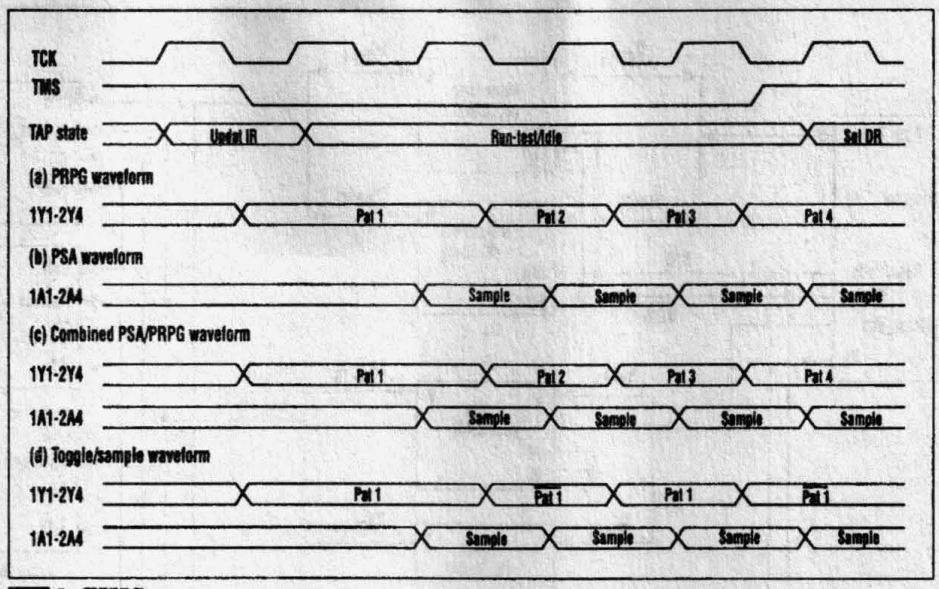
For PRPG, the patterns are generated at the functional outputs. The user should select an initial seed value and scan it into the boundary-scan register before performing the scanning sequence required to place the device into PRPG *(Table 2)*. After the Instruction Register (IR) scan of step 5 is completed and the test access port (TAP) has entered the Run-Test/Idle state, the device outputs begin generating pseudo-random patterns.

The timing relationship of these patterns to TCK and test mode select



1. A SIMPLE CIRCUIT CONSISTING of a memory array and associated bus-interface and control logic was constructed in order to evaluate two memory test methods.

BOUNDARY-SCAN MEMORY TESTS



2. THIS timing diagram shows the relationship between the IEEE-1149.1 signals—TCK, TMS, and TAP state—and the different types of test data signals that can be used to test the memory.

(TMS) is given in Figure 2a. The Scope octal's outputs change value after the falling edge of TCK while the TAP is in Run-Test/Idle and the current instruction register is loaded with the instruction Runt.

All Scope octals use an internal 16-bit linear feedback shift register (LFSR) for PRPG. The devices must receive a total of 65,535 TCKs in order to generate every sequence combination of 8-bit (octal) output values. The sequence of these values is pseudo-random, based on the initial seed value written into the boundary-scan register. The seed can be any value between x0001 and xFFFF. A seed of x0000 causes the LFSR to remain at x0000. After 65,535 TCKs, the output pattern sequence begins to repeat.

The 16-bit PRPG function can be used to generate input patterns for the data bus when performing memory write operations. This function would not normally be used for generating address patterns because it would take more than 256 TCKs to ensure that all 256 memory locations were accessed.

USING PSA

When the PSA function is used, data appearing on the eight functional data inputs is compressed into a 16-bit signature. As with PRPG, an initial seed value must be scanned into the boundary-scan register before the scanning sequence required to place the device into PSA is performed *(Table 3)*. The compression occurs after the IR scan of step 5 is completed and the TAP enters the Run-Test/Idle state.

The timing relationship of the data sampling to TCK is shown in Figure 2b. The A-inputs of the Scope octal devices are sampled on the rising edge of TCK, while the TAP is in Run-Test/Idle and the current instruction register is loaded with the instruction Runt.

The PSA function uses the 16-bit LFSR to generate the 16-bit signature, based on the initial seed value loaded in the boundary-scan register. The 16-bit seed can be any value between x0000 and xFFFF. The seed value chosen will affect the validity of the signature and the detection of faulty patterns. Therefore, the engineer should carefully study the nature of the LFSR's signature analysis in order to understand aliasing conditions. Aliasing occurs when multiple input-pattern combinations produce the same final signature. If that happens, certain memory data faults could be masked and thus go undetected.

The PSA mode would typically be used when verifying the validity of known data previously written to a block of memory. Using the 16-bit PSA function of a Scope octal device reduces the chance of aliasing.

As noted, the Scope octals can also combine PRPG and PSA operations. In this mode, the devices simultaneously generate pseudo-random patterns on the outputs while compressing a signature on the inputs. The IEEE-1149.1 scan operations needed to set up a device for combined PSA/PRPG operation are similar to those for the PSA mode *(Table 3, again)*. One difference is that the 16-bit seed value is split into two 8-bit seeds, one for PRPG and the other for PSA (step 2). In addition, the boundary-control register should be loaded with a b'11' value (step 4). After the IR scan of step 5 is completed and the TAP enters the Run-Test/Idle state, the octal's outputs begin generating PRPG patterns and the inputs are compressed. The timing relationship of these operations to TCK is shown in Figure 2c.

Because the two 8-bit seeds split the 16-bit LFSR, only 255 TCKs are required to generate every PRPG output value, and the device generates only an 8-bit PSA signature. After 255 TCKs, the output PRPG sequence repeats itself. Because of the nature of an LFSR, the eight outputs will never be all zeros. Because only 8 bits of the LFSR are used for PSA, the possibility for aliasing increases. Consequently, the 8-bit PRPG func-

TABLE 3: SCAN SEQUENCE FOR PSA

Step	Type	Data scanned into device	Register accessed
1	IR scan	READBN opcode	Instruction
2	DR scan	Initial seed (16 bits)	Boundary Register
3	IR scan	SCANCN opcode	Instruction
4	DR scan	b'10' (PSA)	Boundary Control
5	IR scan	Runt opcode	Instruction
6	IR scan	READBN opcode	Instruction
7	DR scan	Resulting signature	Boundary Register

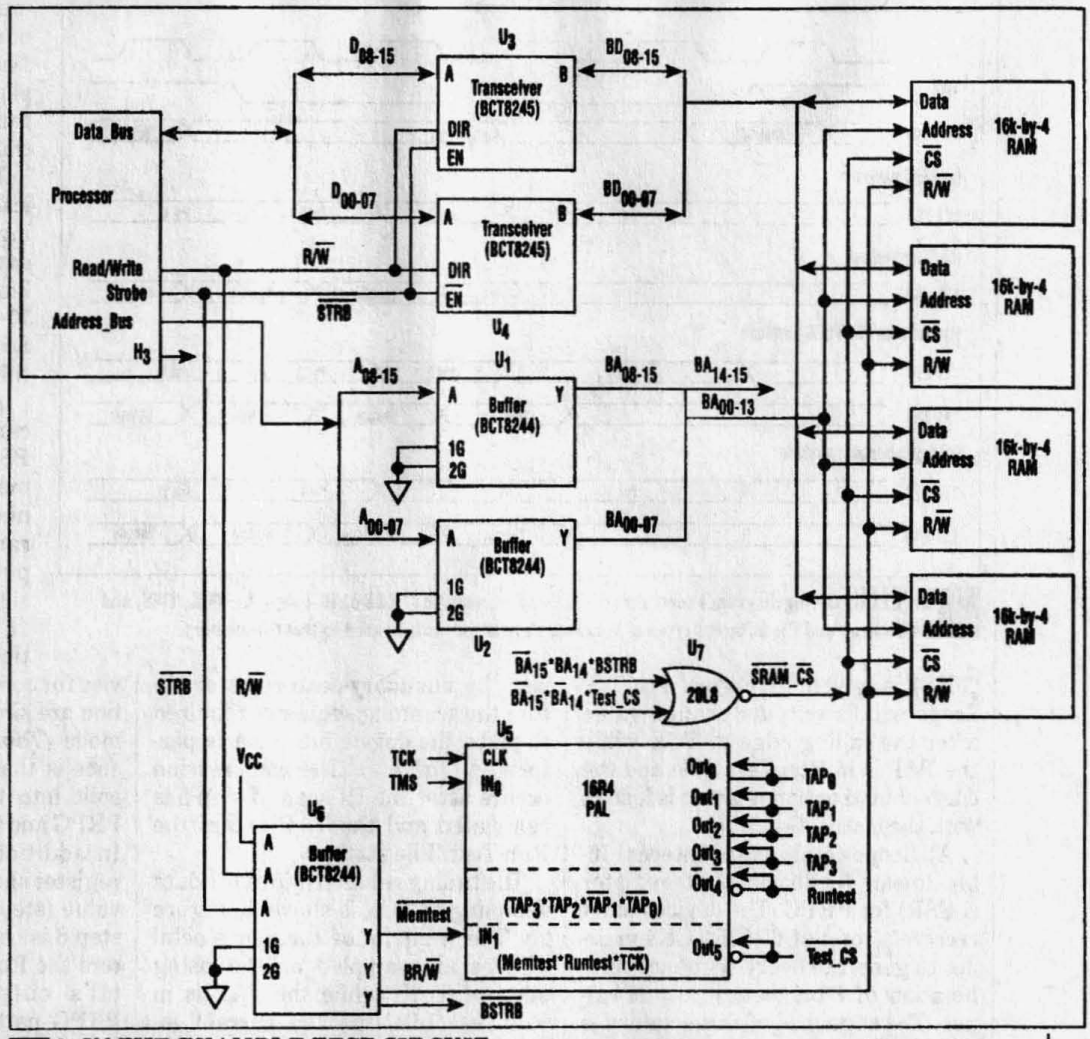
BOUNDARY-SCAN MEMORY TESTS

tion could be used to produce memory addresses, since 255 address values can be generated within 255 TCKs. But the 8-bit PSA function would not be recommended for sampling memory data because of the greater possibility of aliasing.

In the Toggle/Sample mode, the octal device generates a toggle pattern at the functional outputs while the inputs are sampled. Once again, the scan operations used to set up the octal for Toggle/Sample mode are similar to those for PSA setup. Two 8-bit seeds are entered (step 2). The first is the initial value of the toggle pattern at the outputs, and the second isn't used. To configure the octal for this BIST function, the boundary control register should be loaded with a b'00' value (step 4). As in the other modes, the octal's outputs begin to toggle after the IR scan of step 5 is completed and the TAP enters the Run-Test/Idle state.

The timing relationship of these patterns to TCK is shown in Figure 2d. The outputs of the Scope octal change value after the falling edge of TCK, and the TAP is in Run-Test/Idle and the current instruction register is loaded with the instruction Runt. The toggling output function could also be used for generating memory data input patterns, such as 55/AA, FF/00, and so on.

An example circuit consists of a generic microprocessor, a static RAM array, two PALs, and several Scope octal ICs *(Fig. 3)*. The microprocessor has a 16-bit address bus and a 16-bit data bus, as well as read/write (R/W) and address strobe ($\overline{STRB}$) control signals. The Scope octal devices partition the address and data buses to facilitate boundary scan around the microprocessor. Specifically, U_1 and U_2 (BCT8244 types) buffer the microprocessor's address bus, and U_3 and U_4 (BCT8245 types) are transceivers on the microprocessor's data bus. U_6 (a BCT8244) buffers the processor's R/W signal and other control signals.



3. IN THE EXAMPLE TEST CIRCUIT, several bus-interface devices partition the address and data buses to facilitate boundary scan around the microprocessor.

For simplicity, the example circuit doesn't detail the data-transfer acknowledgement logic. The signal H_3 is the microprocessor's functional clock, from which all functional read/writes are timed *(Fig. 4)*.

The circuit's memory map and address decoder equation, including the buffered upper address lines, BA_{14}, and BA_{15}, are defined in Table 4. To select the memory resource to be tested by the BIST function, BA_{14} and BA_{15} must be controlled properly to generate the necessary chip select. The 20L8 PAL, U_7, generates a chip select to the RAM array, $\overline{SRAM_CS}$.

The logic equation generating $\overline{SRAM_CS}$ has two product terms

TABLE 4: MEMORY MAP AND ADDRESS DECODER

Address range BA_{00}-BA_{15}	Memory selected
0000-3FFF	Not defined
4000-7FFF	RAM array (to be tested)
8000-FFFF	Not defined

!SRAMCS = ((!BA15 & BA14 & BSTRB) # (!BA15 & BA14 & TSTCS))

BOUNDARY-SCAN MEMORY TESTS

(P-Terms). The first generates the "functional operation" chip select; the second supports IEEE-1149.1 BIST testing. When BA_{15} is a logic 0 and BA_{14} is a logic 1 and $\overline{STRB}$ is a logic 0, the output $\overline{SRAM_CS}$ is a logic 0. This enables the RAM array (via the chip-select pin).

The second term is logically ORed with the first and supports the BIST operation. U_1 (the octal that buffers the upper address bus) must be loaded with the Extest instruction and must drive the upper address lines, BA_{00-15}. The output $\overline{SRAM_CS}$ is a logic 0 when BA_{15} is a logic 0, BA_{14} is a logic 1, and $\overline{Test_CS}$ is a logic 0. The lower address lines, BA_{00-07}, are driven by U_2's PRPG BIST circuit.

The 16R4 PAL, U_5, generates the $\overline{Test_CS}$ signal at the appropriate time to allow the IEEE-1149.1 BIST functions to time properly with the RAM circuitry. This device holds three logic components.

The first logic component has two inputs—TCK and TMS. The TMS signal is sampled on every rising edge of TCK, just as in other IEEE-1149.1 devices. By sampling TMS, the PAL logic can monitor the TAP state of the IEEE-1149.1 scan bus. The TAP has 16 possible states, encoded into four outputs defined as TAP_0-TAP_3 *(Table 5)*.

The PAL's second logic component generates the output signal $\overline{Runtest}$. This signal is asserted (logic 0) whenever the TAP is in the Run-Test/Idle state. This signal, which indicates when the TAP is in Run-Test/Idle state, is important. When the TAP is in this state and the octal is loaded with the Runt instruction, the BIST circuitry generates pseudo-random patterns or compresses a PSA signature.

The third logic component actually generates the $\overline{Test_CS}$ signal. While the octals are performing the BIST in the Run-Test/Idle state, this PAL needs to know when the Runt instruction is loaded into the octals. A scannable signal, $\overline{Memtest}$, is used to accomplish this. U_6, a BCT8244 octal buffer, drives this signal.

The equation for $\overline{Test_CS}$ is:

$\overline{Test_CS}$ = (Memtest * Runtest * $\overline{TCK}$)

Software performing the IEEE-1149.1 scan operations must set the $\overline{Memtest}$ signal low at the same time that the Runt instruction is loaded into the octals performing PRPG and PSA.

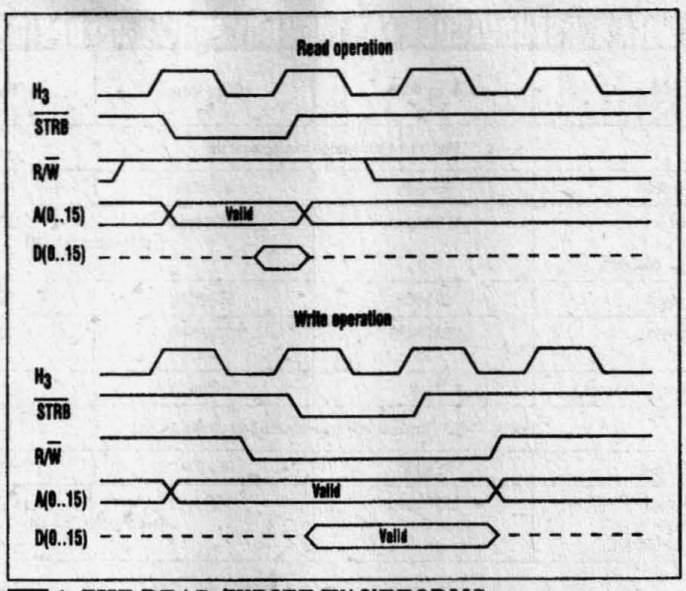
The designer must be able to shut off the microprocessor or hold it in a reset state while the test is executing. Thus, the processor should be controllable via an IEEE-1149.1 scannable register. Table 6 defines the scan operations required to perform BIST memory writes to RAM addresses 4001-40FF, using pseudo-code to generate both the address and data patterns. Device U_2 generates pseudo-random addresses on signals BA_{00-07}, and devices U_3 and U_4 generate pseudo-random data on signals BD_{00-15} *(Table 6)*.

The following steps execute the BIST memory write operation:

Step 1 loads all Scope octals with a READBN instruction, which allows access to the octal boundary-scan register (BSR) while the octals remain in their functional mode.

Step 2 involves a Data Register scan that initializes the BSRs of each octal device. U_1 (BA_{08-15}) is set up with the desired RAM memory address and U_2 (BA_{00-07}) is loaded with a PRPG seed value. Both U_3 (BD_{08-15}) and U_4 (BD_{00-07}) are loaded with a PRPG seed value. U_5 is set up with the Memtest signal asserted (logic 0), and the read/write-signal (BR/$\overline{W}$) logic level selecting a write (logic 0) operation.

Step 3 is an Instruction Register scan that loads the octals U_2, U_3, and U_4 with the SCANCN instruction. This instruction allows access to the boundary control register (BCR). U_1



4. THE READ/WRITE WAVEFORMS for the example circuit show the relationship between the microprocessor's functional clock, H_3, and the appropriate signals.

TABLE 5: DEVICE U5 TAP STATE DEFINITION

Output				
TAP_3	TAP_2	TAP_1	TAP_0	TAP State
1	1	1	1	Strap
1	1	0	0	Run-Test/Idle
0	1	1	1	Select_DR
0	1	0	0	Select_IR
0	1	1	0	Capture_DR
0	0	1	0	Shift_DR
0	0	0	1	$Exit_1$_DR
0	0	1	1	Pause_DR
0	0	0	0	$Exit_2$_DR
0	1	0	1	Update_DR
1	1	1	0	Capture_IR
1	0	1	0	Shift_IR
1	0	0	1	$Exit_1$_IR
1	0	1	1	Pause_IR
1	0	0	0	$Exit_2$_IR
1	1	0	1	Update_IR

!RUNTEST = (TAP_3 * TAP_2 * !TAP_1 * !TAP_0)

TABLE 6: PSEUDO-CODE FOR MEMORY WRITE OPERATIONS

Sequence and type	BA_{08}-BA_{15} U_1	BA_{00}-BA_{07} U_2	BD_{08}-BD_{15} U_3	BD_{00}-BD_{07} U_4	$\overline{\text{Memtest}}$ and BR/W U_5
**Shut off the embedded microprocessor					
1. IR	READBN	READBN	READBN	READBN	READBN
2. DR	$BA_{15}=0$ $BA_{14}=1$ $BA_{08\text{-}13}=000000$	LFSR seed	LFSR seed (set direction A → B)	LFSR seed	BR/W = 0 $\overline{\text{Memtest}}=0$
3. IR	Bypass	SCANCN	SCANCN	SCANCN	Bypass
4. DR	Bypass 0	PSA/PRPG 11	PSA/PRPG 11	PSA/PRPG 11	Bypass 0
5. IR	Extest	Runt	Runt	Runt	Extest
**Hold in 1149.1 Run-Test/Idle state for 255 Test Clocks (TCKs)					
6. IR	READBN	READBN	READBN	READBN	READBN
7. DR	$BA_{15}=0$ $BA_{14}=1$ $BA_{08\text{-}13}=000001$	LFSR seed	LFSR seed (set direction A → B)	LFSR seed	BR/W = 0 $\overline{\text{Memtest}}=0$

and U_5 are loaded with the Bypass instruction.

Step 4 is a Data Register scan that loads the U_2, U_3, and U_4 BCRs with the PSA/PRPG code (11).

Step 5 is an Instruction Register scan that loads U_2, U_3, and U_4 with the Runt instruction and loads U_1 and U_5 with the Extest instruction. Extest allows the previously loaded values for BA, BR/W, and $\overline{\text{Memtest}}$ to be asserted when the TAP enters the Update-IR state. When the TAP enters the Runtest/Idle state, U_2, U_3, and U_4 begin generating PRPG patterns *(Fig. 5)*.

Step 6 is an Instruction Register scan that puts the octals into their functional mode. It also deasserts U_5's Memtest signal (logic 1), preventing Test_CS from being generated when the Runtest/Idle state is reentered.

Step 7 is a Data Register scan that sets up the memory write operation for the next block of memory.

Similarly, the scan operations needed for memory read operations read from RAM addresses 4001-40FF. U_2 generates pseudo-random addresses on address bus signals $BA_{00\text{-}07}$, and devices U_3 and U_4 compress a signature from data bus signals $BD_{00\text{-}15}$ *(Table 7)*.

The following steps are required in order to execute the memory read operation:

Step 1 loads the octals with the READBN instruction, which allows access to the octal BSR while the octals remain in their functional mode.

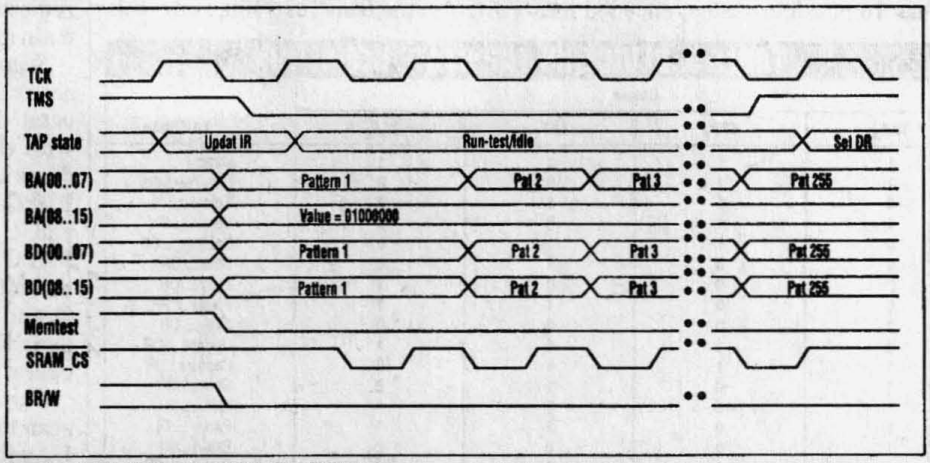
Step 2 is a Data Register scan that initializes the Scope octals' BSRs. U_1 ($BA_{08\text{-}15}$) is set up with the desired RAM memory address and U_2 ($BA_{00\text{-}07}$) is loaded with a PRPG seed value. Both U_3 ($BD_{08\text{-}15}$) and U_4 ($BD_{00\text{-}07}$) are loaded with a PSA seed value. U_5 is set up with the Memtest signal asserted (logic 0), and the read/write signal BR/W logic level selects read (logic 1).

Step 3 is an Instruction Register scan that loads octals U_2, U_3, and U_4 with the SCANCN instruction, permitting access to the boundary control register. U_1 and U_5 are loaded with the Bypass instruction.

Step 4 is a Data Register scan that loads the U_2, U_3, and U_4 boundary control register with the PSA/PRPG code (11) and PSA code (10).

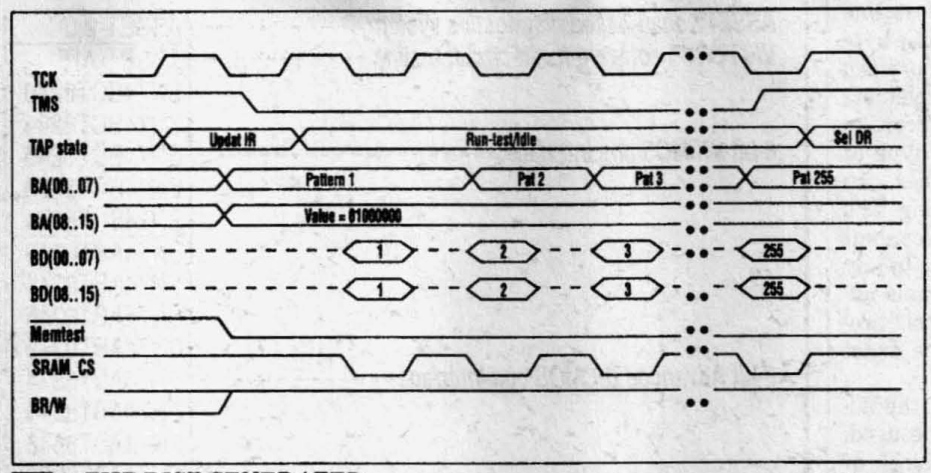
Step 5 is an Instruction Register scan that loads U_2, U_3, and U_4 with the Runt instruction and loads U_1 and U_5 with the Extest instruction. The Extest instruction allows the previously loaded values for $BA_{08\text{-}15}$, BR/W, and $\overline{\text{Memtest}}$ to be asserted when the TAP enters the Update-IR state. When the TAP enters the Runtest/Idle state, U_2 begins generating PRPG patterns and U_3 and U_4 begin compressing a signature.

Step 6 is an Instruction Register scan that puts the octals into functional mode. It also deasserts octal device U_5's Memtest signal (logic 1),



5. THE BIST-GENERATED PRPG patterns for memory write operations are created after U_2, U_3, and U_4 are loaded with the Runt instruction, and the TAP enters the Run-test/Idle state.

BOUNDARY-SCAN MEMORY TESTS



6. THE BIST-GENERATED waveforms for memory read operations are created after the Data Register scan that reads the signature from octals U_3 and U.

preventing Test_CS from being generated when the Runtest/Idle state is reentered.

Step 7 is a Data Register scan that reads the signature from octals U_3 and U_4. In adition, it sets up the memory read operation for the next block of memory.

The BIST-generated waveforms for the memory read operation are shown in Figure 6.

The designer can repeat these procedures to access other locations in the RAM array by changing the value of U_1's boundary-scan register output signals, BA_{08-13}. Because U_1 operates in the Extest mode, software has to increment and scan out each of these addresses.

During Read cycles, the data bus, BD_{00-15}, becomes valid during the assertion of SRAM_CS (after the RAM access time). The bus is sampled by devices U_3 and U_4 on the rising edge of TCK, which is when SRAM_CS is being deasserted. The address bus changes value after the falling edge of TCK (after the propagation time, TCK-to-Q valid). The calculation of the minimum TCK period must consider the address setup time, RAM access time, and the octal data setup and hold times.

OTHER CONSIDERATIONS

The 8-bit Scope octals offer two practical patterns for generating BIST addresses to a block of memory: 8-bit PRPG and Binary Count-up (for ABT parts only). The devices also supply four ways of writing data to a block of memory: 8-bit PRPG, 16-bit PRPG, Toggle, and Binary Count-up. The parts allow for reading BIST data from a block of memory by using 16-bit PSA data compression.

The use of 8-bit PRPG for address generation has a minor weakness in that it does not include address 00. Designers can ignore this shortcoming or do a separate boundary-scan procedure for address 00 in each memory block tested. The Binary Count-up algorithm accesses every address in the memory block.

One type of fault not fully covered by PRPG, or by one pass of any data pattern, is a single stuck bit in a memory cell. To guarantee detection of this fault, the test must write and read back a data pattern and its complement on two successive BIST executions. Only the Toggle algorithm can do this. The other data patterns require many more BIST operations.

Regardless of the address and data patterns used, all BIST memory blocks are read back using 16-bit PSA data compression. If the data patterns created a unique signature for each data byte within all the memory blocks, the tests should detect the general area and/or type of error. For example, if an error occurs in the same byte of every block, a data line probably has a short or an open. If all the bytes in a memory

TABLE 7: PSEUDO-CODE FOR MEMORY READ OPERATIONS

Sequence and type	BA_{08}-BA_{15} U_1	BA_{00}-BA_{07} U_2	BD_{08}-BD_{15} U_3	BD_{00}-BD_{07} U_4	$\overline{\text{Memtest}}$ and BR/W U_6
**Shut off the embedded microprocessor					
1. IR	READBN	READBN	READBN	READBN	READBN
2. DR	$BA_{15}=0$ $BA_{14}=1$ $BA_{08-13}=000000$	LFSR seed	LFSR seed (set direction B → A)	LFSR seed	BR/W = 1 $\overline{\text{Memtest}}=0$
3. IR	Bypass	SCANCN	SCANCN	SCANCN	Bypass
4. DR	Bypass 0	PSA/PRPG 11	PSA 10	PSA 10	Bypass 0
5. IR	Extest	Runt	Runt	Runt	Extest
**Hold in 1149.1 Run-Test/Idle state for 255 Test Clocks (TCKs)					
6. IR	READBN	READBN	READBN	READBN	READBN
7. DR	$BA_{15}=0$ $BA_{14}=1$ $BA_{08-13}=000001$		Read signature (and load next LFSR seed)	Read signature	BR/W = 1 $\overline{\text{Memtest}}=0$

BOUNDARY-SCAN MEMORY TESTS

block are in error, an address line may have a problem. If only one byte in a block has a error, a memory cell may be bad, especially if complementary data does not cause an error.

Once the general area or type of error is known, the designer can write a simple program using TI's Asset boundary-scan development tools that will read and write to any selected address. Using various addresses and data patterns, this program can help determine the exact location of the problem.

For larger memory arrays, the Widebus interface parts can be used. These parts allow a larger block of data (up to 65,536 addresses) to be tested in one BIST execution. Also, one device can generate or read two data bytes. Although this capability increases test speed, it reduces resolution in locating a particular fault.

The techniques discussed in this article are for testing of static devices (RAM, ROM, EPROM, etc.). However, with some minor changes depending on the type of device being tested, similar methods can be used to test dynamic RAMs. The main consideration is the refresh cycle time required by the DRAM. One alternative is to make the BIST for each memory block short enough that a burst refresh before and after each BIST can keep the memory refreshed. Another technique is to design the address generator part of the BIST circuit so that it is tied to all the DRAM row-address lines. Then the DRAM will be refreshed automatically while the BIST is running.

Jim Coleman, hardware development manager for Texas Instruments Semiconductor Group's Test Technology Center, received a BS in computer engineering from the Rochester Institute of Technology, Rochester, N.Y.

Richard Thorpe, a member of the group technical staff for the Test Technology Center, holds a BS and MS in electrical engineering from the University of Texas at Austin.

TEXAS INSTRUMENTS

TI SCOPE™ Family of JTAG/IEEE 1149.1
Boundary Scan Testability Products

ASSET™ scan-based diagnostics system	ASSET-2.0
VICTORY™ software for in-circuit testing	ASSET-AIT
8-bit BiCMOS bus interface	SN74BCT8240 SN74BCT8244 SN74BCT8245 SN74BCT8373 SN74BCT8374
8-bit Advanced BiCMOS bus interface	SN74ABT8240 SN74ABT8244 SN74ABT8245 SN74ABT8373 SN74ABT8374 SN74ABT8543 SN74ABT8646 SN74ABT8652 SN74ABT8952
18- and 20-bit wide Advanced BiCMOS bus interface	SN74ABT18245 SN74ABT18502 SN74ABT18504 SN74ABT18640 SN74ABT18646 SN74ABT18652
3.3 Volt 18- and 20-bit wide bus interface	SN74LVT18245 SN74LVT18502 SN74LVT18504
Futurebus+ Chipset	TFB2002 TFB2010 TFB2022
microSPARC™ - RISC microprocessor	TMS390S10
SuperSPARC™ - superscalar RISC microprocessor and cache controller	TMS390Z50 TMS390Z55
Parallel-processing, 32-bit, floating-point DSP	TMS320C40
High-performance, 16-bit, fixed-point DSPs	TMS320C50 TMS320C51 TMS320C52 TMS320C53
Field-programmable gate arrays (FPGAs)	TPC12xx
CMOS Gate Arrays	TEC1000 TEC1000LV TGC1000 TGC1000LV
BiCMOS Gate Arrays	TEB1000 TGB1000 TGB2000 TGB2000E
Test Bus Controller	SN74ACT8990
Scan Engine™ (Test Bus Controller support software)	TBC-SE-SW
16-bit Digital Bus Monitor	SN74ACT8994
Scan Path Support Devices	SN74ACT8997 SN74ACT8999

SATR001

Copyright © 1993 by Penton Publishing, Inc., Cleveland, Ohio 44114

Design-For-Test Analysis of a Buffered SDRAM DIMM

Sri Jandhyala and Adam Ley
Semiconductor Group

SCTA027
Reprinted with permission from Proceedings of International Workshop on Memory Technology, Design and Testing, Singapore, August 13–14, 1996.
© 1996 IEEE

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	Page
Abstract	**7–17**
1 Introduction	**7–17**
2 Module Construction	**7–18**
3 Module Function	**7–18**
4 Taxonomy of Defects	**7–19**
5 Fault Models	**7–22**
6 Test Methodologies	**7–22**
7 Card-Edge Test (Module Without DFT)	**7–22**
8 Module DFT	**7–23**
9 In-Circuit Test	**7–23**
10 Boundary-Scan Test	**7–25**
10.1 Boundary Scan at Register and Clock Driver	7–25
10.2 Boundary Scan at Register Only	7–25
10.3 Boundary Scan at SDRAM ICs	7–25
10.4 Boundary Scan at Buffer	7–25
10.5 Boundary Scan: Beyond Manufacturing Test	7–25
11 Comparative Study	**7–26**
12 Conclusion	**7–26**
References	**7–27**

List of Tables

Table	Title	Page
1	Summary of Module Construction	7–18
2	Node/Solder-Joint Matrix With Card-Edge and In-Circuit Test Fault Classification	7–20
3	Defined Solder-Joint Fault Model	7–22
4	Card-Edge Test Fault Classification	7–23
5	In-Circuit Test Accessibility Classification	7–24
6	In-Circuit Test Fault Classification	7–24
7	Comparison of Test Methodologies	7–26

Abstract

This paper presents a design-for-test (DFT) analysis of a buffered synchronous dynamic random-access memory (SDRAM) dual in-line memory module (DIMM). The analysis is restricted to board-level manufacturing faults. The test problem is described, alternate test methods are suggested, and a comparative study is presented contrasting a DFT approach – including boundary-scan test – versus a non-DFT approach.

Keywords: boundary scan, design-for-test, DFT, DIMM, DRAM, IEEE Std 1149.1, in-circuit, JTAG, memory, module, SDRAM, test.

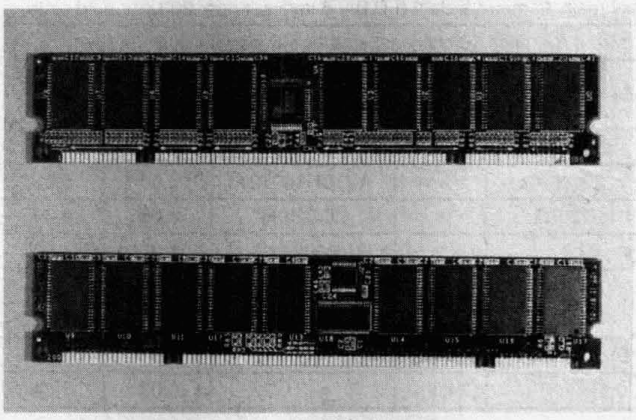


Figure 1. Subject Module (1/2X)

1. Introduction

The high quality of electronic systems being demanded by business and private consumers today is driving the growing importance that manufacturers are placing on testing as a whole. Ever-increasing miniaturization and complexity of very-large-scale integration (VLSI) integrated circuits (ICs) and systems are, in turn, leading to escalating difficulties faced by board/module manufacturers in using conventional test methods for their testing needs. The advent of new assembly technologies like fine-pitch surface-mount technology (SMT), multichip modules (MCMs), tape-automated bonding (TAB), and chip-on-board (COB) have complicated matters further.

Due to such advances, not only has it become difficult to gain physical access to probe printed-wiring-board (PWB) traces, but it has also become impractical to continue with conventional test development. With increased IC and module complexity, the high costs involved with developing test programs are recurring, as standard test programs that could be reused several times in the past, now need to be generated with a specific application in mind, due to the application-specific nature of ICs. Therefore, to maintain quality of products and increase competitive advantage while remaining economically viable, new and evolving system-level test methodologies aimed at improving overall testability must be adopted. This paper will demonstrate the applicability of such methods to a buffered SDRAM DIMM.

2. Module Construction

The analysis to be presented in this paper is based on a 200-pin, 2-bank x 2M x 72, buffered SDRAM DIMM designed at Texas Instruments (TI) according to JEDEC Standard 21-C. Figure 1 shows the subject module at half-size magnification. As shown, the module is a double-sided assembly that uses a high degree of miniaturization for both components and assembly.

The fundamental elements of the buffered SDRAM DIMM are a laminate substrate with dual-in-line edge contacts, a high-speed buffered register IC, a phase-locked-loop (PLL) clock distribution IC, several SDRAM ICs, as well as several capacitor and resistor components. Table 1 provides a summary of the module construction. As can be ascertained from this summary, all components, including passives as well as ICs, are of the fine-pitch surface-mount type.

Table 1. Summary of Module Construction

PWB							
Finished size: 1.15 in. x 6.05 in. x 0.05 in; finished cost: $10							
Substrate: glass-base epoxy resin, flame retardant (FR4) – 6 layers; edge: 200 pin, gold plate							
Wiring: copper/entek plus, size 4 mil, pitch 10 mil; vias: size 12 mil, pitch 50 mil							
ICs	**DESCRIPTION**	**NO.**	**PART NO.**	**COST $**		**PACKAGE**	**LEAD PITCH**
				UNIT	**EXT'ED**		
SDRAM	2M × 8	18	TMS626802	30.00	540.00	44-pin TSOP	0.80 mm
Buffered register	20 bit	1	ALVCH162721	5.00	5.00	56-pin TSSOP	0.50 mm
Clock driver	1-to-12 PLL	1	CDC2586	6.00	6.00	52-pin TQFP	0.65 mm
PD buffer	8 bit	1	LVC244	1.00	1.00	20-pin TSSOP	0.65 mm
PASSIVES		**NO.**		**COST $**		**PACKAGE**	**PITCH**
				UNIT	**EXT'ED**		
Shunt/tie-off resistors (0, 10)		8, 72		0.01	0.80	0603	50 mil
Bypass capacitors (0.001, 0.1)		24, 24		0.03	1.44	0603	50 mil

In the dual-bank architecture of the subject module, nine SDRAM ICs are placed on each side of the PWB. The clock driver and related passives are placed on one side of the board, while the register and buffer, along with associated passives, are placed on the other side of the board.

As noted in the construction summary, the PWB was constructed in six layers. The two outer layers were used for the data I/O and address/control buses. One inner layer was used for the clock signal routing, while another was used for routing register outputs to receiving SDRAMs on the back side. Finally, the remaining two layers were used for power (Vcc) and ground planes.

3. Module Function

The function of the subject SDRAM DIMM is shown in the block diagram of Figure 2. All address (12) and control (8) lines to the SDRAM devices are buffered and retimed through the 20-bit register. Data in/out signals are driven directly to/from the card edge via 10-ohm series damping resistors. External damping resistors are avoided on the address, clocks, and controls through the use of ICs that integrate such resistors. The single clock driver supplies buffered, phase-controlled clock signals to the register, as well as all SDRAM devices. The octal buffer sources the buffered presence-detect outputs, which provide configuration information about the DIMM. The output enable for this buffer is controlled by the presence-detect enable (PDE) signal.

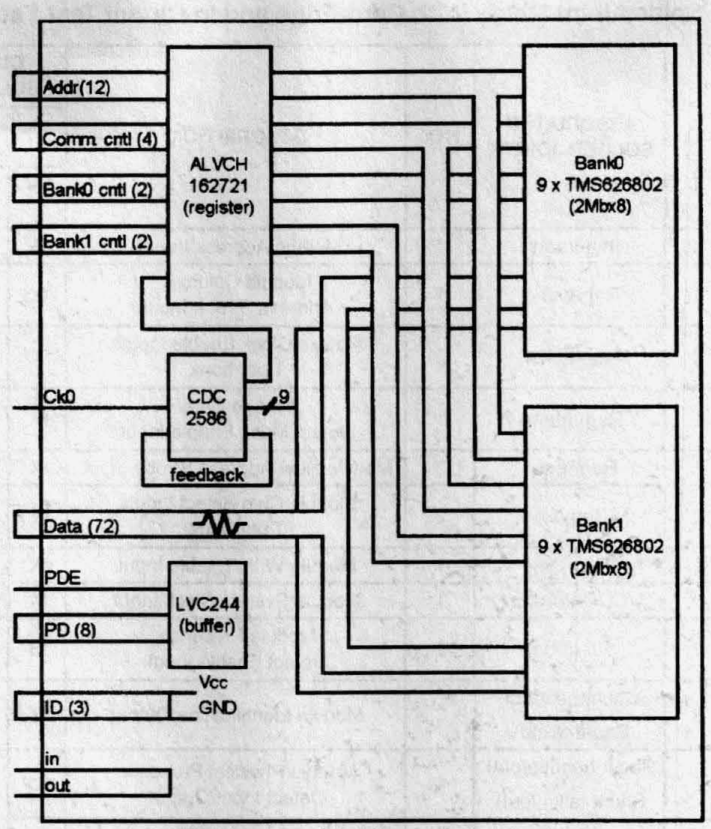


Figure 2. Module Block Diagram

4. Taxonomy of Defects

The causes for defects in a module can broadly be classified into process defects and random point defects. Process defects can result from high or abnormal variation in processing, such as in solder paste thickness, wiper pitch, etc., while point defects may result from particulate or other contamination.

Some defects that occur during the assembly process are commonly caused by manufacturing errors, such as the use of wrong components or missing components. Defects introduced during module assembly can also result from manufacturing processes, such as incorrect or insufficient paste, incorrect component placement, cold solder, solder splashes, contamination, or process damage. These may also be caused by use of defective or faulty components in the form of broken or improper leads, mislabeled parts or wrong values, or cracked components.

Regardless of their root cause, such defects can result in improper operation/function of the assembly. Therefore, testing is necessary to verify proper module function, to identify defects in faulty assemblies for rework and repair, as well as to eliminate sources of defects in the process.

A specific manifestation of a defect in an assembly is referred to as an assembly fault. These can be broadly grouped into gross and marginal classes. Marginal assembly faults are parametric in nature and deal with electrical characteristics of circuits like threshold, bias, and leakage currents and voltages. Delay faults can be classified as such. Gross assembly faults can be divided into interconnect faults, which include shorts and opens, and placement faults, which are caused by wrong component orientation or wrong part in socket.

Table 2. Node/Solder-Joint Matrix With Card-Edge and In-Circuit Test Fault Classification

SIGNAL NODES	NO.	ASSOCIATED SOLDER JOINTS	NO.	DESCRIPTION	CLASSIFICATION OF SOLDER JOINT FAULTS					ICT ACCESSIBILITY
					CARD-EDGE (NO DFT)				ICT	
					ss/ L	ss/ H	so/ L†	so/ H†	so‡	
Edge → Reg(addr)	12	Reg-I(addr)	12	Module Address Inputs	fA	fA	fA	fA	iB	a
Edge → Reg(cas)	1	Reg-I(cas)	1	Module Column-Address Strobe Input	fX	fX	fX	fX	iB	a
Edge → Reg(cke)	2	Reg-I(cke)	2	Module Clock Enable Inputs 1 per bank	fX'	fQ	fX'	fQ	iB	a
Edge → Reg(dqm)	1	Reg-I(dqm)	1	Module Data/ Output Mask Enable Input	fR	fX	fR	fX	iB	a
Edge → Reg(ras)	1	Reg-I(ras)	1	Module Row-Address Strobe Input	fX	fX	fX	fX	iB	a
Edge → Reg(s)	2	Reg-I(s)	2	Module Chip Select Inputs 1 per bank	fX'	fX'	fX'	fX'	iB	a
Edge → Reg(w)	1	Reg-I(w)	1	Module Write Enable Input	fX	fX	fX	fX	iB	a
Edge → CDC(clk)	1	CDC-I(clkin)	1	Module System Clock Input	fX	fX	fX	fX	iC	a
Edge → Buf(pde)	1	Buf-I(pde)	2	Module Presence Detect Enable Input	fS	fS	fS	fS	iS	a
Edge → Shunt(id)	3	Shunt-head(id) Shunt-tail(id)	3	Module Identification Output	fT	fT	fT	fT	iT	a x
Edge ↔ Shunt(in/out)	2	Shunt-head(in/out) Shunt-tail(in/out)	1	Module Physical Presence Detect Input/Output	fU	fU	fU	fU	iT	a
Edge ↔ SDRAM(dq):	72	Resistor-head	72	Module Data Input/Data Output All SDRAM I/Os are driven through 10-ohm resistors to/from card edge	fV	fV	fV	fV	iV	a
Edge ↔ Resistor	72	Resistor-tail	72		fV	fV	fV	fV	iV	d
Resistor ↔ SDRAM(dq)	72	SDRAM-I/O(dq)	144		fV	fV	fV	fV	iV	
Edge	8	Buf-O(pd)	4	Module Logical Presence	fW	fW	fW	fW	iB	a
				Detect Outputs	fW'	fW'	fW'	fW'		
Reg → SDRAM(addr)	12	Reg-O(addr)	12	SDRAM Address	fA	fA	fA	fA	iB	b
		SDRAM-I(addr)	216				fA'	fA'	iA'	
Reg → SDRAM(cas)	1	Reg-O(cas)	1	SDRAM Column-Address Strobe	fX	fX	fX	fX	iB	b
		SDRAM-I(cas)	18				fX'''	fX'''	iX'''	
Reg → SDRAM(cke)	2	Reg-O(cke)	2	SDRAM Clock Enable 1 per bank	fX'	fQ	fX'	fQ	iB	b
		SDRAM-I(cke)	18				fX'''	fQ'	iX'''	
Reg → SDRAM(dqm)	1	Reg-O(dqm)	1	SDRAM Data/Output Mask Enable	fR	fX	fR	fX	iB	b
		SDRAM-I(dqm)	18				fR'	fX'''	iX'''	
Reg → SDRAM(ras)	1	Reg-O(ras)	1	SDRAM Row-Address Strobe	fX	fX	fX	fX	iB	b
		SDRAM-I(ras)	18				fX'''	fX'''	iX'''	
Reg → SDRAM(s)	2	Reg-O(s)	2	SDRAM Chip Select 1 per bank	fX'	fX'	fX'	fX'	iB	b
		SDRAM-I(s)	18				fX'''	fX'''	iX'''	
Reg → SDRAM(w)	1	Reg-O(w)	1	SDRAM Write Enable	fX	fX	fX	fX	iB	b
		SDRAM-I(w)	18				fX'''	fX'''	iX'''	

n/c = not considered; n/f = no fault

† Noise injected onto open inputs may cause intermittent/unexpected results

‡ Assuming 100% node coverage

Table 2. Node/Solder-Joint Matrix With Card-Edge and In-Circuit Test Fault Classification (Continued)

SIGNAL NODES	NO.	ASSOCIATED SOLDER JOINTS	NO.	DESCRIPTION	CLASSIFICATION OF SOLDER JOINT FAULTS					ICT ACCESSIBILITY
					CARD-EDGE (NO DFT)				ICT	
					ss/ L	ss/ H	so/ L†	so/ H†	so‡	
CDC → SDRAM(clk)	9	CDC-O(clk)	9	SDRAM System Clock	fX"	fX"	fX"	fX"	iC'	b/c
		SDRAM-I(clk)	18				fX"'	fX"'	iX"'	
CDC → Reg(clk)	1	CDC-O(clk)	1	Register System Clock	fX	fX	fX	fX	iC'	b
		Reg-I(clk)							iD	
CDC → CDC(fb)	1	CDC-O(fb)	1	CDC External Feedback	fX	fX	fX	fX	iC'	b
		CDC-I(fb)							iC	
Buf ← Shunt(pd-I)	4	Buf-I(pd)	4	Buffer Input (Presence Detect) Tie-offs	fW	fW	fW	fW	iB'	d
		Shunt-head(pd)							iT	
		Shunt-tail(pd)							iT	x
		OTHER SOLDER JOINTS								
		Reg-I(clken)	1	Reg Clock Enable (to be low)	n/f	fX	n/f	fX	iD	x
		Reg-I(NC)	1	Reg No-Connect (to be low)	n/f	n/f	n/f	n/f	n/f	x
		Reg-I(oe)	1	Reg Output Enable (to be low)	n/f	fX	n/f	fX	iS	x
		CDC-I(clr)	1	CDC Clear (to be low)	n/f	n/f	n/f†	n/f†	n/f†	x
		CDC-I(NC)	1	CDC No-Connect (to be low)	n/f	n/f	n/f	n/f	n/f	x
		CDC-I(oe)	1	CDC Output Enable (to be low)	n/f	fX	n/f	fX	iS	x
		CDC-I(sel)	2	CDC Select (to be low)	n/f	fY	n/f	fY	iY	x
		CDC-I(test)	1	CDC Test (to be low)	n/f	fZ	n/f	fZ	iZ	x
		SDRAM-I(NC)	90	SDRAM No-Connect (to be low)	n/f	n/f	n/f	n/f	n/f	x
		Buf-I(pd)	4	Buf Input (Presence Detect -- to be low)	n/f	fW'	n/f	fW'	iB	x
		Reg-Power	12	Register Vcc/GND	n/c	n/c	n/c	n/c	n/c	x
		CDC-Power	32	CDC Vcc/GND	n/c	n/c	n/c	n/c	n/c	x
		SDRAM-Power	216	SDRAM Vcc/GND	n/c	n/c	n/c	n/c	n/c	x
		Buf-Power	2	Buffer Vcc/GND	n/c	n/c	n/c	n/c	n/c	x
		Cap-head	48	Bypass Capacitors	n/c	n/c	n/c	n/c	n/c	x
		Cap-tail								
TOTAL SIGNAL NODES	**214**	**TOTAL SOLDER JOINTS**	**1175**							

n/c = not considered; n/f = no fault
† Noise injected onto open inputs may cause intermittent/unexpected results
‡ Assuming 100% node coverage

Because of its construction, the module typically is subject to such manufacturing defects and consequent assembly faults. As the majority of defects in fine-pitch surface-mount assemblies, especially those associated with process rather than human error, directly affect solder joints, the analysis presented in this paper addresses that issue. Columns 1 to 5 of Table 2 enumerate the signal nodes, their associated solder joints, and other solder joints (those associated with Vcc/GND nodes) in the module.

5. Fault Models

For faults to be modeled or simulated – for coverage and diagnostic analysis among other purposes – they must be represented mathematically by abstraction through a logical model. Such logical models are called fault models. They constitute a basic set of assumptions that represent such faults. By such abstraction, the problem of modeling physical faults is reduced to a logical level that can represent the effects of physical faults on the behavior of the system. The process of fault analysis is also simplified by converting faults across several technologies into logical fault models that are independent of process.

A fault model used pervasively in many sorts of test and DFT analysis is the single-stuck-at model, in which a single defective node is presumed to behave as if it were constantly held to a static low or high level. For our analysis, this model will be extended to comprehend faults resulting from defects in solder joints.

Each solder joint can be faulty, either due to an open condition or a short condition. Thus, the single-stuck-at model is modified to cover both cases, resulting in the fault model detailed in Table 3.

Table 3. Defined Solder-Joint Fault Model

NOTATION	FAULT NAME	DESCRIPTION
ss/L	Solder-short/low	Entire associated node stuck low
ss/H	Solder-short/high	Entire associated node stuck high
so/L	Solder-open/low	Pin is stuck low, independent of associated node
so/H	Solder-open/high	Pin is stuck high, independent of associated node

6. Test Methodologies

Two categories of test are typically considered for manufacturing use:

1. Dynamic functional tests: tests defined in association with a functional and/or performance fault model. These test for faults, such as delay faults, that are associated with the performance of the system and are intended to demonstrate the suitability of the finished module to its intended function.
2. Static structural tests: tests defined in association with a structural fault model. These methods test for gross interconnectivity issues. In-circuit test (ICT) is an example of a static structural test method. The solder-open/short faults of Table 3 would be susceptible to such methods.

While the need for dynamic functional test is taken as a given, such analysis is beyond the scope of this paper. Such testing may in fact be required to detect certain classes of solder-open faults, such as those associated with bypass capacitors. However, the capability of such testing to diagnose or even detect structural defects is generally suspect. Therefore, the remaining analysis will focus exclusively on structural test goals.

7. Card-Edge Test (Module Without DFT)

As the subject module was designed solely for the purpose of demonstrating electrical performance characteristics of a buffered SDRAM DIMM, it was designed without any consideration for testability. Without such DFT, observability and controllability are limited to the primary (card edge) input/outputs (I/Os) of the module. This implies that for faults to be detected, such faults must be sensitized from the card-edge inputs and propagated through the entire module to the card-edge outputs. Diagnosis (isolation and location) of faults poses even greater difficulties, as many faults will produce the same syndrome at the primary I/Os.

The various fault syndromes resulting from modeled faults at each class of module solder joint are classified in columns 6–9 of Table 2 and defined in Table 4. The latter table also details the number of patterns and/or read/write cycles to be applied, along with a brief description of algorithms and consequent diagnostic resolution.

As shown in this analysis, many solder-joint faults produce common syndromes resulting in poor diagnostic resolution for structural faults when only card-edge access is provided.

Table 4. Card-Edge Test Fault Classification

FAULT CLASS	DESCRIPTION	NUMBER PATTERNS FOR DETECTION/ISOLATION; (ALGORITHM)	DIAGNOSTIC RESOLUTION	
			NO. COMPONENTS	NO. SOLDER JOINTS
fA	All-chip addressing fault	2 *((N+1)w + (N+1)r) = 26w + 26r; (write to all-0 addr and to all addr with only 1 logic-1 bit – read same; repeat for all-1 addr and all addr with only 1 logic-0 bit)	19	20
fA'	Single-chip addressing fault	"	1	1
fQ	Bank access-hold fault	1wb + 1rb; (CKE low during read burst for access hold)	10	11
fQ'	Single-chip access-hold fault	"	1	1
fR	All-chip access-mask fault	1wb + 1rb; (DQM high during read/write burst for data mask)	19	20
fR'	Single-chip access-mask fault	"	1	1
fS	Presence detect enable/disable fault	2; (PDE low/high)	1	1
fT	Identification output fault	1; (static output)	1	2
fU	IN/OUT fault	4; (IN low/high, OUT low/high)	1	2
fV	Dual-chip data fault	2 * 2*72(1w + 1r) = 288w + 288r; (walking-1 each bank, walking-0 each bank)	3	4
fV'	Single-chip data fault	"	1	1
fW	Presence detect output fault(1)	1; (static output)	2	4
fW'	Presence detect output fault(2)	1; (static output)	1	1
fX	All-chip gross access fault	1w + 1r; (any valid write /read access with any addr/data)	20	69
fX'	Bank gross access fault	"	10	22
fX"	Dual-chip gross access fault	"	2	3
fX"'	Single-chip gross access fault	"	1	7
fY	Clock multiply fault	2*(1wb + 1rb); (1 wb/rb to bank0, 1 wb/rb to bank1)	1	1
fZ	Clock PLL-bypass fault	1w + 1r; (at freq. which will not result in phase-lock)	1	1

8. Module DFT

Design-for-test techniques are generally based on providing greater access to the module under test for the purpose of improving the degree to which the module function can be observed and controlled. Another way of looking at DFT is that it seeks to partition the larger module function into smaller functions that are easier to test. Several techniques for this are in common use today. The two that are considered in this paper are in-circuit test (ICT) and boundary scan.

9. In-Circuit Test

ICT is based on providing physical access to probe as many module nodes as possible and on *ad-hoc* circuit techniques that allow internal nodes to be safely controlled (as well as observed) by an external tester. The resulting test fixture is commonly called a "bed of nails" (or in the case of double-sided assembly such as the subject module, a "clam shell") and the required tester consists of a large number of high-drive parallel test channels.

Generally, on fine-pitch SMT assemblies such as the subject module, provision for ICT requires placement of "test points" on which ICT probes may land. In some cases, the vias that are anyway present to route signals from outer layers to other layers may provide such test points. In other cases, vias must be added to bring signals to be accessed up from inner layer to outer layer.

Such placement of test points requires use of module "real estate" that may not be available. Generally, the finest available ICT probes (50-mil pitch) require test pads of 25 mils minimum width.

While modifications to the module layout have not been specifically implemented, the module layout has been analyzed for placement of physical test points. The results by node are presented in column 11 of Table 2 according to the accessibility classes defined in Table 5.

Table 5. In-Circuit Test Accessibility Classification

ACCESSIBILITY CLASS	DESCRIPTION
a	Accessible from module edge
b	Test points easily provided
c	Test points provided with difficulty
d	Test points difficult/impossible to provide
x	Accessible from module edge (Vcc/GND)

With test points provided at all internal nodes, the module is quite controllable at the IC level. Since all ICs on the module provide means for placing their outputs at high impedance, the tester can safely disable any ICs that are not under test. The only provision that would be required for this is to add pull-down resistors at register and clock driver output-enable pins versus the direct tie to GND that is specified for the original module.

Based on the presumed insertion of test points at all internal nodes except those in accessibility class d (quantity 31), full coverage and diagnostic of solder shorts are provided. The nodes excluded are indirectly accessible via shunt or resistor, and so their exclusion may somewhat reduce fault diagnostic, but not coverage. In case of solder opens, the consequent fault syndromes resulting at each class of module solder joint are classified in column 10 of Table 2 and are defined in Table 6. The latter table also indicates the consequent diagnostic resolution.

Table 6. In-Circuit Test Fault Classification

FAULT CLASS	DESCRIPTION	DIAGNOSTIC RESOLUTION	
		NO. COMPONENTS	NO. SOLDER JOINTS
iA'	Single-Chip Addressing Fault	1	1
iB	Buffer Data Fault	1	2
iB'	Buffer Data Fault (no access)	2	3
iC	Gross Clock Output Fault	1	2
iC'	Single Clock Output Fault	1	1
iD	Register Clock Fault	1	2
iS	Output Enable Fault	1	1
iT	Shunt/Resistor Fault	1	2
iV	Memory Data Fault	2	3
iX""	Single-Chip Gross Access Fault	1	7
iY	Clock Multiply Fault	1	1
iZ	Clock PLL-Bypass Fault	1	1

As shown, the diagnostic resolution is remarkably improved (versus card-edge test), such that all single solder-stuck faults are generally diagnosable to the component and often to the pin level. Such a diagnostic provides the information necessary to improve process and repair failed boards for subsequent shipment.

10. Boundary-Scan Test

Like ICT, boundary-scan test (BST), as standardized in IEEE Std 1149.1 (JTAG), is based on providing test access to as many module internal nodes as possible. Unlike ICT, boundary scan provides access by integrating digital test cells behind the pins of compliant ICs. Access to such boundary-scan cells for control and observation of the module is provided by a 4-wire test access port (TAP) at each compliant IC. Thus, the complex and expensive fixturing and automated test equipment (ATE) required for ICT is avoided.

10.1 Boundary Scan at Register and Clock Driver

Of the 31 internal nodes that are presumed to be ICT accessible, 21 are associated with the register (ALVCH162721) while 10 are associated with the clock driver (CDC2586). Therefore, if the register and clock driver were replaced with suitably equivalent ICs with boundary scan, all ICT-covered nodes would be boundary-scan accessible, and thus, ICT could be eliminated without any consequent loss of fault coverage or diagnostic.

Such equivalents or near equivalents to the ALVCH162721 are, or will be, available soon (such as LVTH182504A and/or ALVCH182504, at an estimated additional cost of $5). Unfortunately, the authors are unaware of any clock drivers available or planned with boundary scan. If these were available (at an estimated additional cost of $3), then boundary scan would displace ICT, while requiring off-edge physical access only to the four TAP signals and using much less expensive ATE – all at an additional component cost that is barely 1% of the total cost of module materials.

10.2 Boundary Scan at Register Only

Even with boundary scan available only in the register, controllability and observability of the SDRAM ICs is provided, with the exception of the clock signals. Observability of one output of the clock driver is also provided. Therefore, if access to the TEST input of the CDC2586 were provided, the low-cost boundary-scan tester could source the module CLKIN signal so that it would be coordinated with boundary-scan operations to perform read/write cycles to the SDRAM array. By doing so, all interconnects to the SDRAMs can be tested with the same fault coverage and diagnostic capability provided by ICT. Access to only five off-edge signals is required (four TAP signals, plus the CDC2586 TEST input).

10.3 Boundary Scan at SDRAM ICs

Boundary scan in the SDRAMs would greatly impact the overall controllability/observability of the module such that diagnostic resolution would be improved over that provided by ICT. For example, where faults of class iX''' (single-chip gross access fault) occur in ICT, the boundary-scan facility on the SDRAM would be able to distinguish which of seven pins on the device were open.

At this time, the authors are unaware of any available or planned offerings of SDRAMs with boundary scan. However, due to the large ratio of die size to I/O pins of such ICs, it is estimated that the silicon overhead for providing boundary-scan should be less than 5%. It is hoped that memory IC vendors will realize the benefit of scan-test techniques, not only for board/manufacturing test, but also to access built-in test capabilities of such ICs.

10.4 Boundary Scan at Buffer

As it has a very simple function on the module (drive static outputs), the octal buffer is the last device to warrant consideration for boundary scan. Still, the additional cost (estimated at $2) required to procure equivalent buffers with boundary scan would be minimal.

10.5 Boundary Scan: Beyond Manufacturing Test

A real advantage that boundary scan holds over any other manufacturing test or DFT approach is that it is built into the ICs and, thus, the module, and so is available for use when ATE is not. For example, it can be used for module test during burn-in or under other conditions where the module is not accessible by ATE. Additionally, if appropriate system-level access to boundary scan is provided, it can be used for in-system test, diagnostics, configuration, programming, emulation, etc.

11. Comparative Study

Several metrics have been used to grade the different structural test methodologies outlined. A tabulation of the performance of the various test methodologies versus these metrics is given in Table 7.

Table 7. Comparison of Test Methodologies

METRIC	CARD-EDGE	ICT	BST
Fault coverage	95%+	95%+	95%+
Fault diagnostic	4 sol. joints	2 sol. joints	2 sol. joints
Vector development	100 per-hr	30 per-hr	15 per-hr
Test pattern size	1 Mb	100 kb	20 kb
Test time	0.1 s	0.1 s	0.1 s
Tester cost	$200k	$400k	$40k

Fault coverage is the estimated percentage of faults that will be detected. Since the subject module is fairly simple structurally, it is expected that all test methods will obtain a high level of coverage.

Fault-diagnostic capability is expressed as a weighted average of resolution in terms of solder joints. Excellent results from ICT and BST are typical, while the result for card-edge test belies the simple function of this module.

Vector development effort is measured in terms of the estimated number of person-hours required to complete the test set. Boundary-scan test development is highly automated, while ICT is somewhat less so. On the other hand, card-edge test development tends to be manual.

Test-pattern size is expressed in bits. With full BST, the vector set is on the order of $\log_2$ (number of module nodes). ICT vector sets will be somewhat longer, while card-edge vector sets can be very lengthy, in order to obtain desired fault coverage and diagnostic resolution.

Test time is a factor of the number of vectors and the vector application time. BST uses a low vector bit rate, but due to the small number of vectors, performs quite adequately. ICT and card-edge testers can use much higher vector bit rates.

Tester cost is estimated and is a function of performance (vector bit rate), number of test channels, etc. The small number of channels required for BST and modest performance requirements result in very inexpensive test systems.

12. Conclusion

Considering the metrics and discussion provided in the prior section, boundary-scan test is clearly a winning manufacturing test strategy, even for a module of modest functional complexity. Add to this the ability to reuse boundary scan during burn-in, and more importantly in fielded systems, and a small investment in additional component cost for boundary scan will reap dividends many times over throughout the product's life cycle.

References

1 *IEEE Std 1149.1–1990 (includes IEEE Std 1149.1a–1993) Standard Test Access Port and Boundary-Scan Architecture, Institute of Electrical and Electronics Engineers, New York, 1993.*

2 *JEDEC Std 21–C Configurations for Solid State Memories, Joint Electron Device Council, Electronic Industries Association, Arlington, VA, 1990, pp. 4–62–65.*

3 *M. Abramovici, M. A. Breur, and A. D. Friedman, Digital System Testing and Testable Design, Computer Science Press, New York, 1990.*

4 *J. H. Lau, Handbook of Fine Pitch Surface Mount Technology, Van Nostrand Reinhold, New York, 1994.*

5 *K. P. Parker, The Boundary-Scan Handbook, Kluwer Academic Publishers, Norwell, MA, 1992.*

6 *R. P. Prasad, Surface Mount Technology – Principles and Practice, Van Nostrand Reinhold, New York, 1989.*

7 *D. Bhavsar, "Testing Interconnects to Static RAMS," IEEE Design & Test of Computers, IEEE Computer Society Press, Los Alamitos, CA, June 1991.*

8 *M. Bullock, "Designing SMT Boards for In-Circuit Testability," Proceedings of the International Test Conference, Altoona, PA, 1987.*

9 *W. T. Daniel, "Optimizing Fault Detection for Boundary Scan Testing," Integrated System Design, The Verecom Group, Los Altos, CA, September 1995, pp. 30–36.*

10 *F. de Jong, A. J. de Lind van Wijngaarden, "Memory Interconnect Test at Board Level," Proceedings of the International Test Conference, Altoona, PA, 1992.*

11 *P. Hansen, "Testing Conventional Logic and Memory Clusters Using Boundary Scan Devices as Virtual ATE Channels," Proceedings of the International Test Conference, Altoona, PA, 1989.*

12 *A. W. Ley, "A Look at Boundary Scan from a Designer's Perspective," Proceedings of Electronic Design Automation & Test Asia Conference, Asian Electronics Engineer, Hong Kong, 1994.*

13 *C. Maunder, F. Beenker, "Boundary Scan: A Framework for Structured Design-For-Test," Proceedings of the International Test Conference, Altoona, PA, 1987.*

14 *M. Muris, A. Biewenga, "Using Boundary Scan Test to Test Random Access Memory Clusters," Proceedings of the International Test Conference, Altoona, PA, 1993.*

15 *G. D. Robinson, J. G. Deshayes, "Interconnect Testing of Boards with Partial Boundary Scan," Proceedings of the International Test Conference, Altoona, PA, 1990.*

16 *M. V. Tegethoff, T. W. Chen, "Sensitivity Analysis of Critical Parameters in Board Test," IEEE Design & Test of Computers, IEEE Computer Society Press, Los Alamitos, CA, Spring 1996.*

17 *P. Wagner, "Interconnect Testing with Boundary Scan," Proceedings of the International Test Conference, Altoona, PA, 1987.*

18 *1994 16-Megabit Synchronous DRAM Technical Reference (SMOU001A), Texas Instruments.*

19 *1994 Boundary-Scan Logic Data Book (SCTD002), Texas Instruments.*

20 *1994 Clock-Distribution Circuits Data Book (SCAD004), Texas Instruments.*

21 *1996 Semiconductor Group Package Outlines Reference Guide (SSYU001B), Texas Instruments.*

22 *SN74LVC244A product data sheet (SCAS414C), 1996 Low Voltage Logic Data Book (SCBD003B), Texas Instruments.*

23 *TMS626802 product data sheet (SMOS182A), 1995 MOS Memory Data Book (SMYD095), Texas Instruments.*

24 *CDC2586 product data sheet (SCAS337B), Texas Instruments.*

25 *SN74ALVCH162721 product data sheet (SCBS055), Texas Instruments.*

Hierarchically Accessing 1149.1 Applications in a System Environment

Lee Whetsel
Texas Instruments Incorporated
Senior Member Technical Staff
Semiconductor Group

SCTA033
© 1993 IEEE. Reprinted, with permission, from Proceedings of
International Test Conference, Baltimore, Maryland, October 17–21, 1993.

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1993, Texas Instruments Incorporated

Hierarchically Accessing 1149.1 Applications in a System Environment

Lee Whetsel
Senior Member Technical Staff
Texas Instruments Inc
Ph/Fx 214-575-2601/6198

Abstract

This paper presents a novel connection method that enables an 1149.1 test bus controller to hierarchically access and test 1149.1 circuits, independent of where the circuits exists within in an electronic system. The advantage of this approach is that it enables the 1149.1 test bus to be used hierarchically as a system level test bus, instead of only as a board level test bus.

Background

In the electronics industry, significant improvements have been made in the area of board level testing, largely due to the development of a standard test access port and boundary scan architecture for ICs, referred to as IEEE Std 1149.1-1990 [1]. The 1149.1 standard defines a test access port and associated test circuitry that can be included in ICs to simplify testing at the board level.

One of the most important features of the 1149.1 standard is a four wire test bus that enables commands and data to be serially communicated to ICs on a board for testing purposes. The presence of this standard board level test bus interface has inspired the test community to focus on a common approach to board level testing problems.

The challenge now facing the electronics test industry is how to gain access to 1149.1 testability features after the board has been embedded within a system. Most system companies who invest in 1149.1 at the board level, do so under the assumption that the board testability resources can be reused to simplify their system testing problems. However, currently there are no proposed methods of accessing 1149.1 in a system environment. There are proposals for accessing 1149.1 boards in a backplane environment, but these proposals are focused on single level access operations and do not anticipate the hierarchical access needs found within system architectures. [2,3,4,5,7,8]

If test access solutions progress the way they currently are, the industry will eventually have a unique test access standard for each different environment level within a system. For example, the industry may eventually have different standards for: accessing multi-chip modules on a board, accessing boards in a backplane, accessing backplanes in a subsystem, and accessing subsystems in a system. If system test access evolves in this fashion, the end result may well turn out to be an overly complicated, inefficient network of non-compatible test buses interfaced together using protocol translating devices.

Introduction

This paper presents an approach which anticipates the hierarchical test access needs of system architectures. Using this approach, hierarchical connections can be made in a system architecture to enable 1149.1 applications to be accessed directly via the standard 1149.1 test bus. The primary benefit of this approach is that it eliminates the need to use other environment-specific test buses to gain access to embedded 1149.1 applications within systems.

A paper presented at ITC in 1992 described how an 1149.1 test bus controller (TBC) could select and access 1149.1 applications in a single level environment, such as boards in a backplane, using a protocol referred to as a shadow protocol and a connection device referred to as an addressable shadow port (ASP) [6]. The approach described in this paper is based on an extended shadow protocol and a connection device referred to as a hierarchically addressable shadow port (HASP). The extended shadow protocol and HASP allow the connection features described in the 1992 paper to be used hierarchically in a system architecture, instead

Copyright IEEE, Reprinted, with permission, from Proceedings of International Test Conference, Baltimore, Maryland, October 17-21, 1993.

of being limited to single level connection applications.

Throughout the remainder of this paper the words "environment" and "application" are used. The word "environment" is used to indicate a physical level within a system architecture where one or more ASPs or HASPs reside. The "root environment" is the lowest level environment, and is where the 1149.1 TBC resides. The word "application" is used to indicate an 1149.1 circuit within an environment that can be accessed by a TBC after a hierarchical connection has been made. In this paper, the hierarchical access examples are described as coming from a lower level environment to a higher level environment.

Shadow Protocols

The 1149.1 test bus has four signal wires, test clock (TCK), test mode select (TMS), test data output (TDO), and test data input (TDI). 1149.1 protocol transmitted on the TMS signal controls applications on the test bus to scan data, enter an idle state, or enter a reset state. When TMS places the test bus in an idle state (i.e. 1149.1 RT/IDLE, PAUSE-IR or PAUSE-DR states) or a reset state (i.e. 1149.1 TLRST state), all 1149.1 applications are disabled from responding to data transmitted on TDI and TDO. While the 1149.1 test bus is idle or reset, the shadow protocol can be transmitted over the TDI and TDO wires to make a connection between a TBC and a target application within a system, via an ASP or via an ASP connected to one or more HASP circuits.

The shadow protocol comprises two protocols, a select protocol and an acknowledge protocol. At the beginning of a shadow protocol, a select protocol is transmitted from the TBC to an ASP either directly or through one or more HASPs residing between the TBC and ASP to make a connection. After the select protocol has been transmitted, an acknowledge protocol is transmitted to the TBC from the selected ASP either directly or through one or more HASPs residing between the ASP and TBC to confirm the connection. The shadow protocol is transmitted on the TDI and TDO bus wires using a bit-pair signaling method. The TMS signal is not involved with the shadow protocol, therefore the TMS signal can be used to hold 1149.1 applications in a desired 1149.1 steady state while the shadow protocol is transmitted to make a connection.

The bit-pair signaling method used in the shadow protocol allows control and data to be transmitted together on a single wiring channel. The control signals are used to start and stop the select and acknowledge protocols and to frame data signals that form addresses within the select and acknowledge protocols. The bit-pair signals used in the select and acknowledge protocols are defined in the following list.

Idle Signal (I) – a control signal identified by the transfer of two successive logic one bits from a transmitter to a receiver.

Select Signal (S) – a control signal identified by the transfer of two successive logic zero bits from a transmitter to a receiver.

Data 1 Signal (D) – a logic one signal identified by the transfer of a logic zero bit followed by a logic one bit from a transmitter to a receiver.

Data 0 Signal (D) – a logic zero signal identified by the transfer of a logic one bit followed by a logic zero bit from a transmitter to a receiver.

The bit-pair signals are output from the transmitting device's (TBC's, ASP's, or HASP's) TDO on the falling edge of TCK and are input to the receiving device's (TBC's, ASP's, or HASP's) TDI on the rising edge of TCK. Since this data transfer is consistent with the way 1149.1 serial data is transferred, upgrading a TBC to support this approach is simply a matter of controlling TMS to idle or reset 1149.1 applications, while using otherwise normal 1149.1 scan operations to transmit and receive the select and acknowledge protocols.

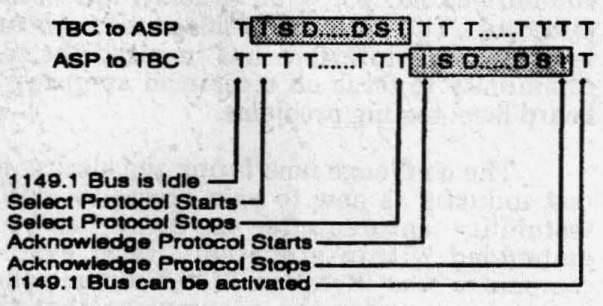


FIGURE 1 Select and Acknowledge Protocols

Select and Acknowledge Protocols

In Figure 1, a diagram is shown of a single level select and acknowledge protocol being transmitted while the 1149.1 test bus is idle to make a connection between a TBC and

ASP application. The tristate signals (T) before and after the protocol sequences indicate that the 1149.1 test bus is idle and that the TDO outputs from the TBC and ASP are disabled and pulled high. The "ISD..DSI" sequence transmitted from the TBC to the ASP is the select protocol. The "ISD..DSI" sequence transmitted from the ASP to the TBC is the acknowledge protocol. After the ASP transmits the acknowledge protocol it connects the TBC up to the application.

The I signal at the beginning of each protocol is designed to be indistinguishable from the preceding T signals. This avoids unintentional entry into a select or acknowledge protocol when the 1149.1 bus enters an idle or reset state. However, the I signal at the end of each protocol is designed to be distinguishable from the preceding S and D signals so that it can be used to terminate the protocol. Inside each protocol, first and second S signals are used to frame the address which is defined by a series of logic 1 and logic 0 D signals.

In this single level access shadow protocol, only one address frame (SD..DS) is transmitted between the first and second I signals of the select and acknowledge protocol. However, in a multi-level shadow protocol, two or more address frames (SD..DS) are transmitted between the first and second I signals of the select and acknowledge protocol to make a hierarchical connection.

Hierarchical Access Examples

The following examples illustrate how a TBC can use ASP and HASP circuits to hierarchically access 1149.1 applications in systems having from one to "m" environment levels. In the examples, analogies are made between the way this approach hierarchically links to an 1149.1 application through multiple system environments, and the way an operating system hierarchically links to a file through multiple software directories. In the analogies, "Sys"=system, "Sub"=subsystem, "Bpn"=backplane, "Brd"=board, "App" = application, "Env"=environment, and "Dir"=directory.

Single Level System Test Access

In the single level environment of Figure 2, a Backplane resident TBC is connected to Board ASPs (1-n) via a four wire 1149.1 test bus. Each ASP is further connected to ICs on a board (application) via a four wire 1149.1 test bus. The naming convention given to the ASPs in Figure 1 is "ASPn:m", where "n" indicates the ASP's address and "m" indicates the environment level the ASP resides on. The ASPs are connected to the TBC via their primary port signals (PTDI, PTMS, PTCK, PTDO) and to the application via their secondary port signals (STDI, STMS, STCK, STDO). While all four 1149.1 signal wires are shown in Figure 2, only the ASP PTDI, STDI, PTDO, and STDO, and application and TBC TDI and TDO signals are named. The environment level number of the ASP is included in the primary and secondary port signal names, i.e. PTDI1, PTDO1, STDO1, and STDO1. The above mentioned naming conventions are followed throughout the remainder of this paper.

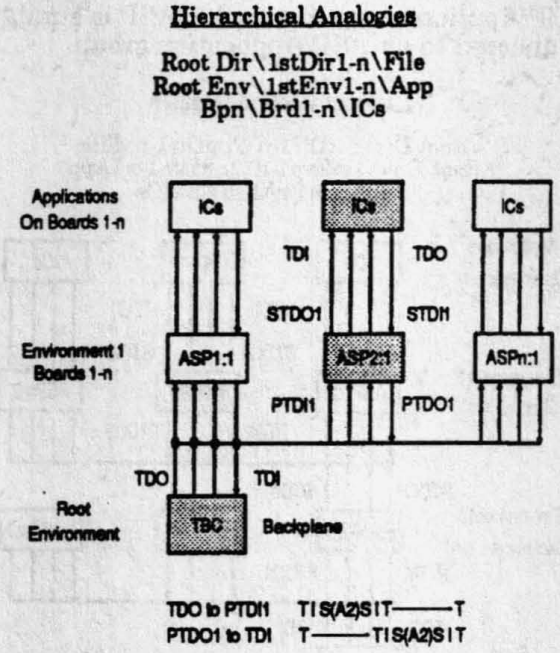


FIGURE 2 Single Level System Test Access

Before an application on one of the Boards (1-n) can be serially accessed by the TBC, a connection must be made between the TBC and application. To make a connection between the application of ASP2:1 and the TBC, the TBC outputs a single level select protocol from its TDO output to the PTDI1 input of all ASPs on Environment 1. In this example, the address sent in the select protocol is address 2 (A2). In response to receiving the select protocol with an address of 2, ASP2:1 outputs an acknowledge protocol containing its

address (A2) from its PTDO1 output to the TBC's TDI input, then connects the application to the TBC (as shown in darkened boxes). The TBC verifies the connection by inspecting the address returned in the acknowledge protocol, then accesses the application using the 1149.1 protocol. This single level connection example is identical to the one described in the 1992 paper, since only a single level connection is made, i.e. board and backplane.

Two Level System Test Access

In the two level environment of Figure 3, a Subsystem resident TBC is connected to Backplane HASPs (1-n) in Environment 1. Each Backplane HASP (1-n) is further connected to Board ASPs (1-n) in Environment 2. Each Board ASP (1-n) is further connected to an Application. While connections are only shown between HASP1:1 and its ASP/Application group, each HASP is similarly connected to an ASP/Application group.

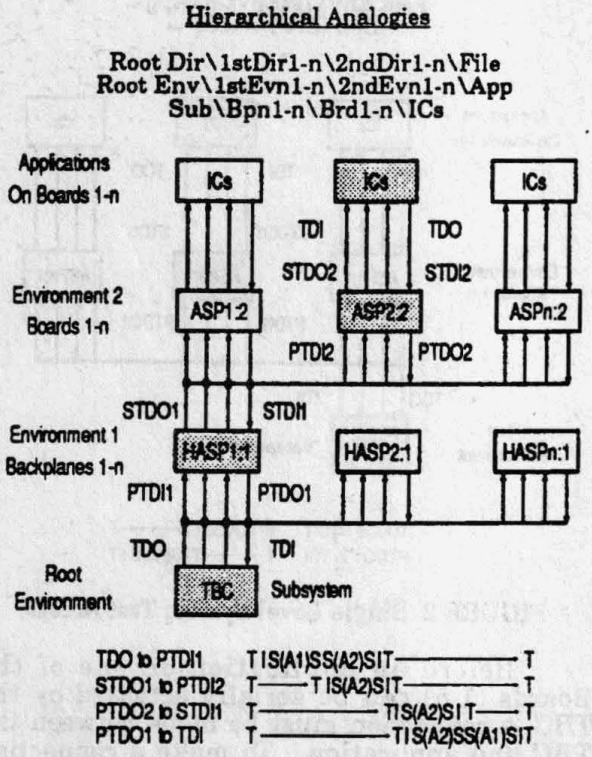


FIGURE 3 Two Level System Test Access

Before an application on one of the Boards (1-n) can be serially accessed by the TBC, a hierarchical connection must be made between the TBC and application. To make a connection between the application of ASP2:2 and the TBC, the TBC outputs a two level select protocol from its TDO output to the PTDI1 input of all HASPs on Environment 1. The two level hierarchical select protocol differs from the single level select protocol of Figure 1 in that two address frames are transmitted between the first and second I signals. The first address frame (A1) selects HASP1:1 and the second address frame (A2) selects ASP2:2.

After HASP1:1 has received its address frame (SA1S), it looks to see what signal follows the address frame. If an I signal were to follow the first address frame, HASP1:1 would recognize the protocol as a single level type and would start its acknowledge protocol. However, since an S signal follows the first address frame, HASP1:1 recognizes that the select protocol is hierarchical and that a new address frame is being transmitted. After HASP1:1 recognizes that the select protocol is hierarchical, it does not respond to any of the additional address frames it receives, thus it cannot be deselected by subsequent address frames transmitted within the current hierarchical select protocol. Also when HASP1:1 recognizes that the select protocol is hierarchical, it sets an internal flag which modifies the way it operates during the hierarchical acknowledge protocol.

In response to the start of the second address frame (SA2S) from the TBC, HASP1:1 enables its STDO1 output, sends an I signal, then relays the second address frame to ASPs of Environment 2. There is a one bit-pair signal latency between the end of the first address frame from the TBC (SA1S) and the start of the relayed second address frame from HASP1:1 (SA2S). This latency is caused by the decision step HASP1:1 performs to determine what signal (S or I) follows the first address frame (SA1S).

When the TBC completes the transmission of the hierarchical select protocol, it outputs T signals (or logic 1's) on its TDO output and monitors its TDI input for the start of an acknowledge protocol from the PTDO1 output of HASP1:1. Likewise, when HASP1:1 completes relaying the hierarchical select protocol it outputs T signals on its STDO1 output and monitors its STDI1 input for the start of an acknowledge protocol from the PTDO2 output of ASP2:2.

After ASP2:2 has received its address frame (SA2S) from HASP1:1, it starts an

acknowledge protocol output to HASP1:1. After transmitting a first I signal to initiate the acknowledge protocol, ASP2:2 outputs its address frame sequence (SA2S) from its PTDO2 output to the STDI1 input of HASP1:1. In response to the first S signal of the address frame input from ASP2:2, HASP1:1 enables its PTDO1 output and starts relaying the acknowledge protocol from ASP2:2 to the TBC's TDI input by outputting a first I signal. After ASP2:2 has transmitted its address frame to the STDI1 input of HASP1:1, it terminates its acknowledge protocol by outputting a second I signal, then makes a connection between its application and the secondary port of HASP1:1.

In response to the second I signal input from ASP2:2, HASP1:1 continues the acknowledge protocol sequence by inserting and outputting its own address frame (SA1S) to the TDI input of the TBC. After HASP1:1 has transmitted its address frame to the TBC, it terminates the hierarchical acknowledge protocol by outputting a second I signal, then makes a connection between ASP1:1 and the TBC. After the TBC receives the second I signal it determines that the hierarchical acknowledge protocol is complete and examines the addresses received to confirm the correct hierarchical connection was made. If the connection is correct, the TBC accesses the application using the 1149.1 protocol.

Three Level System Test Access

In the three level environment of Figure 4, a System resident TBC is connected to Subsystem HASPs (1-n). Each Subsystem HASP (1-n) is further connected to Backplane HASPs (1-n). Each Backplane HASP (1-n) is further connected to Board ASPs (1-n). Each Board ASP (1-n) is further connected to an Application.

The steps for the TBC to hierarchically connect and access the application of ASPn:3 is similar to the two level access example of Figure 3 and comprises; (1) outputting a three level hierarchical select protocol to select HASP1:1, HASP2:2, and ASPn:3, (2) receiving and confirming a three level hierarchical acknowledge protocol from ASPn:3, HASP2:2, and HASP1:1, and (3) accessing the application via the connections made between HASP1:1, HASP2:2, and ASPn:3 using the 1149.1 protocol.

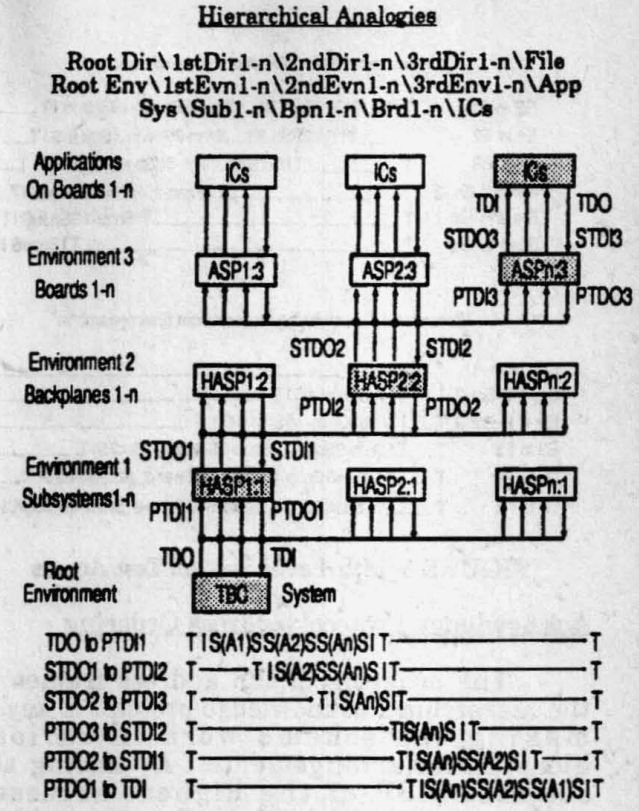


FIGURE 4 Three Level System Test Access

Mth-Level System Test Access

While the previous examples have shown how shadow protocols and ASP/HASP circuits are used to access applications existing on 1, 2, and 3 level system environments, the approach can be used to access any environment level (m) within a system.

For example, the hierarchical select and acknowledge protocols of Figure 5 illustrate connecting an application in environment level "m" to a TBC in the root environment (RE) via intermediate environment levels E1, E2, E3...Em-2, and Em-1. Each address frame in the hierarchical select and acknowledge protocols is indicated by the sequence "Sn:mS", where "n" is the address and "m" is the environment level the address is sent to or received from. The ability of the this approach to hierarchically connect a TBC to an application on any environment level within any type of system, provides an extremely simple, yet powerful method of accessing and testing 1149.1 applications.

Hierarchical Select Protocol to Environment "m"

RE to E1	TI Sn:1SSn:2SSn:3S....Sn:m-2SSn:m-1SSn:mS IT.....T
E1 to E2	T.....TI Sn:2SSn:3S....Sn:m-2SSn:m-1SSn:mS IT.....T
E2 to E3	T.....TI Sn:3S....Sn:m-2SSn:m-1SSn:mS I T....T
Em-3 to Em-2	T.....TI Sn:m-2SSn:m-1SSn:mS IT..T
Em-2 to Em-1	T.....TI Sn:m-1SSn:mS ITT
Em-1 to Em	T.....TI Sn:mS IT

Hierarchical Acknowledge Protocol from Environment "m"

Em to Em-1	TI Sn:mS IT ..... T
Em-1 to Em-2	TT I Sn:mSSn:m-1S I T ..... T
Em-2 to Em-3	T...TI Sn:mSSn:m-1SSn:m-2S I T ..... T
E3 to E2	T....TI Sn:mSSn:m-1SSn:m-2SSn:m-3_Sn:3SI T..... T
E2 to E1	T.....TI Sn:mSSn:m-1SSn:m-2SSn:m-3_Sn:3SSa:2SI T..... T
E1 to RE	T.....TI Sn:mSSn:m-1SSn:m-2SSn:m-3_Sn:3SSn:2SSn:1SIT

FIGURE 5 Mth-Level System Test Access

Acknowledge Protocol Address Ordering

The ordering of the address frames in the hierarchical acknowledge protocol is key to making the scheme work in various hierarchical arrangements. By having the selected ASP of the highest accessed environment level initiate the hierarchical acknowledge protocol, HASPs in lower environment levels only have to monitor their STDI inputs to determine when the hierarchical acknowledge protocol has been started.

Since the higher level acknowledge protocols are framed by first and second I signals, it is a simple process for a lower level HASP to determine when a higher level acknowledge protocol transmission is complete so that it can insert its own address frame in the hierarchical acknowledge protocol being relayed to the TBC. By its design, the operation of the hierarchical acknowledge protocol is simple and structured, and independent of the number of environment levels it traverses.

Hierarchical Connection Example

In Figure 6, a System TBC is connected to Subsystem HASP1 of Environment 1, HASP1/E1. HASP1/E1 is connected to Backplane HASP1 of Environment 2, HASP1/E2. HASP1/E2 is connected to Board ASP1 of Environment 3, ASP1/E3. ASP1/E3 is connected to the Application on Board 1 (ICs).

The TBC has a transmitter (XMT) to output the select protocol, a receiver (RCR) to receive the acknowledge protocol, and a controller (CTL) to regulate the operation of the transmitter and receiver, and the TMS output signal. When the controller is not using the transmitter and receiver to communicate select and acknowledge protocols, the controller can use them to communicate the 1149.1 protocol by activation of the TMS output signal.

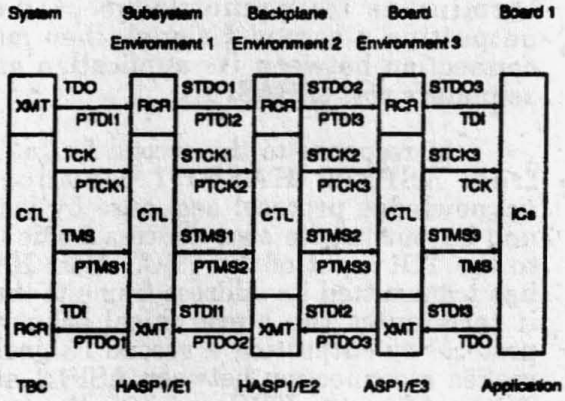


FIGURE 6 Hierarchical Connection Example

The ASPs and HASPs have a receiver (RCR) to receive the select protocol, a transmitter (XMT) to output the acknowledge protocol, and a controller (CTL) to regulate the operation of the transmitter and receiver, and the PTMS to STMS signal connection. If the receiver and transmitter are not being used to communicate select and acknowledge protocols, and if the ASP/HASP is selected, serial data and TMS control may be transferred from PTDI to STDO, from STDI to PTDO, and from PTMS to STMS during 1149.1 scan operations.

When scan access of the ICs of Board 1 is required, the TBC outputs a hierarchical select protocol to the receiver of HASP1/E1. In response, HASP1/E1's receiver strips off its address frame and relays the remaining portion of the select protocol to the receiver of HASP1/E2. In response, HASP1/E2's receiver strips off its address frame and relays the remaining portion of the select protocol to the receiver of ASP1/E3.

After the hierarchical select protocol completes, the transmitter of ASP1/E3 outputs an acknowledge protocol to the transmitter of HASP1/E2. In response, HASP1/E2's

transmitter relays the acknowledge protocol to the transmitter of HASP1/E1, inserting its own address frame before terminating the acknowledge protocol. In response, HASP1/E1's transmitter relays the acknowledge protocol to the receiver of the TBC, inserting its own address frame before terminating the acknowledge protocol.

After each HASP and ASP completes its acknowledge protocol, it connects its primary and secondary ports together. After receiving and verifying the hierarchical acknowledge protocol, the TBC's control circuit enables the transmitter, receiver, and TMS output to access the ICs of Board 1, via the connections made through HASP1/E1, HASP1/E2, and ASP1/E3, using the 1149.1 protocol.

Synchronizing 1149.1 Data Transfers

In Figure 7, an important difference is shown between the methods used by the HASPs and ASP of Figure 6 to connect their primary and secondary bus signals. In the ASP, a simple electronic switch is used to connect the primary and secondary port signals, since only a single level connection is made. However, since any number of levels may be connected using hierarchically arranged HASPs, it is important to provide a method of synchronizing the data transfer between HASP primary and secondary ports using clocked storage elements such as the D-flip flops (DFF) of Figure 7.

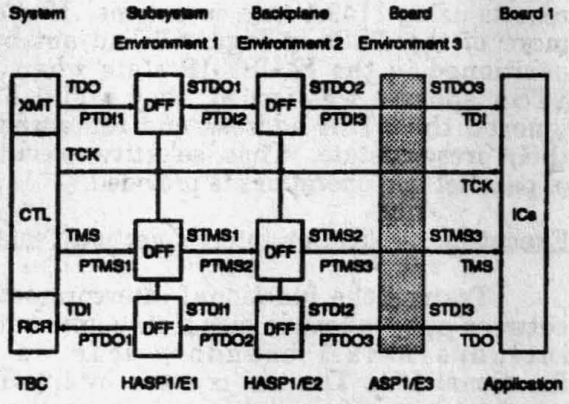


FIGURE 7 HASP Port Synchronization

If the primary and secondary bus signal connections of the HASP were made by simple electronic switches, as in the ASP, the accumulation of delays through the switches of hierarchically connected HASPs would limit the 1149.1 data transfer rate through the connection. However, with the primary and secondary HASP connections synchronized through DFFs as shown in Figure 7, delays do not accumulate as more HASPs are included in a hierarchical connection. Thus, no limitation is placed on the 1149.1 data transfer rate as more environment levels are connected between the TBC and application.

Accessing and Testing Applications

In Figure 8, a TBC is shown connected to the primary ports (PP) of ASPs 1-(n-2) via an 1149.1 test bus. Each ASP's secondary port (SP) is connected to an appropriately numbered 1149.1 application via an 1149.1 test bus. The TBC and applications illustrate the 1149.1 steady states in which shadow protocols can be transmitted to make or break connections between the TBC and applications. The darkened boxes of Figure 8, indicate reserved addresses "0", "n-1" and "n", which are not used as application addresses.

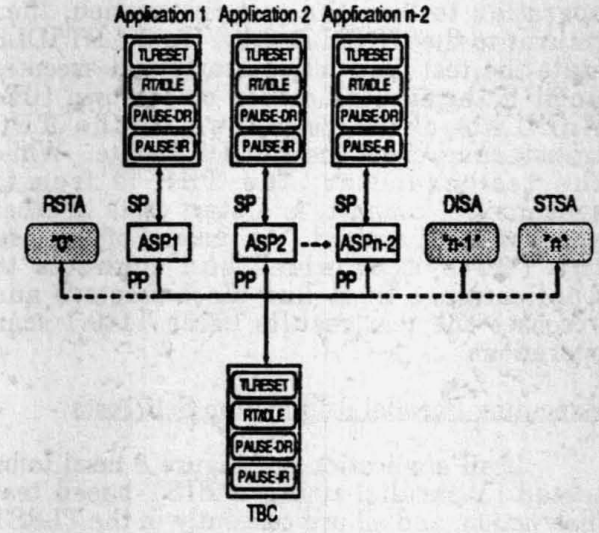


FIGURE 8 Single Level Test Access Example

The "0" address is a reset address (RSTA) recognizable by all ASPs and HASPs. ASPs and HASPs receiving the RSTA address disconnect their ports and force their applications into the TLRST state by setting their STMS output to a logic one. The "n-1" address is a disconnect address (DISA) recognizable by all ASPs and HASPs. ASPs and HASPs receiving the DISA address

disconnect their ports and remain in the 1149.1 steady state they were in when the disconnect occurs. The "n" address is a self test synchronization address (STSA) recognizable by all ASPs and HASPs. ASPs and HASPs receiving the STSA address while in the 1149.1 PAUSE-IR/DR states connect PTMS to STMS and disconnect PTDI and STDO, and STDI and PTDO.

Executing Single Application Self Tests

If Application 1 needs to be tested using a BIST based test instruction, like the 1149.1 RunBist instruction [1], and is currently in the TLRST state, the TBC moves itself to the TLRST state to synchronize states with Application 1, then executes a shadow protocol to connect to Application 1. After a connection is made between the TBC and Application 1, the TBC transitions itself and Application 1 from TLRST to the RT/IDLE state to prepare for testing.

After entering the RT/IDLE state, the TBC executes an 1149.1 instruction scan operation to load the test instruction, then returns to the RT/IDLE state. In the RT/IDLE state the test instruction starts and executes until it terminates either on its own (like RunBist) or in response to the TBC transitioning from the RT/IDLE state. While the test executes, the TBC is free to synchronize, connect, and start tests in other applications if desired. At the end of the test, the TBC synchronizes and connects to Application 1 (if it has disconnected) and accesses the test results using 1149.1 scan operations.

Executing Parallel Application Self Tests

If all applications of Figure 8 need to be tested in parallel using a BIST based test instruction, and all are currently in the TLRST state, the TBC moves itself to the TLRST state and executes the following sequence.

The TBC transmits a shadow protocol to connect Application 1 to the TBC. After the connection is made, the TBC transitions itself and Application 1 from TLRST to the RT/IDLE state. After entering the RT/IDLE state, the TBC executes an instruction scan operation to load the test instruction into Application 1 then terminates the instruction scan operation in the PAUSE-IR state. The TBC then transmits a shadow protocol containing the DISA address to disconnect Application 1 in the PAUSE-IR state. The TBC then transitions itself from PAUSE-IR to the TLRST state to synchronize 1149.1 states with the next application to be connected. These steps are repeated on Applications 2 through n-3.

After Application n-3 has been setup as previously described, the TBC transmits a shadow protocol to connect Application n-2 to the TBC. After the connection is made, the TBC transitions itself and Application n-2 from TLRST to the RT/IDLE state. After entering the RT/IDLE state, the TBC executes an instruction scan operation to load the test instruction into Application n-2 then terminates the instruction scan operation in the PAUSE-IR state. While in PAUSE-IR, the TBC transmits a shadow protocol containing the STSA address. All ASPs currently in the PAUSE-IR state respond to the STSA address to connect their PTMS and STMS signals together, enabling the TBC's TMS output to be input to each ASP application. After making this global TMS connection, the TBC transitions itself and all applications from PAUSE-IR to RT/IDLE to start the parallel test operation.

The parallel test operation continues until all tests have terminated either on their own or in response to the TBC transitioning from the RT/IDLE state. At the end of the parallel test operation, the TBC executes shadow protocols to connect to each application, one at a time, to access the test results using 1149.1 scan operations. If one or more of the ASPs in Figure 8 had not been positioned in the PAUSE-IR state when the STSA address was issued, they would have ignored the STSA address and remained in their present state. Thus, selective execution of parallel test operations is provided.

Executing Application Interconnection Tests

Testing the functional interconnection between applications is easy if each application includes 1149.1 boundary scan on its functional I/O. The test is setup by the TBC synchronizing states with and connecting to each application, one at a time. After the TBC is connected to an application it performs an 1149.1 instruction scan operation to load the 1149.1 Sample/Preload instruction. After loading the Sample/Preload instruction, the TBC performs a data scan operation to load a safe initial boundary I/O test pattern. Next,

the TBC performs an instruction scan operation to load the 1149.1 Extest instruction, terminating the instruction scan operation in the PAUSE-IR state. While in the PAUSE-IR state, the TBC executes a shadow protocol containing the DISA address to disconnect from the application so that other applications can be connected and setup as described. Since the application is disconnected in PAUSE-IR, the Extest instruction has not been updated to take effect.

After all applications have been setup as described, the TBC positions itself in the PAUSE-IR state, then transmits a shadow protocol containing the STSA address. In response to the STSA address, all applications are connected to the TBC's TMS output, via their ASPs. The TBC then transitions itself and all applications from PAUSE-IR to RT/IDLE to cause all applications to simultaneously update their Extest instructions and enter test mode. Since each application was loaded with a safe initial boundary I/O test pattern, no I/O conflicts occur between applications when the Extest mode is entered.

Following this setup procedure, interconnection testing is accomplished by the TBC selectively connecting to each application, one at a time and while in the RT/IDLE state, to set boundary outputs and read boundary inputs using 1149.1 data scan operations.

While this example used the Extest instruction to scan test the interconnections between applications, at-speed interconnection tests based on BIST (i.e. pseudorandom pattern generation/data compaction) could be used as well. If BIST interconnection testing is performed the applications are setup and enabled for testing as described in the "Executing Parallel Application Self Test" section.

Hierarchical Access and Testing

In the example of Figure 8, the TBC was shown directly connected to the ASP of each application. In actual systems however, the TBC may not always be directly connectible to the ASP of each application due to the placement of the applications in the system hierarchy. Therefore HASPs may reside between the TBC and ASPs to provide a hierarchical connection between the TBC and applications, as shown in Figure 9.

The access and testing procedures previously described in regard to the single level connection arrangement shown in Figure 8 still apply to the three level connection arrangement shown in Figure 9. The only difference in Figure 9 is that a three level connection is traversed to access and test the applications.

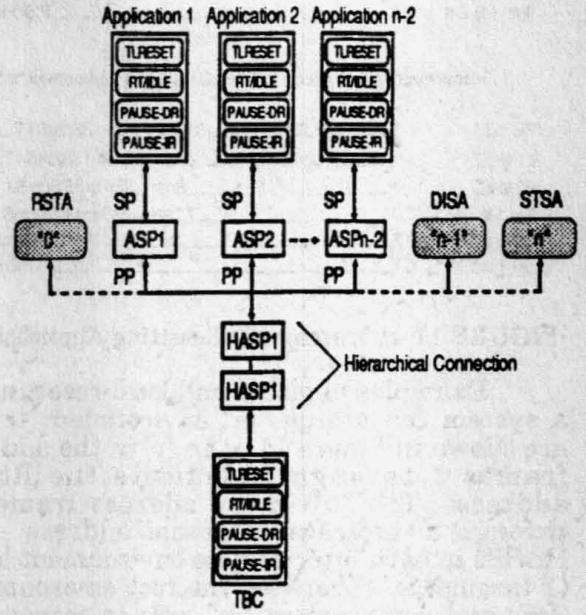


FIGURE 9 Three Level Test Access Example

Hierarchically Sending RSTA Addresses

After hierarchically accessing and testing applications within a system, numerous applications may be left in various 1149.1 steady states and test modes. To insure the stability of the system in its mission mode, all applications need to be placed in the TLRST state following test.

One way of placing system applications in the TLRST state is for the TBC to individually connect and set each application into the TLRST state. However, a faster way of placing system applications in TLRST is for the TBC to globally transmit a hierarchical select protocol consisting of multiple RSTA address frames. Alternately, the TBC can locally place applications existing at and above a selected environment level in TLRST by sending actual address frames in a hierarchical select protocol prior to sending the RSTA frames. The actual address frames direct the reset action to only the applications at and above the selected environment level.

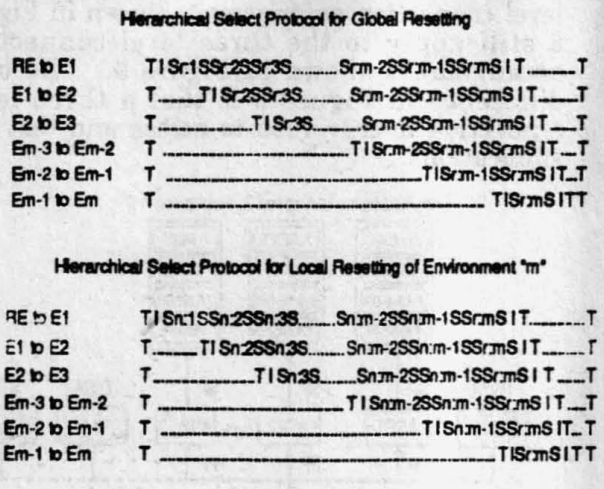


FIGURE 11 Hierarchically Resetting Applications

Examples of global and local resetting in a system containing "m" environment levels are shown in Figure 11. The "r" in the address frames 1 through m indicate the RSTA address. The "n" in the address frames 1 through m indicate an actual address. All HASPs in each intermediate environment level (1 through m-1) between the root environment (RE) and environment "m" wait to respond to the RSTA address until after the hierarchical select protocol terminates, so that all relayed RSTA address frames can be transmitted to the highest environment level (m). HASPs and ASPs receiving a RSTA address do not execute an acknowledge protocol. However, HASPs that receive an actual address do respond with an acknowledge protocol.

Hierarchically Sending DISA/STSA Addresses

While Figure 11 illustrates RSTA address frames "r" being globally and locally transmitted to connections and applications, DISA and STSA address frames can be globally or locally transmitted as well. DISA address frames are transmitted in place of the "r" addresses in the hierarchical select protocols to disconnect connections and applications. STSA frames are transmitted in place of the "r" addresses in the hierarchical select protocols to synchronize selected connections and application groups to the TBC's TMS output. As with the RSTA address frame, HASPs and ASPs receiving DISA or STSA address frames do not execute an acknowledge protocol.

Conclusion

This paper has described a hierarchical test access problem the industry will eventually face in system architectures, and a proposed solution to this problem. The solution is based on a connection circuit and protocol that can operate in any hierarchical arrangement to provide access to and test control of 1149.1 applications in a system environment. This access method provides a simple way to effectuate expanded use of the 1149.1 test bus in systems. The advantages of this approach are: (1) connection protocol is supportable by most 1149.1 TBCs/ATEs, (2) connection protocol rides on top of existing 1149.1 bus wiring, (3) does not require protocol translation in the connection path, (4) does not impact 1149.1 test bus bandwidth, (5) supports parallel 1149.1 test operations, (6) supports any type of hierarchical connection arrangement, and (7) simple, cost-effective implementation.

References

1. IEEE Std 1149.1-1990, Standard Test Access Port and Boundary Scan Architecture

2. IEEE Standard Proposal 1149.5, A Standard Module Test and Maintenance Bus.

3. L. Whetsel, "JTAG Compatible Devices Simplify Board Level Design For Testability", IEEE Wescon Convention, November 1989.

4. N. Jarwala and C. Yau, "The Boundary-Scan Master: Target Applications and Functional Requirements", IEEE International Test Conference, September 1990.

5. D. Bhavsar, "An Architecture for Extending the IEEE Standard 1149.1 Test Access Port to System Backplanes", IEEE International Test Conference, October 1991.

6. L. Whetsel, "A Proposed Method of Accessing 1149.1 in a Backplane Environment", IEEE International Test Conference, September 1992.

7. D. Landis, "Applications of the IEEE 1149.5 Module Test and Maintenance Bus", IEEE International Test Conference, September 1992.

8. D. Ohnesorge, "A Position Independent Scan Architecture", IEEE European Design for Test Workshop, 1992.

JTAG/IEEE 1149.1
Design Considerations

SCTA029
August 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	Page
Introduction	**7–45**
Is JTAG Right for You?	**7–46**
Boundary-Scan Training	**7–48**
Determining Where to Place Boundary-Scan Devices	**7–49**
Available Literature on TI's JTAG Boundary-Scan Logic Products	**7–50**
Acknowledgment	**7–50**
Appendix A – Basics of Boundary Scan	**7–51**
Appendix B – Boundary-Scan Success Stories	**7–55**

List of Illustrations

Figure	Title	Page
1	Physical Access Problem in PCB Designs	7–45
2	Life-Cycle Costs of Typical Product	7–47
3	Boundary-Scan Cell	7–51
4	Pinout of TI's SN74BCT8244	7–51
5	TAP-Controller State Diagram	7–52
6	Scan Path Connecting Two Boundary-Scan Devices	7–53

List of Tables

Table	Title	Page
1	Comparative Test-Cost Model	7–46
2	Performance Comparison, JTAG Transceiver Functions	7–49

Introduction

The JTAG/IEEE 1149.1 test standard is becoming widely accepted as a way to overcome the problems created by surface-mount packages, double-sided boards, and multichip modules (see Figure 1), all of which result in a loss of physical access to signals on the board. By providing a means to test printed-circuit boards and modules that might otherwise be untestable, the time and cost required to develop a product and bring it to market can be reduced significantly. (see Appendix A for a brief overview of the 1149.1 standard.)

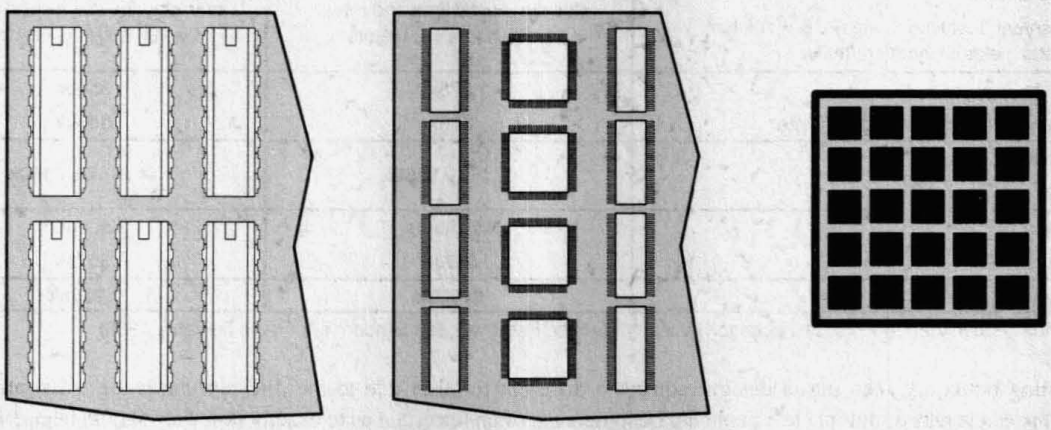


Figure 1. Physical-Access Problem in PCB Designs

The conversion to boundary scan has been readily accepted by many who realize that traditional test methods are not effective in dealing with the issues of decreasing physical access. Their products are such that faults not detected in the factory can be costly to isolate and repair if they surface after they are in the field. These customers see boundary scan as the only solution and have realized cost as well as time-to-market savings, in addition to providing a more reliable product to their customers.

There are others who view boundary scan more skeptically and are uncertain of the ultimate benefits. To help illustrate the potential savings of boundary scan, Table 1 provides a comparative test cost model for an application from the professional product division of Philips Electronics, which involved including boundary scan in their ASICs. Though it doesn't specifically address boundary-scan logic, the benefits to test program generation, testers, fixture costs, etc. apply.

The reader may use this table as a guide to determine the comparative cost savings for his application. In place of the implementation costs for ASICs, you can substitute additional material costs associated with boundary-scan bus interface devices over their nonscan counterparts. In addition to costs savings, there are the benefits of decreased time to market, improved product quality, reduced customer downtime, etc.

Table 1. Comparative Test-Cost Model

	BOUNDARY SCAN	NON BOUNDARY SCAN
Implementation cost (BSR) 200k boards/year, 12 ASICs per PCB, 1% of $25 ASIC	**$600k**	**None**
Test program generation 30 PCB types/year @ $50/hour	50 hours/type = **$75k**	300 hours/type = **$450k**
Diagnostics 70% yield of 200k PCBs = 60k PCBs to be repaired @ $25/hour	2 min. per repair = 2k hours = **$50k**	10 min. per repair = 10k hours = **$250k**
Number of testers 200k PCBs/year, test time 3 min./PCB = 10k hrs; 3 shifts/tester yields 5k hrs/year/tester	plus diagnostic time and retest = 15k hours = 3 testers	plus diagnostic time and retest = 23k hours = 5 testers
Tester costs Investment = cost of ownership 33%/year	$75k **$75k**	$500k **$830k**
Fixture costs 30 fixtures	@ $5k = **$150k**	@ $15k = **$450k**
Labor cost @ $25/hour	15k hours **$375k**	23k hours **$575k**
Yearly total	**$1325k**	**$2555k**

(from: *Boundary-Scan Test, A Practical Approach* by Harry Bleeker, Peter van den Eijnden, and Frans de Jong, 1993)

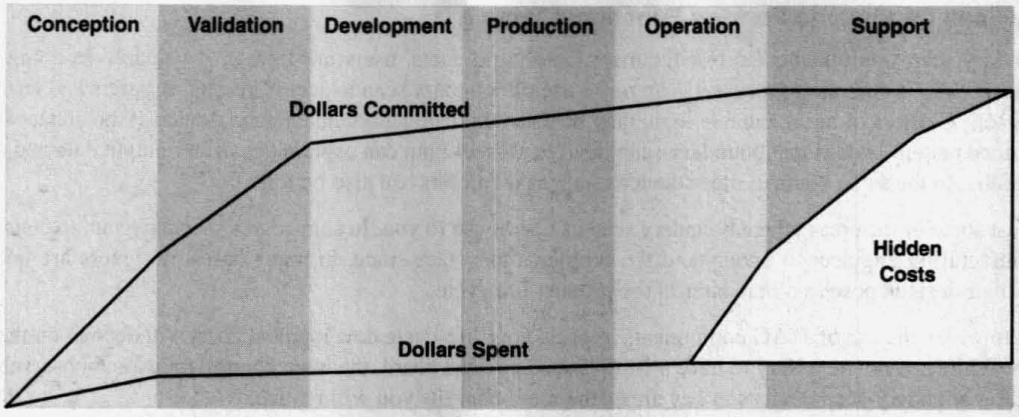
Implementing boundary scan into a design requires a different mindset due to the different hardware, software, and test equipment needs versus traditional test methods, Designers are often uncertain as to exactly how they should begin, what issues must be considered, and what pitfalls await. The purpose of this report is to touch on some of the issues designers should consider when designing with off-the-shelf boundary-scan logic components.

Is JTAG Right for You?

As noted in the introduction, one of the first decisions you will face is whether using boundary scan is of benefit to you. The designer is faced with many issues that must be addressed when implementing boundary scan into a design, versus a design with standard components. A key concern is the fact that boundary-scan devices generally are priced slightly higher than their non-JTAG counterparts. However, as shown in Table 1, there are many situations where the additional material cost of implementing boundary scan is offset by a reduction in life-cycle costs.

Figure 2 provides two views of product life-cycle costs. The lower curve represents actual dollars spent. The upper curve illustrates that development decisions commit funds that other process steps must spend. By the time engineering "releases" a product to manufacturing, 85% of the project's total costs are committed. These costs are driven by decisions made during the design phase and can only be reduced if they are considered early in the design phase.

Both of the above examples illustrate that the goal of boundary scan is to reduce the product's life-cycle cost, even though board or system material costs may increase. The life-cycle cost reduction is achieved by enabling faults to be easily identified and isolated, reducing test development and execution time. Further cost reduction is achieved by reducing or eliminating the need for expensive test fixtures and equipment.



(from "Controlling Life-Cycle Costs Through Concurrent Engineering", Addendum to the ATE and Instrumentation Proceedings, Miller Freeman Expositions, 1992)

Figure 2. Life-Cycle Costs of Typical Product

The use of boundary scan can also have a positive impact on time to market, resulting in a maximization of profit potential. These benefits are discussed in greater detail throughout this document.

To make an accurate assessment of the benefits of boundary scan, representatives of all of the disciplines involved in the product's development must discuss their respective problem areas. Only then can a solution be reached that truly addresses the total product life-cycle cost. Several factors can be analyzed to determine the impact of boundary scan on your application:

Boundary Scan Can Reduce PCB Debug Time

By providing access to device I/O without probes, boundary scan allows you to quickly identify and isolate defects to the device and, often, the pin level. Boards that previously may have taken weeks to debug can now be tested in a matter of days or even hours. Additionally, faults that may not have been detected during board test can now be found, preventing faults from surfacing during final test when the costs of finding and repairing the failure are magnified.

Boundary-Scan Components Help Reduce Test Program Development Time

Because tests can be performed independent of device functionality, costly in-circuit test models do not have to be developed. Instead, the user can obtain boundary-scan description language files (BSDL) from the silicon vendor. These files describe how boundary scan has been implemented within the part so tools can understand how to communicate with it. Another key feature of boundary scan is that tests performed at the device level can be rerun at the PCB and system level, reducing or eliminating the need to develop new tests or generate new test vectors. (See Appendix B for examples of how other customers have benefited from the use of boundary scan.)

Boundary Scan Can Reduce the Need for Costly Fixtures

Boundary-scan testing of a PCB only requires the user to access the 4-wire JTAG bus. Thus, a PCB or system can be tested in its normal configuration without the need to develop fixtures for each PCB or subsystem.

Boundary Scan Can Reduce or Eliminate the Need for Test Points

By providing "virtual nails" to each boundary-scannable I/O, the designer no longer needs test points for standard in-circuit testers. Removing these test points reduces board manufacturing cost by reducing the number of board layers required.

Boundary Scan Can Reduce the Number of Pins Needed for In-Circuit Testers

Even if all parts on a PCB do not have boundary scan, all of the benefits discussed here still apply. You may still need to use in-circuit testers to access nonscan nodes. However, by reducing the number of test points needed, you also reduce the number of pins required for the in-circuit tester, which determines the type and cost of the tester needed. The cost of automatic test equipment of this type has risen to as much as $1.5M in the past several years. Reducing the complexity of the tester may mean being able to utilize a tester that is priced significantly less.

Boundary Scan Can Help to Perform Functional Testing

While boundary scan was invented to test for manufacturing defects, users are finding it valuable in doing a variety of functional tests. ASICs and microprocessors can make use of boundary scan to access internal registers and enable testing of the device itself. Clusters of nonscannable logic may be tested by using a boundary-scan device at the cluster input to drive a predetermined pattern. Additional boundary-scan devices at the output can capture the cluster output data and compare it to expected results. In the same manner, other devices such as memories can also be tested.

These are just some of the areas where boundary scan can be of use to you. In some cases you may want to consult with your test or manufacturing engineer to understand the problems they face since, in many cases, designers are unaware of the difficulties their designs pose to others later in the product life cycle.

The degree to which the use of JTAG components impacts your life-cycle development costs will depend on the specifics of your design. While it is not necessary to have a 100% boundary-scan board, the more controllability and observability you can gain by adding boundary-scan devices in key areas, the more benefits you will realize.

Boundary-Scan Training

Whether you are a hardware design engineer, ASIC designer, test engineer, or program manager, there are several options available for learning more about design for test (DFT) and specifically boundary scan. Texas Instruments (TI) has developed several testability training tools to aid you in finding out more about how boundary scan works and how it can benefit you. Some of these are listed below. For more information on available literature and training, please contact your local TI sales representative or authorized distributor.

TI Boundary-Scan Training

Scan Educator (SATB002A)

An educational software program, Scan Educator introduces the fundamentals of the IEEE 1149.1 boundary-scan standard, including architecture, protocol, and required instruction sets.

Self-paced and menu-driven, it contains both information and animated boundary-scan test simulations. Hands-on, practice exercises guide you through boundary-scan test of our SCOPE™ octals at the TAP and at the register level. You are also shown how to use IEEE 1149.1 with single or multiple devices for in-circuit observability and controllability and for interconnect testing.

Testability Primer (SSYA002C)

This pocket-sized book provides an introduction and indispensable reference to JTAG/IEEE 1149.1 testability. It includes discussion of cost benefits/trade-offs associated with design for test, a technical overview of IEEE Std 1149.1 and supporting data formats (BSDL, HSDL, SVF), and a set of application briefs. Summary information on TI silicon testability solutions and support and learning products is also included.

Testability Videotape

This two-part videotape provides a background of the growing need for testability and its economic impact. It also describes the work of JTAG and the provisions of the IEEE 1149.1 standard. Part two of the videotape examines the standard in detail. It explains the function of each component of the standard and shows how they work together to provide an accurate, dependable test procedure.

Testability CD-ROM

TI has assembled the key components of testability on a searchable CD-ROM that includes the IEEE Std 1149.1-1990 and IEEE Std 1149.1a-1993 merged into a single updated document, the TI Test Bus Evaluation Report, application notes on IEEE 1149.1, and device data sheets.

In addition to educational opportunities from TI, other vendors supplying boundary-scan products are usually able to provide training.

For more personal training, TI is also able to hold on-site meetings and seminars tailored to address the needs of your application. Please contact your local TI sales representative or authorized distributor.

Determining Where to Place Boundary-Scan Devices

Once you have become familiar with boundary scan, you will want to integrate it in your design. TI has a broad spectrum of boundary-scan devices available today:

- ASICs
- Fixed and floating-point digital signal processors
- Bus-interface ICs
- Scan-Support ICs

To identify which devices are needed and where they should be placed, there are several questions you should ask:

What Signals Do You Need to Control and Observe?

The boundary-scan standard allows you to take control of an I/O to either sample data at the pin or stimulate the pin with known data. By replacing standard components with JTAG-compliant devices, you can gain access to individual pins for a variety of tests.

Would You Like to Use Boundary Scan to Test Nonscan Logic Clusters?

By having the ability to control and observe device I/O, you can use scannable devices to test devices without JTAG capability. One JTAG device can be loaded with a predetermined pattern that can be driven onto the cluster inputs while additional JTAG devices can capture the output information to be compared against the expected result.

Do You Need Embedded Test Capability?

In support of applications requiring a JTAG controller to be "embedded" within the design, TI has developed devices that can translate parallel commands from a processor into the required JTAG protocol to drive the JTAG bus. For embedded applications, TI has developed a software driver for this bus controller that can be compiled with user code to execute pass/fail tests stored in memory.

Will You Be Implementing Built-in-Self-Test Capability in Your Design?

If you would like to have your board/system execute some form of self test, TI has devices that can help. Within each TI bus interface device lies the ability to execute instructions that command the device to automatically generate output patterns. This capability can reduce or eliminate the need to develop test patterns, as well as significantly reduce the time involved to execute some tests.

What Performance Requirements (Speed, Power, Drive) Are Needed?

The constraints of your design will determine the technology you require in a bus-interface device. TI's JTAG family contains over 20 devices and crosses a variety of technologies, giving you the ability to pick the device that best suits your needs. Table 2 below provides an example of the performance differences between TI's BCT and ABT technologies versus competing technology.

Table 2. Performance Comparison, JTAG Transceiver Functions

SPECIFICATION	BCT (TI)	ABT 18-BIT (TI)	FACTQ (NSC)
tp A/B to B/A	10 ns	5.4 ns	8.8 ns
Maximum TCK rate	20 MHz	50 MHz	25 MHz
Number of bits	8	18	18

Based on comparison of TI BCT8245 and ABT18245 vs. NSC SCAN18245.

Will You Require Devices That Operate From 3-V Power?

With more systems moving toward 3-V power, TI has developed 3-V versions of our more popular JTAG Widebus™ devices. These devices are designated as LVTH18xxx. Universal bus transceiver (UBT™) functions are also available now.

Will You Need to Drive JTAG Signals Across a Backplane?

As boundary scan gains acceptance at the board level, the need to perform system-level tests with boundary scan is creating an interesting problem for test engineers. While several approaches have been proposed to date, none addresses the problem better than TI's ABT8996 addressable scan port. This device provides a simple approach to solving a very complex problem without the overhead associated with competing solutions.

What Function Type, Bit Width, or Packaging Limitations Do You Have?

There are many more boundary-scan functions available on the market today than there were even one year ago. Designers are able to select a device based on the functionality, performance, and board area limitations of their design. Boundary-scan buffers, drivers, transceivers, latches, and flip-flops are available in a variety of technologies. TI is the leading supplier of JTAG logic, with over 30 device types available now.

What Type of Test Equipment Do You Expect to Use?

To make the conversion to a test philosophy based on boundary scan, you should define your design, manufacturing, test, and field support flow before beginning hardware design. The details of this test plan will determine the types of tests to be performed, the devices to be used and their placement, and, therefore, the equipment that will be required. There are several vendors supplying CAE and ATE tools to the market today in support of boundary scan.

Will You Need to Use Bare Die for Use in Multichip Modules?

Multichip modules epitomize the problem of no physical access. Boundary scan can be very beneficial by providing you access to internal signals of the MCM. TI supports this effort by supplying bare die for all of its standard components. Additionally, special devices such as the ACT8994 digital bus monitor can give you logic-analyzer capability within the MCM via the JTAG bus.

What Type of Field-Service Requirements Will You Need?

With boundary scan, you now have the ability to access your circuitry via the 4-wire JTAG port without having to totally disassemble the unit. This provides many options to support field maintenance. Will you want the system to execute system self-test and simply notify the end user as to the source of the fault? Or will the system execute self test and then remotely dial back to the factory with the fault? Will a technician go out to the customer site and connect to the JTAG port with boundary-scan diagnostics on a PC to identify the fault? Each of these options and others are available to you because of boundary scan. The option you choose will depend on the ramifications of system downtime to you and your customer and should assist you in determining your use of boundary-scan devices.

The answers to these questions will determine which products you will need, where they should be placed, and what tools and equipment you will require. Additionally, as you begin to understand the types of boundary-scan components that are needed, you will make decisions as to which vendor is best able to support your testability needs. The TI SCOPE family of testability products is the most comprehensive in the industry and is backed by many years of working with customers and other vendors to solve complex testability problems.

Available Literature on TI's JTAG Boundary-Scan Logic Products

The items below contain information on TI's bus-interface and scan-support products that are compatible with the JTAG standard. To obtain a copy of any of these items, please contact your local TI sales representative or authorized distributor.

- Boundary-Scan Logic IEEE Std 1149.1 (JTAG) Data Book 1996 (SCTD002A)
- Testability Primer (SSYA002C)
- Testability CD-ROM
- World Wide Web – URL = http://www.ti.com/sc/docs/jtag/jtaghome.htm

Acknowledgment

The author of this document is Johnny Young.

Appendix A – Basics of Boundary Scan

Boundary scan involves placing test points (boundary-scan cells) within each digital I/O of a device. The boundary-scan cell enables the I/O to observe normal data flow through the pin, or the cell can be used to control the state of a pin by providing source data via the serial input (SI). Figure 3 provides a view of the typical boundary-scan cell.

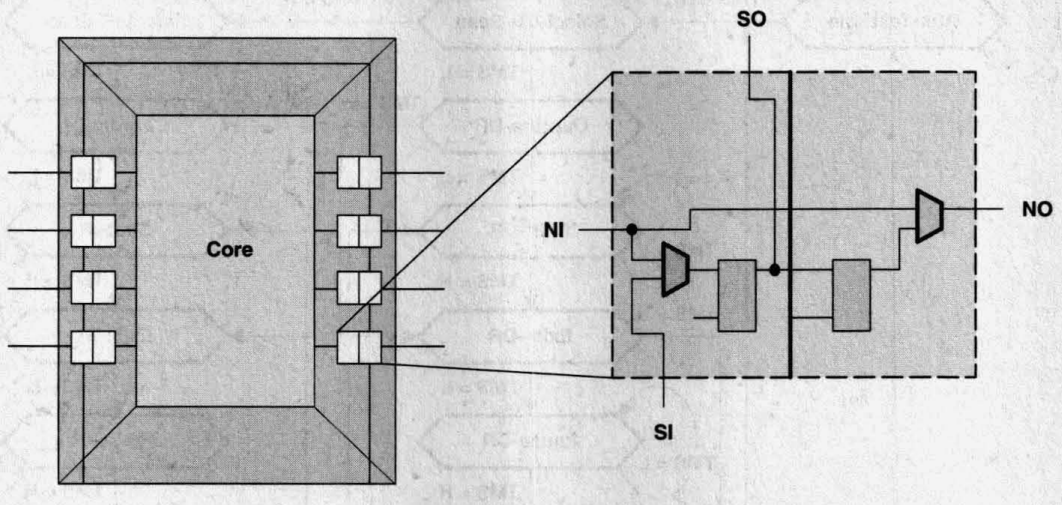


Figure 3. Boundary-Scan Cell

Each boundary-scannable device will contain a minimum of four additional pins:

TDI – test data input
TDO – test data output
TMS – test mode select
TCK – test clock

The TDI and TDO pins serve as the path by which serial data enters and exits the device. The TMS and TCK pins control the state of the device, placing it in either test mode or normal mode. In some cases, an optional fifth pin, test reset (TRST) may be included to reset the test logic and return the device to normal mode. Figure 4 shows these four pins as implemented in one of TI's SCOPE octals.

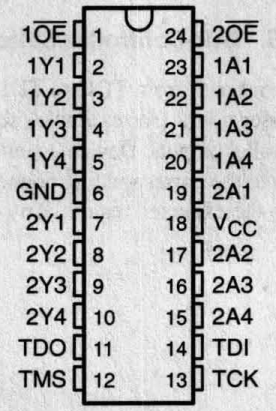
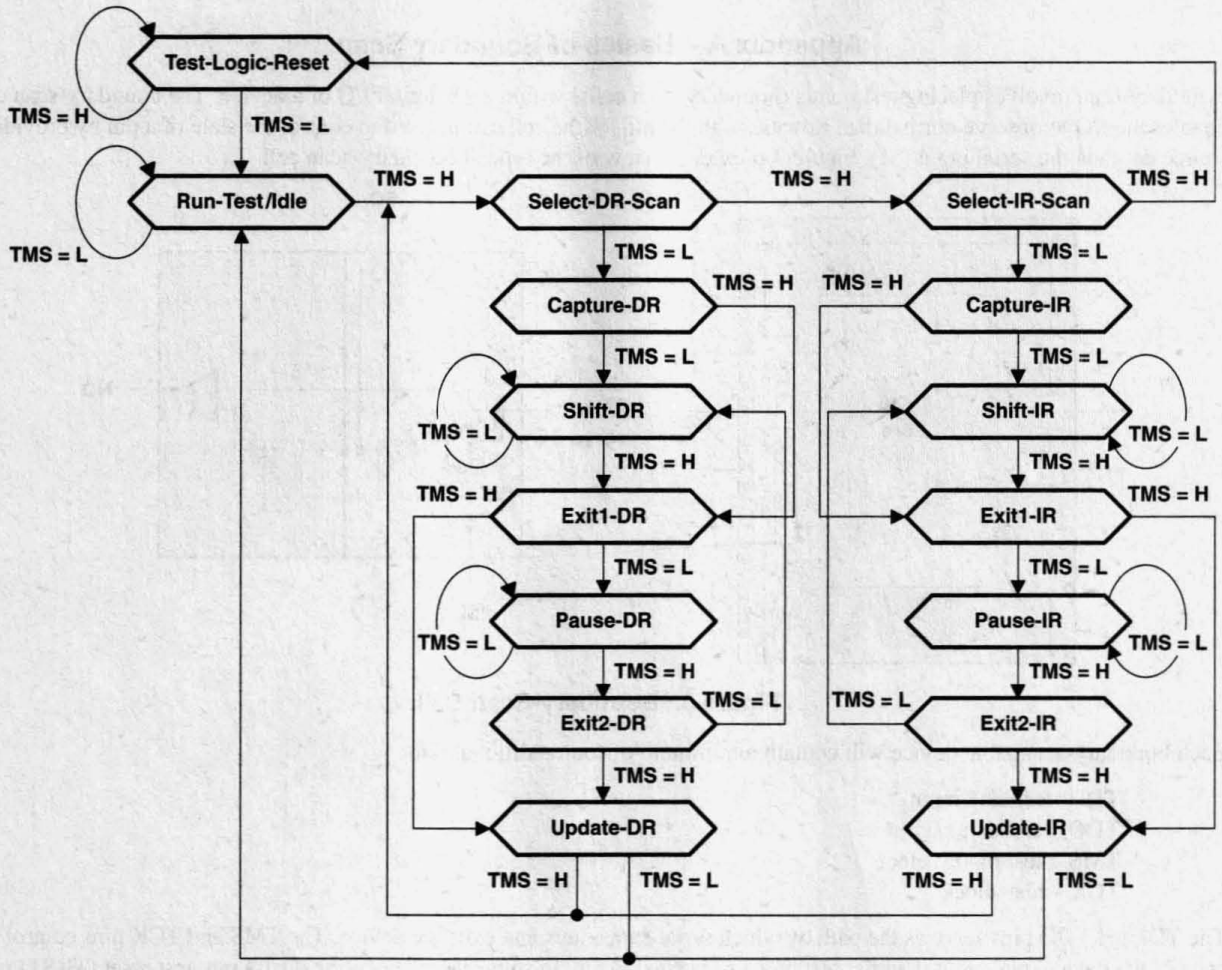


Figure 4. Pinout of TI's SN74BCT8244

The TMS and TCK signals serve as inputs to control the transition of the device between normal and test modes. These inputs drive a state machine known as the test access port (TAP). The TAP controls serial scanning of instruction or data information through the device and is common to all JTAG/IEEE–1149.1-compliant devices. The TAP state is sequenced based on the state of TMS on the rising edge of TCK, as shown in Figure 5.



TMS input value for state transitions
16-State TAP provides four major operations: RESET, RUN-TEST, SCAN-DR, and SCAN-IR.
Scans consist of three primary steps: CAPTURE, SHIFT, and UPDATE.

Figure 5. TAP-Controller State Diagram

Boundary-scan devices communicate via the serial path from TDO to TDI. This connection is shown in Figure 6. To test the interconnect between two JTAG devices, the user could (for example) serially shift all ones into device 1 and execute an instruction that would drive the data onto the parallel outputs. Device 2 could then be commanded to capture the incoming data at its parallel inputs, transferring the information to the corresponding boundary-scan cells for each input and then serially shift the data to an off-board tester to be compared to the expected results. Any discrepancies in the data can be traced back to the pins where the data mismatch occurs.

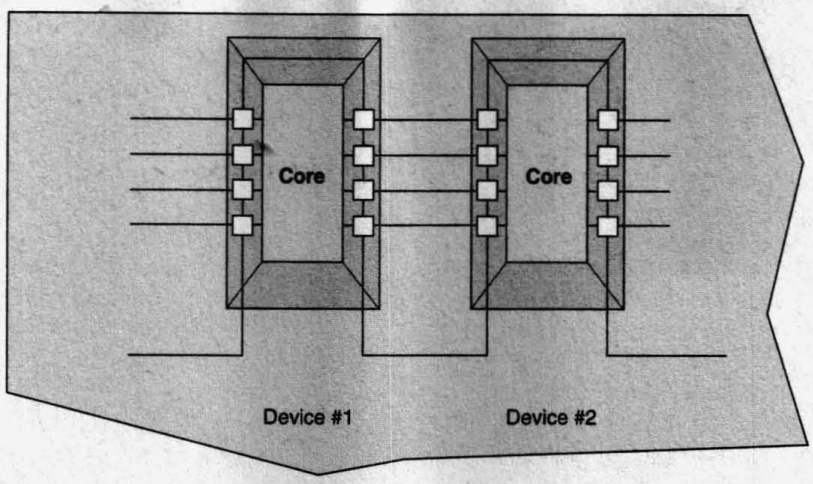


Figure 6. Scan Path Connecting Two Boundary-Scan Devices

For more detailed information on boundary scan, please use the boundary-scan training materials cited in this report.

Appendix B – Boundary-Scan Success Stories

- "We've (AT&T) reduced the number of test points on some boards from 40 down to four and shortened test – debug time on some products from six weeks to two days."[1]

- Hewlett Packard printers reduced the time from the drawing board to production from four and one-half years to two years.[2]

- Test program development time on Intel '386 vs. Intel '486 with JTAG:[3]

Intel '386	Intel '486
7 weeks	10 hours (2 hours if vendor supplied BSDL)

- Controller design company using two programmable logic devices with boundary scan were able to use low-cost tester with ATPG ($25K) instead of standard ATE system ($750K) that would have been used without boundary scan.[4]

[1] Computer Design, January 1994, "Testing Dilemmas and Corporate Alliances Fuel Boundary Scan's Acceptance"

[2] Test and Measurement World, October 1992, "Concurrent Engineering is Common Sense"

[3] Computer Design, November 1992, "Design and Test Engineers Alter Rules to Facilitate Test"

[4] EDN, December 3. 1992. "No 'Accounting' for Boundary Scan Test"

A Look at Boundary Scan From a Designer's Perspective

SCTA028
August 1996
Reprinted with permission from Proceedings of Electronic Design Automation & Test Conference Asia, Taipei, Seoul, Beijing, October 26–November 5, 1994.
© 1994 Asian Sources Media Group

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	*Page*
Abstract	**7–61**
Background	**7–61**
Use of the Standard by the Board Designer	**7–64**
Use of the Standard at Chip Level	**7–68**
Use of the Standard at System Level	**7–69**
Conclusion	**7–70**
Acknowledgement	**7–70**
References	**7–70**

List of Illustrations

Figure	*Title*	*Page*
1	The Incredible Shrinking Board Results in Loss of Test Access	7–61
2	Increasing Integration at Chip Level Complicates Controllability	7–62
3	Traditional Methods of Board Test	7–62
4	The Boundary-Scan Idea	7–63
5	The Boundary-Scan Control Architecture	7–63
6	Board-Level Boundary-Scan Path	7–64
7	IEEE 1149.1 in Action	7–65
8	Logic Cluster Test	7–66
9	Scan-Path Management	7–67
10	Boundary Scan Plus Internal Scan in Mixed-Signal Circuit	7–68
11	Multidrop System TAP	7–69

Abstract

Much attention has been focused in the past on the benefits of boundary scan to the manufacturing test process and the test engineer. While ultimately the decision to use boundary scan in a given project should be based on positive impact to product life-cycle cost, the benefits that accrue to the designer are often overlooked. This paper describes such benefits to designers at all levels of product design: chip, board, system. It also provides insight into special considerations for the designer who implements or uses boundary scan.

Background

Beginning in 1985, several European and North American companies banded together to form the Joint Test Action Group (JTAG). Their stated task was to solve the problem of printed-circuit board (PCB) manufacturing test, which was growing more difficult as integrated circuits (ICs) became smaller and more complex (see Figures 1 and 2).[1,2] Their solution was eventually standardized as the IEEE Std 1149.1-1990 Test Access Port and Boundary-Scan Architecture. This standard provides for inclusion of required test resources into ICs themselves.[3]

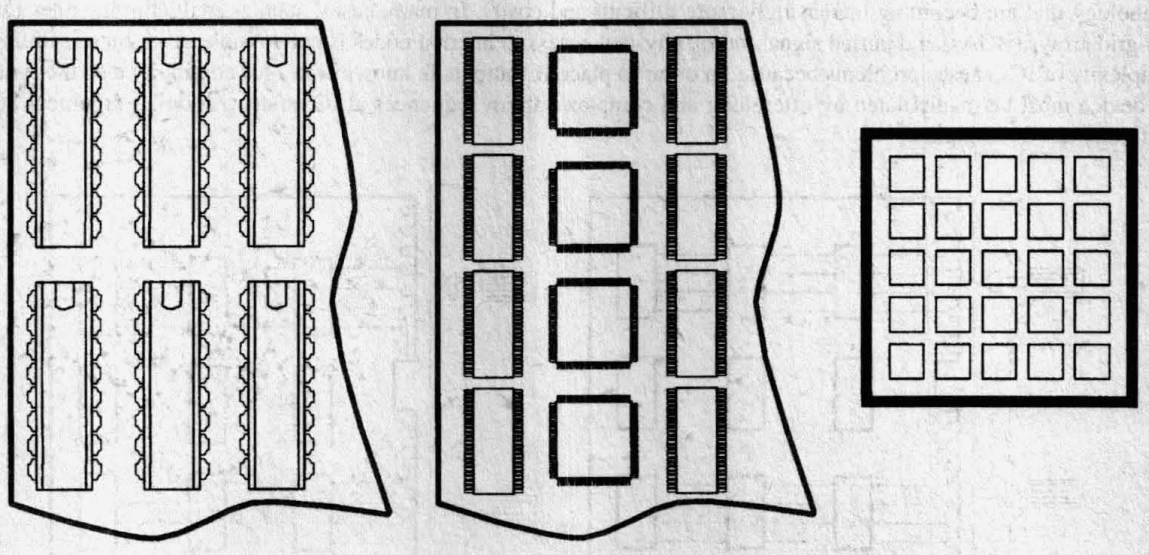


Figure 1. The Incredible Shrinking Board Results in Loss of Test Access

Manufacturing test of PCBs is essentially an effort to find defects (such as net-to-net shorts and solder opens) in the assembly of ICs and other components onto a board. This effort is obviously made more difficult by ICs that are both smaller and more complex. The ability of functional ("edge-connector") test to isolate PCB assembly defects to an adequate level is quickly thwarted by increased board functional density (see Figure 3). Since only the primary input/output are used for the test, the difficulty of test generation and the requisite test length grow dramatically as the board complexity increases.[1,2,4]

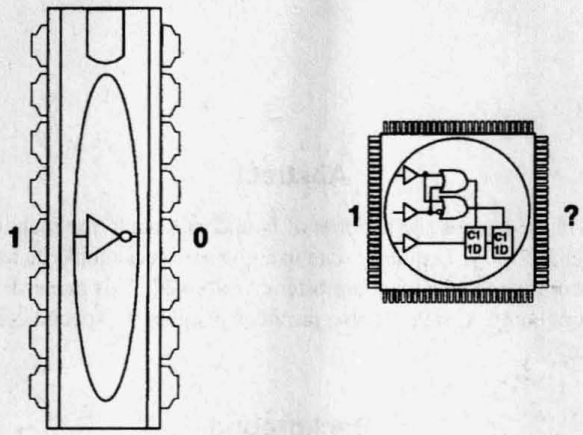


Figure 2. Increasing Integration at Chip Level Complicates Controllability

In-circuit ("bed-of-nails") test, which was an earlier attempt to improve fault isolation in complex boards, is likewise thwarted by increased IC functional density and, further, by physical constraints (see Figure 3). Since in-circuit test is based on the physical probing of (preferably all) nets internal to a PCB, smaller pin-to-pin spacing requires improvements in probe technology that are becoming increasingly more difficult and costly. In many cases, such as multichip modules (MCMs), ball-grid arrays (BGAs) and buried signal traces, physical access to internal nodes is not possible at all. Increased functional complexity of ICs causes problems because, in order to place IC outputs in known states for continuity test, the function of the device must be manipulated by often long and complex pattern sequences at IC inputs. A similar argument holds for continuity test at IC inputs.[1,2,4]

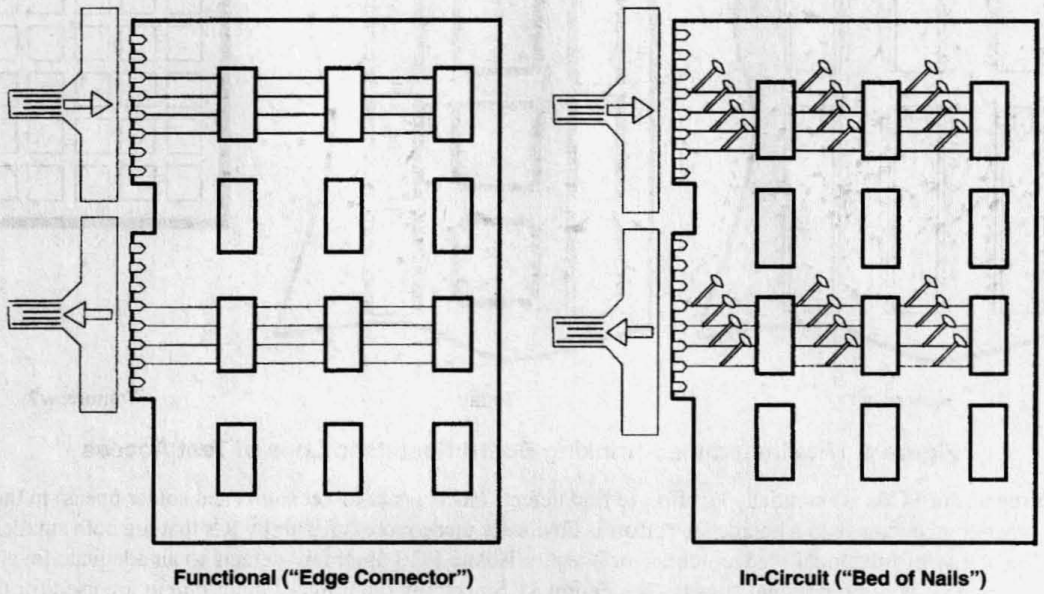


Figure 3. Traditional Methods of Board Test

The boundary-scan idea builds on the concepts of in-circuit test. However, physical probes ("nails"), which are placed mid-net, are replaced by boundary-scan cells (BSCs). These "virtual" probes are placed on-chip at IC inputs and outputs (the boundary of the IC), and are therefore placed at the net ends (see Figure 4). This results in two major improvements: (1) physical access is no longer required at boundary-scan nets, and (2) continuity test is no longer subject to IC complexity. The net effect is that the goal of manufacturing test, to isolate defects in assembly process to a pin or net, can be accomplished by highly automated test-pattern generation (ATPG).[2]

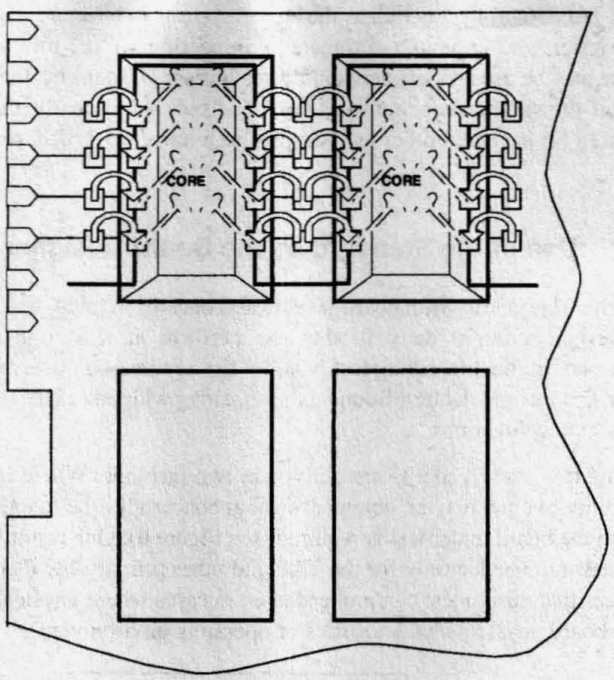


Figure 4. The Boundary-Scan Idea

Finally, in order to provide a means to arbitrarily control and observe these BSCs with minimal pin overhead, the BSCs are designed such that they can be serially concatenated to form a shift register between two IC pins, Test Data Input (TDI) and Test Data Output (TDO). The additional control structures required to select between normal and test operational modes have also been designed to minimize pin overhead and to maximize flexibility to handle test modes in addition to that used for PCB manufacturing test (see Figure 5). This Test Access Port (TAP) is based on a state machine (TAP Controller) that operates synchronously to a Test Clock (TCK, to which all operations of the test logic are synchronous) and under the control of a single Test Mode Select (TMS). The TAP Controller explicitly provides for a single instruction register that controls the test modes and for any number of test data registers (including the boundary-scan register) that can be selected by specific instructions.[2]

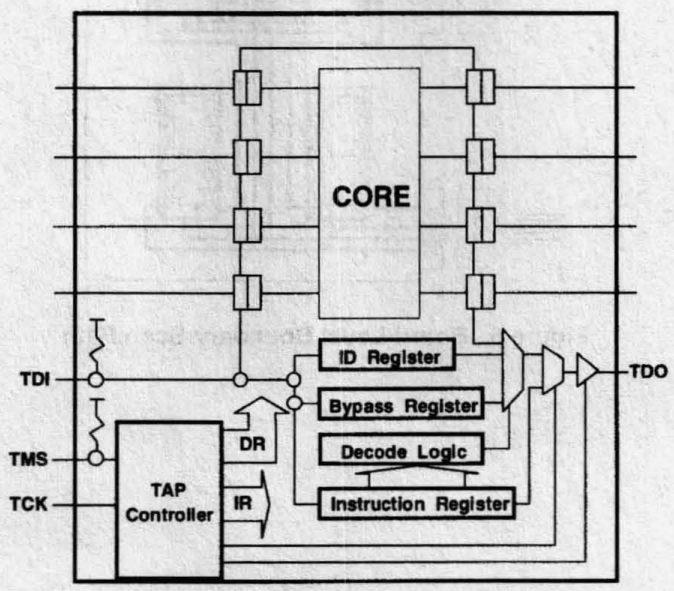


Figure 5. The Boundary-Scan Control Architecture

Standardization of the TAP and TAP Controller, as well as the boundary-scan architecture, has been key to the broad acceptance of the technology across IC, tester, and computer-automated engineering (CAE) tool vendors. Thereby, this structured design-for-test (DFT) technique may be used widely across all types of board designs by all sorts of board manufacturers, even those where catalog ICs and off-the-shelf testers and tools must be used. Additionally, the flexibility of the TAP and TAP Controller allows them to be used for access to other test features built into chip, board, or system, such as on-chip scan test or built-in self-test (BIST).[2]

Use of the Standard by the Board Designer

Since the standard has been designed primarily with board-level (test) concerns in mind, we can expect many benefits for board designers. Although many designers might deny it, they do perform at least one critical "test" operation: design verification/debug. And, just as board manufacturing test benefits from increased observability and controllability, so does board design "test" (that is, verification and debug). Boundary scan, along with other DFT techniques applied at chip or board level, can greatly aid these design test functions.

As in the case of manufacturing test, these benefits are derived in two fashions. Where boundary-scan access is provided, observability and/or controllability of a net may be obtained without concern for the function of the driving and/or receiving ICs. Also, no physical access to the board under test is required (see Figure 6). One result is that inexpensive test equipment can be used, since tester channels are needed only for the TAP and other primary I/O ("edge connector") signals. Another, perhaps more important result, is that design test can proceed even in cases where physical access to board internal nodes is difficult or impossible (due to board physical characteristics or operating environment[5]).

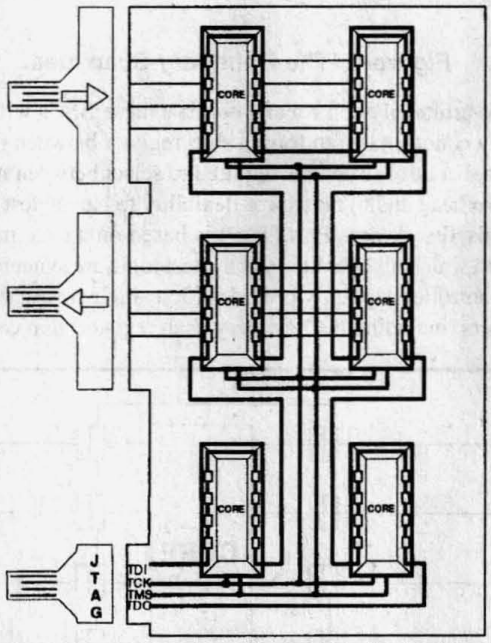


Figure 6. Board-Level Boundary-Scan Path

In the design CAE environment, the designer could have virtually any desired level of observability and controllability to board-internal and (in case of ASICs, FPGAs, or PLDs) chip-internal nodes. With the appropriate boundary-scan and chip-internal scan facilities, the designer can enjoy this same level of access to such nodes in the prototype. Further, a structural ("assembly") test of the prototype can be generated that can be applied from this inexpensive test equipment and without need for expensive test fixturing. Such a test can be automatically generated, given the board netlist and descriptions (in the boundary-scan description language, BSDL) of the boundary-scannable devices. This simple test is available even when manufacturing test program, equipment, and fixtures are not (as is most often the case for prototypes, since they are difficult to provide for an unproved design). Such a test can save many frustrating hours (a testimonial indicates a reduction from 6 weeks to only 2 days[6]) which would normally be required to separate assembly problems from design problems. This is especially important if new and unproved assembly processes have been developed for the board.[5,7,8,9,15]

In some cases, the provision of boundary scan and DFT can permit some prototype testing to begin even in the absence of "key" components. For example, if a processor board were designed with proper planning, associated memory could be tested by emulating the processor, or vice versa.[10]

In addition, the actual design time and manufacturing cost of PCBs may be reduced by elimination of test points.[7,11] If enough test points can be eliminated (one example cites a reduction from 40 down to 4[6]), then possibly some PCB layers can be eliminated as well, which might greatly decrease PCB cost. In some cases, such elimination of test points may be critical to the very miniaturization goal that drives the choice of extremely dense packaging options such as BGAs.[6]

The board designer can obtain these benefits by specifying the use of boundary scan in proprietary ASICs and by placing boundary-scannable catalog (including user-programmable) components wherever possible. The task of finding such components is becoming less difficult daily as the number of such products grows. As of this writing, it has been reported that boundary scan is supported by 22 ASIC vendors, 24 vendors of over 120 standard components and 12 vendors of user-programmable logic (see Figure 7).[12]

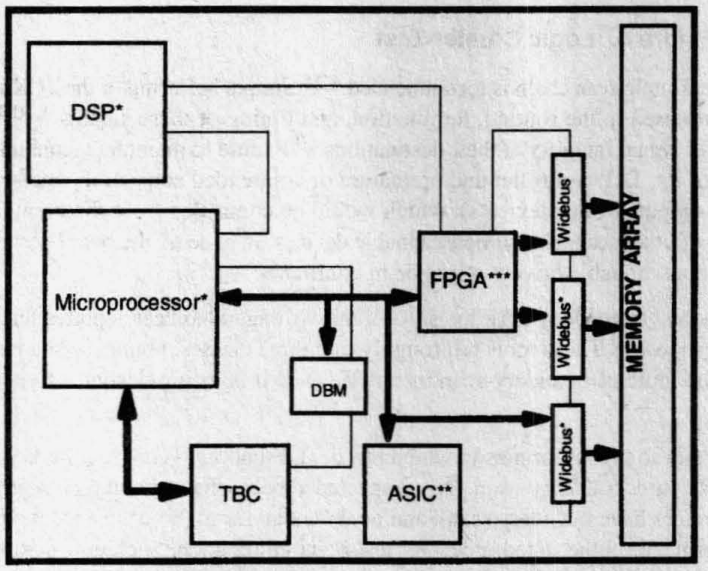


Figure 7. IEEE 1149.1 in Action

Included in such offerings are boundary-scannable bus-interface devices. These reasonably inexpensive components can replace their nonscan counterparts to gain all the above benefits. It may be useful in some cases to insert such devices even where they are not required for normal system function (for example, in parallel to a bus that is not boundary-scannable for performance reasons) in order to improve test access.[13] Often such components may bound simple clusters of nonscannable logic that can be tested using the "virtual nails" of these devices for simple "virtual" in-circuit testing (see Figure 8). Additionally, some vendors offer built-in parallel-output pattern generators and parallel-input signature registers that allow the board designer to implement board-level BIST capabilities that provide high fault coverage with very little test pattern generation.[7,14]

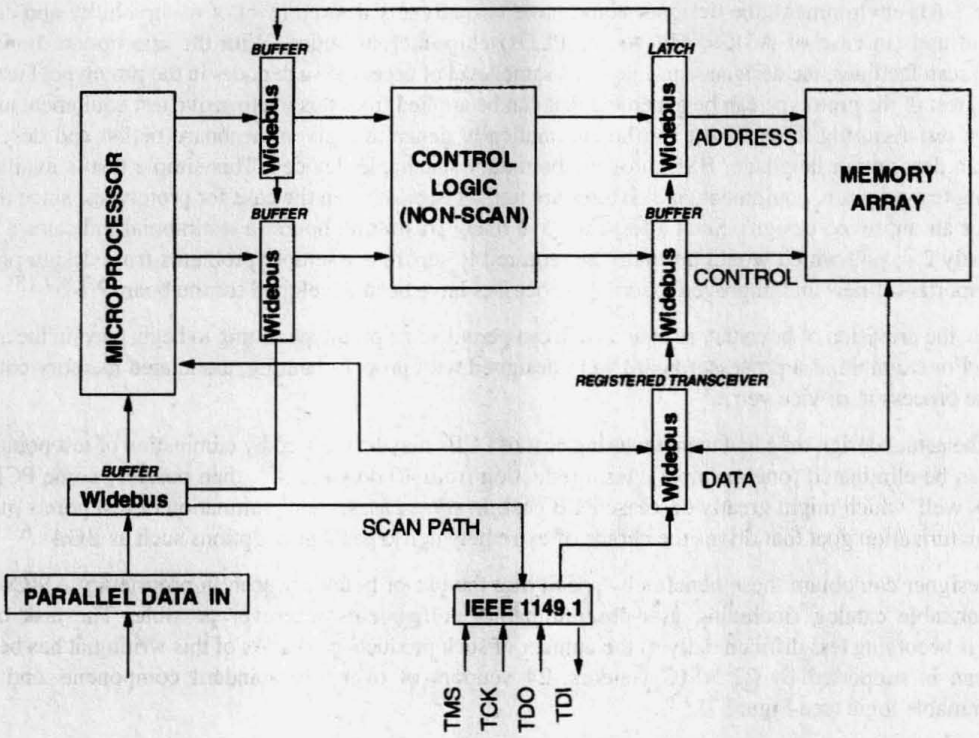


Figure 8. Logic Cluster Test

In designing the board-level scan chain, a single, simple scan chain is recommended.[4,15] Simple buffering of the TCK and TMS signals should be used, and care should be exercised in the routing, termination, and timing of these signals.[4,10,14] In the prototype, all TAP signals should be checked for signal integrity at their destinations.[10] Failure to maintain signal integrity at these signals may cause improper movement of the TAP controller and premature or unintended entry of device(s) into test modes, such as EXTEST. In such modes, the outputs of the device(s), which would be controlled from the boundary-scan register, might come into contention with those of other scannable or nonscannable devices. In general, the board designer must beware of conditions in which scannable and nonscannable drivers might be in conflict.[4]

Another key to obtaining such benefits will be access to enabling CAE tools. As of this writing, it has been reported that 14 CAE vendors supply tools that support boundary-scan test.[12] These tools fall roughly into three classes: boundary-scan insertion, access analysis, and boundary-scan ATPG. The topic of boundary-scan insertion, since it is a chip design activity, will be discussed later.

Access analysis tools examine board designs prior to layout for nets to which physical test access is not required. Such tools will identify nets in at least three categories: pure boundary-scan (all connected devices have boundary scan), mixed boundary-scan (some, but not all connected devices have boundary scan), and nonboundary-scan (no connected devices have boundary scan).[16] These nets will then be prioritized (in the stated order) for test-point elimination. Such information is then passed to a layout tool (or designer) for elimination of the test points, as required for optimal board layout and fabrication cost.[17]

Boundary-scan ATPG tools automatically generate prototype or manufacturing tests to be applied to the board under test using the board-level TAP. Some of these tools can consider physical access (via in-circuit "bed-of-nails") as well. The best-in-class tools of this type will generate tests for TAP and BSDL validation, and board-level scan-path integrity. These tests, in combination, verify the infrastructure for applying remaining tests. The best-in-class tools generate the following additional types of test for board structural test: boundary in-circuit, virtual interconnect and interactions, and virtual cluster/component test. Boundary in-circuit test uses physical access, but utilizes boundary-scan for simple access to on-chip inputs and outputs for reduced test generation time and complexity. Virtual interconnect and virtual cluster/component tests allow for removal of some or all physical access for test of interconnect and of nonscannable logic clusters, respectively. Such tests will include diagnostics of board assembly faults to the pin. Some tools support multiple board-level scan chains, while others support only a single chain.[6,12,16,17,18]

Some means of boundary-scan test application is required. In some cases, this may be in-circuit or board-functional test equipment that is already owned, perhaps with some modifications to handle deep serial patterns. In other cases, it may be an inexpensive test adapter for PC or workstation. Such "testers" must, at a minimum, exercise the board-level TAP(s) under control of a simple vector file. In either case, to get the most out of boundary scan in design debug, an interactive scan-based diagnostic capability is desired.[10]

The best scan-based diagnostic tools will use a scan-path management database that permits interactive view and control of only those portions of the board (pin, register, bus, or user-defined signal group) that are of interest (see Figure 9). Such tools completely hide the complexity of the TAP protocol and boundary-scan chain from the user and allow efficient design debug in the fashion of parallel stimulus generators and logic analyzers to which the design engineer is accustomed. In fact, the best such tools include logic-analyzer-like waveform and state table displays.[19]

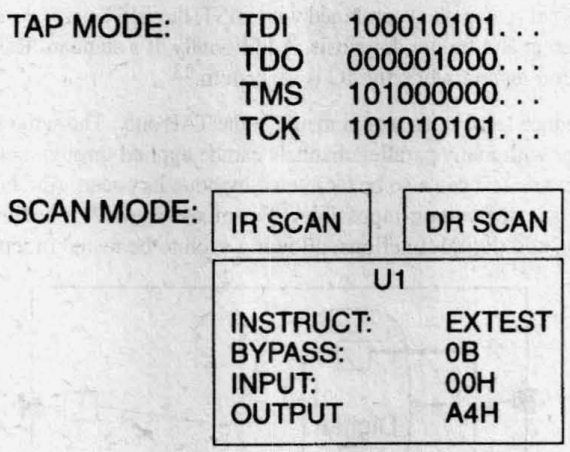


Figure 9. Scan-Path Management

Such tools should also support multiple test vector generation methods: interactive, CAE parallel (with automated serialization), and boundary-scan ATPG (based on a standard interchange format such as the Serial Vector Format, SVF). They should also describe the boundary-scan hierarchy using industry standard formats such as BSDL, the Hierarchical Scan Description Language (HSDL), and EDIF (Electronic Design Interchange Format) netlist. And, they must be sensitive to board-level constraints so that physical damage to the board, which might result from improper control of boundary-scan drivers, does not occur.[19]

Finally, they must support scan test and test reuse across all product phases. This means they must allow access to chip-internal scan and BIST, as well as board-level BIST capabilities. They must provide a flow of test information from chip to board to system. Ideally, they will provide a flow to embedded system test, enabling system built-in test based on reuse of scan-based test.[10,19]

Use of the Standard at Chip Level

At chip level, the standard provides most benefit in its provision for a standard test access method (the TAP) which allows access to chip-internal test facilities in addition to the required boundary-scan test facilities. Such chip-internal test facilities include internal scan path, BIST, and built-in emulation and debug.[5,7,8,10,17,20]

Chip-internal scan path involves the substitution of normal storage elements (latches and flip-flops) with scannable counterparts that can be serially interconnected for test purposes. In a full-scan approach, all such storage elements are replaced, and the circuit is thereby partitioned into blocks of combinational logic between parallel inputs and outputs of a simple shift register. Robust combinational ATPG algorithms can then be used for rigorous structural test of the chip logic. Partial scan implies the replacement of only selected storage elements. It is used in cases where chip area and performance cannot be traded-off for improved fault coverage. However, since not all storage elements are scanned, some sequential ATPG must be used. The failing of such ATPG to provide adequate fault coverage is the primary reason for adopting chip-internal scan in the first place.[21]

BIST uses on-chip stimulus generators and response monitors to eliminate the need for any test generation. Most commonly it uses pseudo-random pattern generation and signature analysis (cyclic redundancy checking) implemented in linear-feedback shift-registers (LFSRs). In such cases, care must be taken that the circuit to be tested is not resistant to pseudo-random techniques. Where the circuit is not suitable for pseudo-random techniques, deterministic BIST methods are possible.[22]

Such features are often most powerful when used in combination. For instance, if boundary-scan and chip-internal scan path are both implemented so that they may be used simultaneously in a given IC, then static test application requirements can be reduced to only the four TAP signals, since the boundary-scan register can control/observe the primary inputs/outputs to the core logic (see Figure 10).[22] If internal scan path is combined with BIST, the BIST may be used for quick pass/fail testing while the internal scan is used for chip debug and failure diagnosis. Additionally, if a standard RUNBIST capability is provided, the end user may perform quick function testing while the IC is in-system.[23]

Finally, boundary scan alone can reduce test access requirements to the TAP only. The same static functional vectors that would be applied by an expensive IC tester with many parallel channels can be applied through boundary scan (if INTEST capability is provided). Setup of ICs for parametric test can also be facilitated by boundary scan. And boundary scan can be used in hostile environments where physical access is difficult or impossible.[5] For mixed-signal ICs, inclusion of boundary scan can provide a very useful partitioning of analog and digital functions, allowing each to be tested independently (see Figure 10).[24]

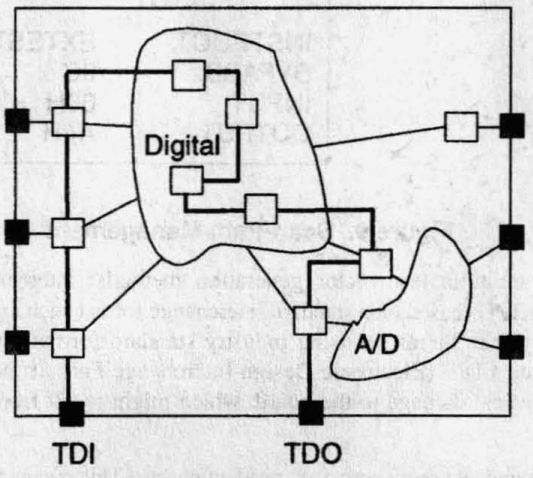


Figure 10. Boundary Scan Plus Internal Scan in Mixed-Signal Circuit

To benefit from these capabilities, they must be designed into the chip. Several types of CAE tools can aid this process. Most such tools provide for some level of automation of internal (full or partial) scan, BIST, and boundary scan. The abstraction level at which these tools operate ranges from register-transfer level down to gate level, and the point of use ranges from pre-synthesis to post-synthesis (or schematic capture). In the area of internal scan insertion, the best tools will provide full scan insertion and partial scan insertion driven from chip area, performance, and test coverage constraints. They will also provide the combinational and/or sequential ATPG needed to capitalize on the scan path.[6,12,21]

Boundary-scan insertion tools are similarly varied. Capabilities to look for besides automated insertion of TAP and boundary-register are BSDL output, test pattern generation for standard-conformance checking and BSDL validation. Some tools use BSDL (or graphical entry) as an input, rather than an output, to the boundary-scan insertion process.[18]

The need for validation of BSDL and TAP integrity cannot be overstated since the entire test infrastructure is based upon proper operation of these components.[4,17] Special attention should be given to TAP pin placement and to considerations for proper clocking of internal scan path relative to boundary-scan path.[4,25]

Use of the Standard at System Level

Finally, the standard can bring benefits to design at system level also. Such benefits are primarily derived from the ability for TAP-accessed tests to be reused at higher levels of product integration, from chip to board to system.[1,7] These capabilities may be used for system hardware debug and hardware/software integration while chips and boards are in their normal system configuration and operating environment. Since no physical access is required, use of "extender" cards, complex connectors, and large environmental control systems is not needed.[5,7,8]

Additionally, boundary scan and other TAP-accessed test facilities may be useful in meeting system design requirements for built-in test, field service test, and remote diagnostics. Clearly, in most such cases it is desirable to limit the expense and complexity of test equipment required. Boundary scan can facilitate this by limiting test access and control requirements to an inexpensive diagnostics port (the TAP).[7,20]

Boundary-scannable bus-interface devices can be useful in these applications, as well, by partitioning the system along field-replaceable unit (PCB) boundaries. Also, if the backplane interface of PCBs is scannable, then backplane connectivity and integrity testing can be performed. By using the previously mentioned pattern generation and signature analysis techniques, it is even possible to perform gross performance testing on the backplane.[14]

One problem in the area of system implementation of TAP access is referred to as the multidrop problem (see Figure 11). Since TDI and TDO are serial terminals, they must be daisy-chained in simple chains. This "ring" configuration presents a problem in backplane-oriented systems, since some boards may be removed, disabling the scan chain. An alternative, proposed by the standard, is the "star" configuration which allows TDI and TDO pins on PCBs to be bussed.[3] However, since multiple TMS signals are required to prevent simultaneous scanning (and thereby contention on TDO bus) of PCBs, many backplane routing channels are required. Several alternative multidrop schemes, based on serial addressing techniques, have been proposed to alleviate this problem. The best of these techniques will enable multidrop routing of backplane signals, with minimal need for test reformatting and minimal impact on test application time.[1,4,6,7,20,26]

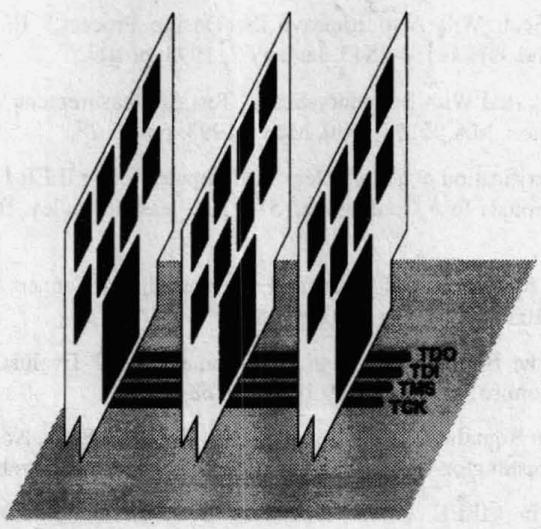


Figure 11. Multidrop System TAP

Conclusion

We have discussed many benefits that are available to designers through use of the Test Access Port and Boundary-Scan Architecture. These benefits are primarily in the area of design verification and debug and are enabled by improved controllability and observability into circuits, and freedom from physical access constraints provided by boundary scan. While some effort is certainly required to derive such benefits, a suite of CAE tools that reduces such effort has been presented. Designers at all levels of product integration (chip, board, system) are encouraged to evaluate boundary scan for benefits that they and their companies may derive from its use.

Acknowledgement

The author of this document is Adam W. Ley.

References

1 Harry Bleeker, Peter van den Eijnden, Frans de Jong, Boundary-Scan Test - A Practical Approach, Kluwer Academic Publishers, 101 Philip Drive, Assinippi Park, Norwell, MA 02061, 1993.

2 Colin M. Maunder, Rodham E. Tulloss, ed., The Test Access Port and Boundary'-Scan Architecture, IEEE Computer Society Press, 10662 Los Vaqueros Circle, PO Box 3014, Los Alamitos, CA 90720-1264, 1990.

3 IEEE Std 1149.1-1990 (includes IEEE Std 1149.1a-1993), IEEE Standard Test Access Port and Boundary-Scan Architecture, Institute of Electrical and Electronics Engineers, 345 East 47th Street, New York, NY 10017, October 1993.

4 Kenneth P. Parker, The Boundary-Scan Handbook, Kluwer Academic Publishers, 101 Philip Drive, Assinippi Park, Norwell, MA 02061, 1992.

5 Peter Fleming, "Applications of IEEE Std 1149.1: An Overview," The Test Access Port and Boundary'-Scan Architecture, IEEE Computer Society Press, 10662 Los Vaqueros Circle, PO Box 3014, Los Alamitos, CA 90720-1264, 1990.

6 Mike Donlin, "Testing Dilemmas and Corporate Alliances Fuel Boundary Scan's Acceptance," Computer Design, PennWell Publishing Company, Ten Tara Blvd, Nashua, NH 03062-2801, January 1994, pp. 65-70.

7 Johnny M. Young, "JTAG/IEEE 1149.1 Design Considerations," Testability Products Data Book, Texas Instruments, PO Box 655303, Dallas, TX, 75265, 1994.

8 Peter Hansen, "Boundary Scan Will Also Improve the Design Process," Electronic Design, Penton Publishing, 1100 Superior Ave., Cleveland, OH 44114-2543, January 7, 1993, p. 109.

9 Dan Romanchik, "Getting Started With Boundary-Scan," Test & Measurement World, Cahners Publishing Company, 275 Washington Street, Newton, MA 02158-1630, March 1993, pp. 75-78.

10 Wayne T. Daniel, "Design Verification of a High Density Computer Using IEEE 1149.1," International Test Conference 1992 Proceedings, International Test Conference, 514 E. Pleasant Valley Blvd., Suite 3, Altoona, PA 16602, September 1992, pp. 84-90.

11 Bob Roth, "No 'Accounting' for BST," EDN Products & Careers Edition, Cahners Publishing Company, 275 Washington Street, Newton, MA 02158-1630, December 1992, p. 65.

12 Gerald Jacob, "Supporting the Boundless Growth of Boundary Scan," Evaluation Engineering, Nelson Publishing, 2504 N. Tamiami Trail, Nokomis, FL 34275, July 1994, pp. 58-62.

13 Jon Turino, "You Can Obtain Boundary Scan's Benefits Despite Use of Some Nonscan ICs," EDN Magazine, Cahners Publishing Company, 275 Washington Street, Newton, MA 02158-1630, November 12, 1992, pp. 171-174.

14 Robert Dougherty, "Applying IEEE 1149.1 Boundary Scan to the HAIDE System," Design & Test Expo 1993 Proceedings, Miller Freeman, 13760 Noel Road, Suite 500, Dallas, TX 75024, January 1993, pp. 313-320.

15 Hewlett-Packard, Application Note 1210-7, "Design for Testability Using Boundary-Scan 1149.1," Hewlett-Packard, 4 Choke Cherry Road, Rockville, MD 20850, 1991.

16 Teradyne, VICTORY-BR05850A-0492, "VICTORY Boundary-Scan Test Software," Teradyn, 321 Harrison Avenue, Boston MA 02118, 1992.

17 Harry Jin, "Using Boundary-Scan Tests to Find Structural Faults at the Board Level," Design & Test Expo 1993 Proceedings, Miller Freeman, 13760 Noel Road, Suite 500, Dallas, TX 75024, January 1993, pp. 321-327.

18 Bruce Peterson, Harry Jin, "Testing High Performance Personal Computer Modules Using Boundary Scan: A Case Study," NEPCON West '93 Proceedings of the Technical Program, Reed Exhibition Companies, PO Box 5060, Des Plaines, IL 60017-5060, February 1993, pp. 173-178.

19 Texas Instruments, Literature Number SATT115A, "ASSET Diagnostic System Product Family- Second Generation: Technical Overview and Applications," Texas Instruments, PO Box 655303, Dallas, TX, 75265, 1992.

20 Stan Runyon, "Design-for-Test Finally Comes A-Board," Electronic Engineering Times, CMP Publications, 600 Community Drive, Manhasset, NY 11030, January 11, 1993, pp. 39-46.

21 Gerald Jacob, "Let New Tools Add the Testability You Always Wanted," Evaluation Engineering, Nelson Publishing, 2504 N. Tamiami Trail, Nokomis, FL 34275, March 1994, pp. 56-59.

22 Dr. Bulent I. Dervisoglu, Mike Ricchetti, "Design for Testability...Addressing the Problems Before They Occur," 1992 High Speed Digital Symposium, Hewlett-Packard, 4 Choke Cherry Road, Rockville, MD 20850, 1992, pp. 9-1 to 9-21.

23 Colin M. Maunder, "Integrating Internal Scan Paths," The Test Access Port and Boundary'-Scan Architecture, IEEE Computer Society Press, 10662 Los Vaqueros Circle, PO Box 3014, Los Alamitos, CA 90720-1264, 1990.

24 J. Hirzer, "Testing Mixed Analog/Digital ICs," The Test Access Port and Boundary'-Scan Architecture, IEEE Computer Society Press, 10662 Los Vaqueros Circle, PO Box 3014, Los Alamitos, CA 90720-1264, 1990.

25 Stephen Yurash, "A Practical Design Methodology for Running an Internal Full-Scan Test From the JTAG Port," Design & Test Expo 1993 Proceedings, Miller Freeman, 13760 Noel Road, Suite 500, Dallas, TX 75024, January 1993, pp. 297-302.

26 Texas Instruments, SN54/74ABT8996 Addressable Scan Port data sheet, Testability Products Data Book, Texas Instruments, PO Box 655303, Dallas, TX, 75265, 1994.

Partitioning Designs With 1149.1 Scan Capabilities

Steve Altaffer
Texas Instruments Incorporated
Defense Systems Electronics Group

SCTA031
August 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Partitioning Designs with 1149.1 Scan Capabilities

by Steve Altaffer

Introduction

Typical 1149.1 Scan Architecture Descriptions

Star vs. Scan path system scan designs addressed in IEEE 1149.1 use either a single scan path, employing a common mode line and daisy-chained data (scan path), or separate mode lines to individually controlled independent rings and common TDI/TDO signals (star). Figure 1 depicts each configuration. Each can have advantages over the other depending on applications and design requirements.

The reduced path lengths of a star configuration simplify the scan controller design since each scan path is shorter than if the entire system were connected on a single scan path. Although the same amount of data may be necessary to control the entire system, the overhead of tracking unused elements in the scan path for a particular test is reduced. The star configuration is usually recommended for systems that require individualized control over independent functions or shorter scan-path lengths to simplify the scan controller design. The star configuration also has an inherent fault tolerance as an advantage. Because each of the rings in a star configuration is isolated from the system, a fault within the scan path itself does not corrupt the entire system scan path as would be the case in a scan-path configuration. A multi-board system employing a scan-path configuration has the ability to control all of the elements in a scan path regardless of the board on which they are located. A system that is backplane bus intensive or has functions spread across board boundaries would most likely employ a scan-path configuration to simplify board boundary and functional testing.

Scan-Path Linker (SPL) and Scan-Path Selector (SPS) Overview

Theory of Operation

The scan ring family of devices (SPS and SPL) provide the ability to create a hybrid star-scan-path architecture in a system while maintaining the advantages of both. The devices can be used to bypass an entire scan path on a board or select up to four independent rings (SPL) on the board. A single scan path can be selected and scanned or a combination of rings can be linked together in series, depending on the scan ring support device being used. Figure 2 depicts the SPS as it would be connected in a system.

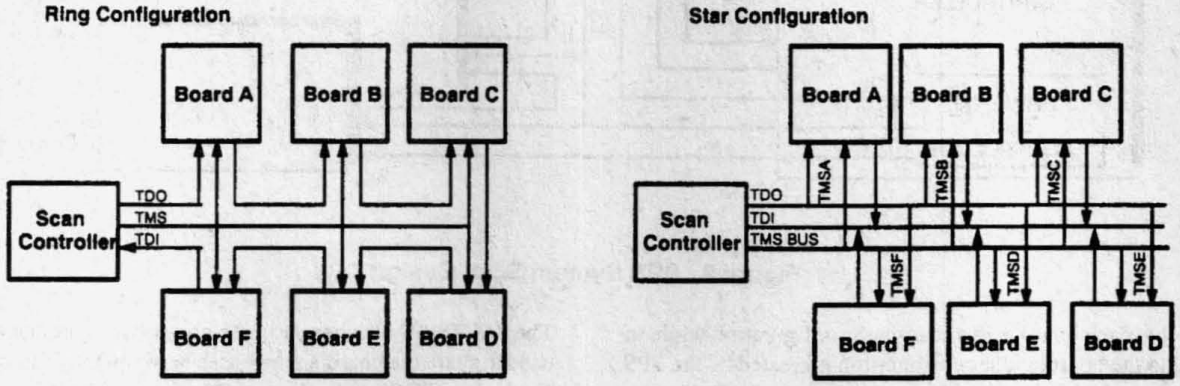


Figure 1. Ring and Star Configurations

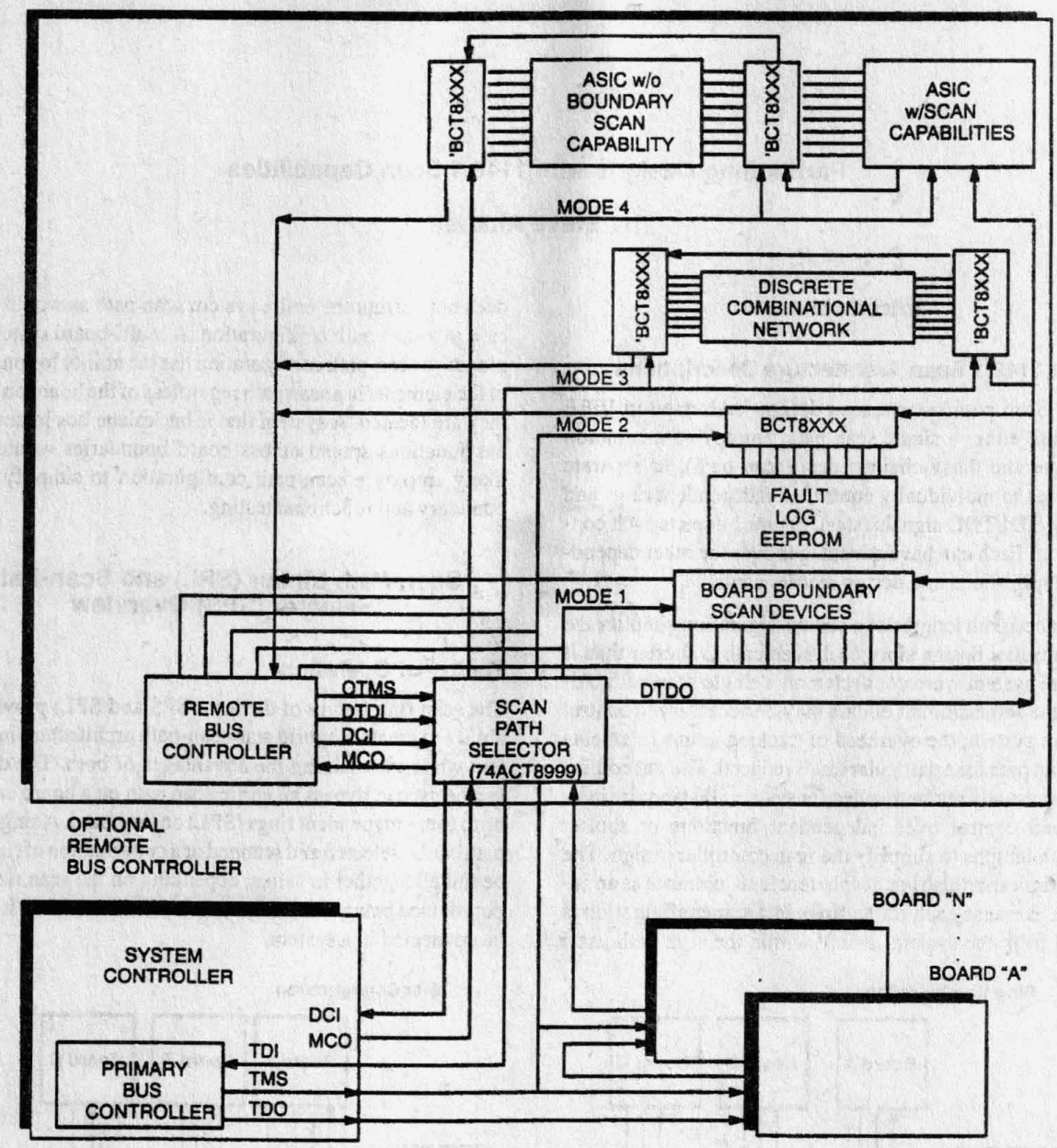


Figure 2. SPS System Scan Design

Note that each board is in a scan-path configuration while internal to the board, a star configuration is created by the SPS. A feature of the scan ring support devices is the ID bus that uniquely identifies a board to a system controller. The ID bus in the SPS (SN74ACT8999) also serves as a bidirectional data bus (BiD), capable of communicating with a remote bus controller or other on-board controller through the scan interface.

The 'ACT8999 also has a remote controller input that can be used to share the board's scan buses between the Primary Bus Controller (PBC) and a Remote Bus Controller (RBC) on the board. The remote input can select any of the four scan rings on a board while maintaining the primary path through the device to the rest of the system. In order to properly handshake with the board for remote-control handoff, ID bus operation,

or status/interrupt capabilities, a four-wire status bus is included in the devices. Those wires are labeled Master Condition Input (MCI), Master Condition Output (MCO), Device Condition Input (DCI) and Device Condition Output (DCO). The DCI pin also serves as the clock input to an 8-bit internal programmable counter. Properties such as the polarity of the clock, up/down counting, and latch-on-zero in the countdown mode are all programmable. The DCO pin can serve as the terminal count (MAX/MIN) output to allow cascading or interrupting the scan controller.

Select Register Operation

The SELECT data register is an 8-bit control register that determines the output of each of the DEVICE TEST MODE SELECT (DTMS) signals (2 bits per output). The select decoding for a single DTMS is shown in Table 1.

Table 1. Select Register Decoding

Select Bit MSB	LSB	DTMS Output
0	0	High (STRAP)
0	1	Low (IDLE)
1	0	OTMS *
1	1	TMS

* For devices without OTMS input, TMS is transferred to DTMS.

It is the same for each of the other DTMS outputs. For the case of a scan-path device not having an OTMS (remote) input, the device will route the primary TMS to the selected DTMS output. When an output or outputs are selected to convey TMS, the scan-path device waits until the primary TMS enters the IDLE state before multiplexing the TMS and TDI to the secondary scan path. This ensures proper state synchronization between the primary and board scan path(s) with respect to the TAP controllers on each. Any other means to "open" a secondary scan path would result in scan-path corruption and asynchroneity of data and control, and therefore is not allowed within the scan-path device hardware. This must be clearly understood by the software or firmware controlling the scan-path device so that the hardware is configured as the software believes it is. Referring to Figure 3, when a secondary scan path is opened, the TMS is driven directly to the output with internal delays only. Due to the routing of the data path directly from TDI to DTDO, it is necessary to sample the data on the rising edge of TCK and output to the secondary scan paths on the falling edge of TCK to comply with IEEE 1149.1 specifications. This creates an extra bit of data in the path whenever an external scan path is selected, but it is necessary to ensure data synchronization to the rings at high TCK frequencies. This sync bit will be present in all data and instruction scans and must be recognized by the scan bus controller whenever a secondary scan path is opened. The data from the scan path is then fed to the "normal" input of the scan-path device data or instruction registers and output to the primary scan path. For the SPL (SN74ACT8997), much the same data path is created.

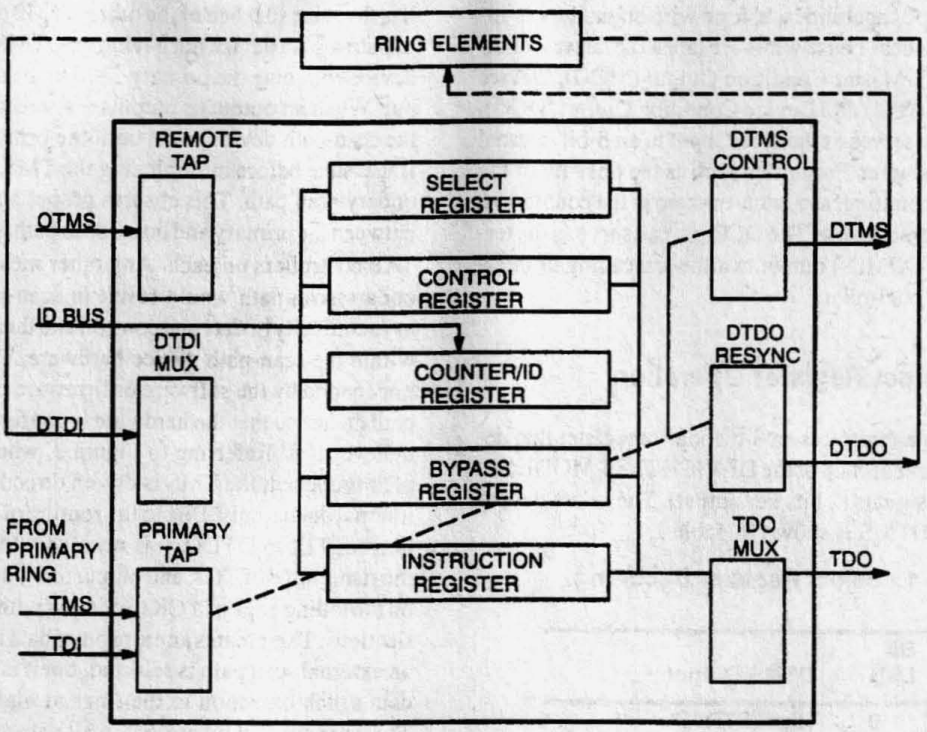


Figure 3. Scan-Path Selector (SPS) Scan-Path Ring with Ring Selected

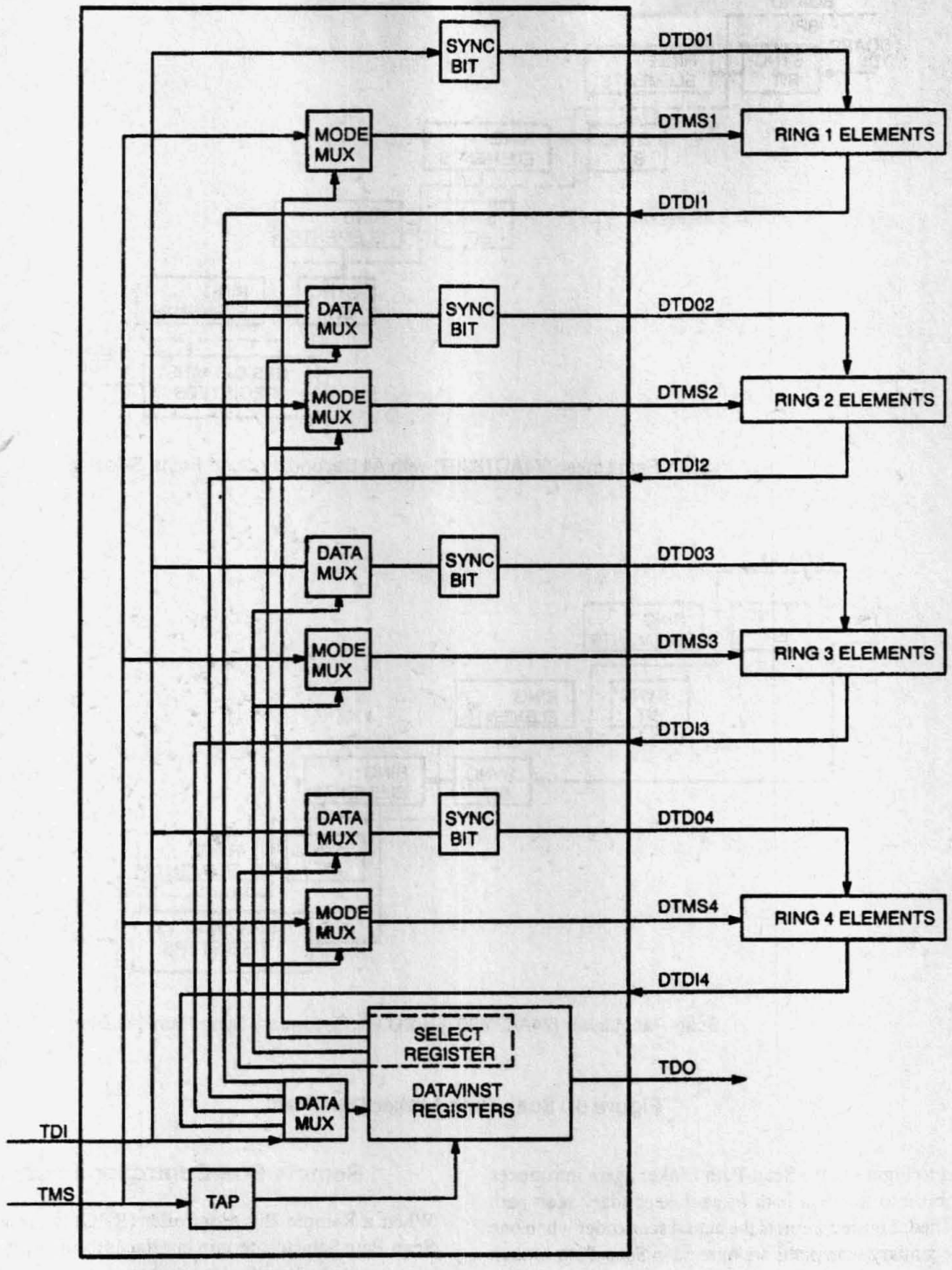
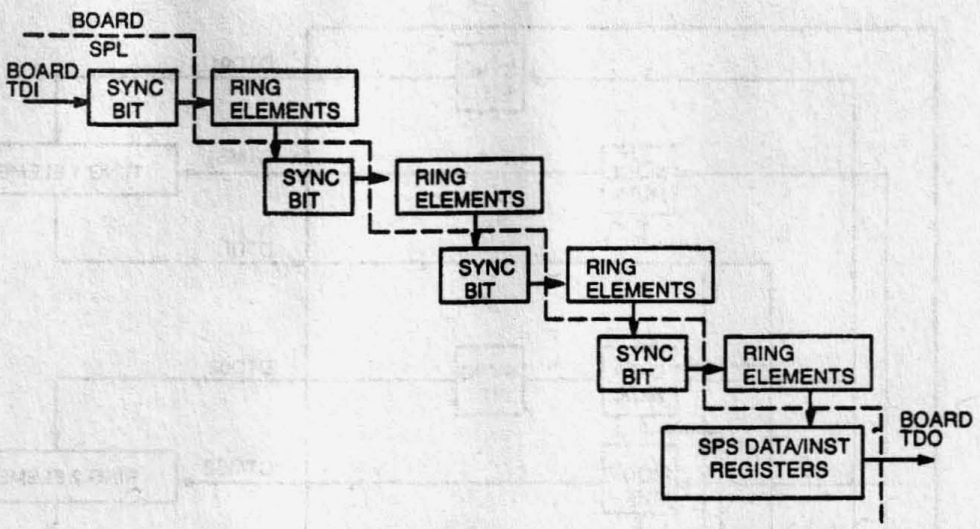
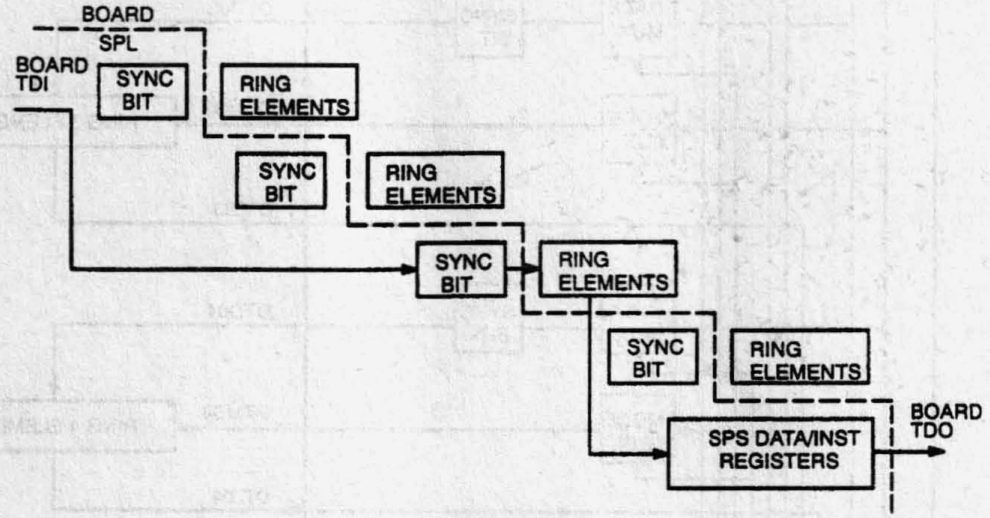


Figure 4. Scan-Path Linker (SN74ACT8997)



Scan-Path Linker (74ACT8997) with All Secondary Scan Paths Selected



Scan-Path Linker (74ACT8997) with One Secondary Scan Path Selected

Figure 5. Scan-Path Linker Data Path

Referring to Figure 4, the Scan-Path Linker again introduces an extra bit into the data path of each secondary scan path when opened. Figure 5 depicts the actual scan order when one or four secondary scan paths are opened in Scan-Path Linker.

Each of the sync bits are bypassed when a scan path is not selected and only the scan path or rings that are selected will introduce an extra bit into the path.

Remote Bus Controller Interfaces

When a Remote Bus Controller (RBC) is present with the Scan-Path Selector, certain interfaces to and from the SPS device need to be modified to ensure proper operation. The RBC inputs its TMS output to the OPTIONAL TMS (OTMS) pin of the SPS. When the SELECT register is loaded to output OTMS to the DTMS outputs, the CONTROL register must

also be loaded with the RBC Enable bit (RBCE) set TRUE to allow the RBC TMS direct control of the SELECT register. In this mode the Remote Test Access Port (RTAP) controls the shifting of data through the DTDI to the DTDO to the rings. When the RTAP is in control a dedicated instruction and bypass register become activated to emulate a true 1149.1 interface as seen by the RBC, as depicted in Figure 6.

The only valid instructions are 'scan the select register' or 'scan the bypass bit' during this mode of operation. The Primary Bus Controller (PBC) still has the ability to scan the other registers in the SPS that enables it to disable the RBC by setting the RBCE bit to FALSE should it become necessary. When connecting an RBC to the SPS the normal interfacing must be altered as shown in Figure 7.

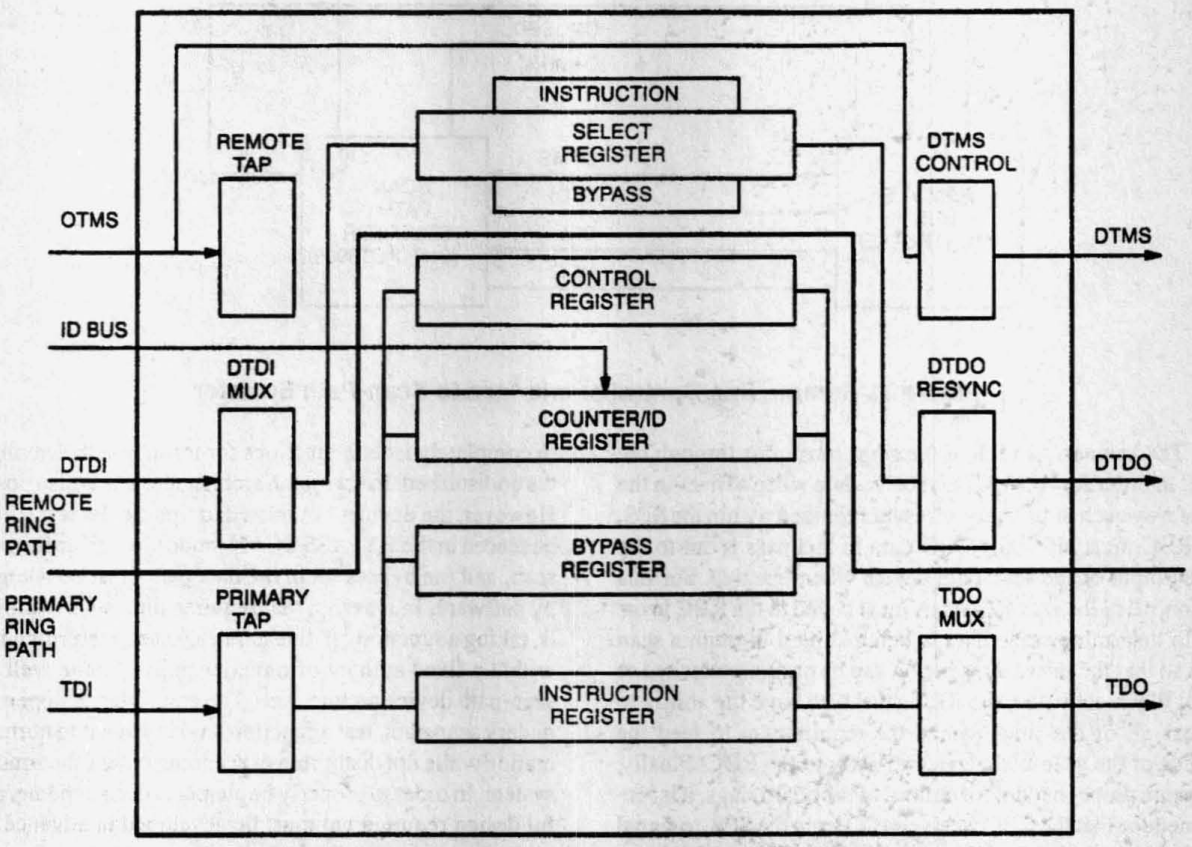


Figure 6. Scan-Path Selector (SN74ACT8999) with Optional (Remote) TMS Selected

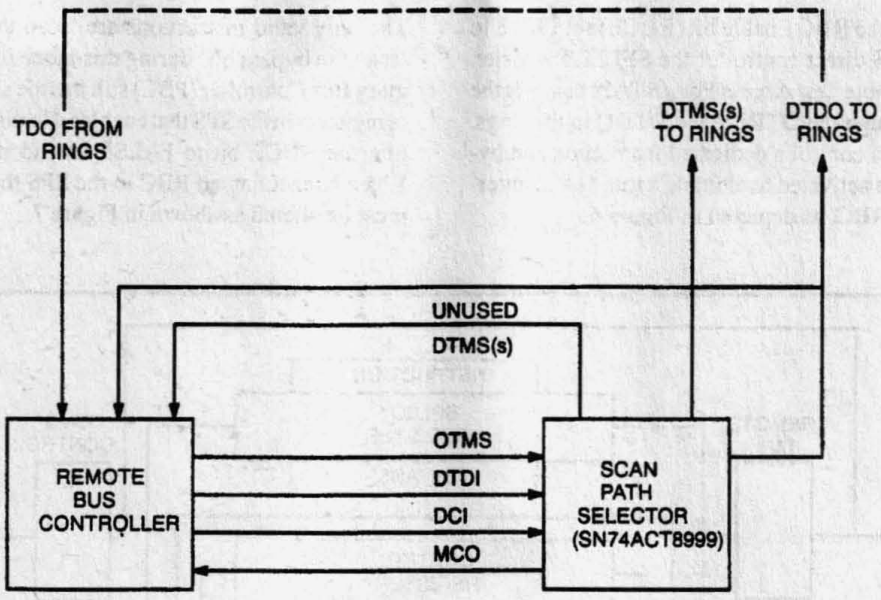


Figure 7. Remote Bus Controller Interface to Scan-Path Selector

The TDO signals of each of the rings must pass through the RBC in order for the RBC to receive data when active. In the same way each of the rings is resynchronized within the SPS, the RBC must clock the TDO data in and pass it out to the DTDI input of the scan-path device when inactive. For this reason, all of the DTMS signals must be fed to the RBC in order to determine when data is being shifted through a scan path so that the internal resync bit can be properly clocked or held. When activated, the RBC must also have the ability to bypass all of the rings, hence the requirement to feed the DTDO of the scan-path device directly to the RBC. Finally, to ensure proper handoff of control of the board rings, it is recommended that the RBC receive MCO from the SPS, to signal a grant from the PBC, and send DCI to the SPS, to indicate to the PBC that the RBC is currently using the board rings. This is also the handshake mechanism between the PBC and RBC for BiD bus transfers.

Partitioning 1149.1 Designs Using the Scan-Path Support Devices

System Level Partitioning and Considerations

Design Requirements

The ability to create a hybrid star/scan-path architecture using a scan-path device has many advantages over a single scan-path design. Scan designs can be partitioned in such a way as to completely isolate functions for testing while leaving others undisturbed. In scan-path architecture this is also possible. However, the devices not related to a particular test still must be placed in the BYPASS SCAN mode through an instruction scan, and the bypass bit in the data path must be recognized by software. In a design that requires time slice testing, that is, taking a function off-line to run a test and returning it back within a fixed amount of time, lends itself quite well to the scan-path device architecture. The controller can open a secondary scan path, test a function, and replace it to normal operation while not disturbing or scanning other functions in the system. In order to properly implement such a scheme, a careful design requirement must be developed in advance to account for any possible unexpected operations when exercising a function. For instance, an ASIC self test may inadvertently toggle its device outputs that in turn ripple to another function not under test. The inputs of the ASIC under test must be isolated so that the circuits feeding it do not effect the self-test. Avoiding inadvertent operation is probably the most common consideration but there are many others when implementing a time slice test scheme. Only through proper system definition and specification can all of the pitfalls be avoided. Another advantage of using a scan-path device is the ability to have a remote bus controller resident on the board to relieve the test burden of the primary bus controller. This creates a distributed test structure in which the PBC can command tests to be run autonomously on multiple boards and report status back. The relief realized at the system level is, of course, not

without cost. The development of board controller software will still be necessary as well as the handshaking and reporting structure between master and remote. This structure has a payoff throughout a product life cycle by exploiting tests during board and system integration, board production and depot testing as well as common module insertion. It can also reduce system test times by having all tests within a system running tests concurrently and reporting status instead of a single primary system executing tests in series.

Partitioning of Scan Paths

The proper partitioning of rings is the single most important factor in successfully reaping the benefits of scan-path device insertion into a scan design. Normally a board is functionally partitioned within a system by design. Within a board, functions also need to be partitioned for scan testing by placing test-related scan elements adjacent in the scan path. When using a scan-path device this is a requirement to enable efficient use of the device. If a test requires scanning of devices on separate rings of a scan-path device on a board, the controller must scan the devices to stimulate a test, scan the scan-path device SELECT register to place the stimulus secondary scan path in IDLE in order to hold the data, and open the response scan path, and then scan the results from the response scan path. This procedure becomes even more complex should the stimulus and response elements be mixed on separate rings. Should the test involve a dynamic stimulus and response, that is not static patterns, repeatability may not be possible. This fact arises due to the need to leave either the stimulus or response elements in IDLE (which implies running) while the other is being initialized. The time between scanning the first scan-path elements and the second could be variable or cause unknown data to be generated or sampled. Careful timing analyses can be performed to eliminate the problem but such an architecture is not recommended. Instead, the linkable scan-path device, SPL, should be used if scan elements for tests MUST reside on different rings for multiple uses, i.e., an element in RING1 is used for stimulus in a test with RING2, and response with elements on RING3. In most cases this is avoidable or optimization is possible to minimize the number of "inter-scan path" tests through proper partitioning.

How Much Scan

Another consideration for system-level designs is how much partitioning should be performed. Each scan-path device has four rings that can be used in a design, but not all of them have to be used. If the design does not lend itself to creating four separate rings, two or three can be used. This can create an open scan-path condition when an unused scan path is inadvertently selected. Great care must be taken during software development and design to avoid this possibility from occurring through constraint checking. If SPL is used, the DTDO and DTDI of unused rings can and should be tied together to at least create a path for data. Software must still detect the lack of any device(s) on the scan path that was opened, based upon instruction scan error checking or through examination of the scan-path device's SELECT register. This problem compounds itself when multiple scan-path devices exist within a system that have unused DTMS signals. Under such conditions the scan controller software will have to find the SELECT register contents of each scan-path device in the scan path to detect the error, determine the true state of the scan path, and correct the problem. The controller software becomes an issue in determining whether to use the scan-path device in a design. The obvious solution is to use all of the scan rings available on the scan-path device. Switching between multiple secondary scan paths for a test again becomes a problem and the SPL is recommended. If a remote controller is being used, all of the DTMS signals and the DTDO must be fed to it and can be used to detect the error condition, maintain the data-path integrity, and signal the PBC through the DCI-> DCO status signals of the condition.

Board Boundary Testing

When implementing scan-path devices into designs that contain board boundary scan elements to test backplanes or motherboards, two options exist for placing the boundary elements as depicted in Figure 8.

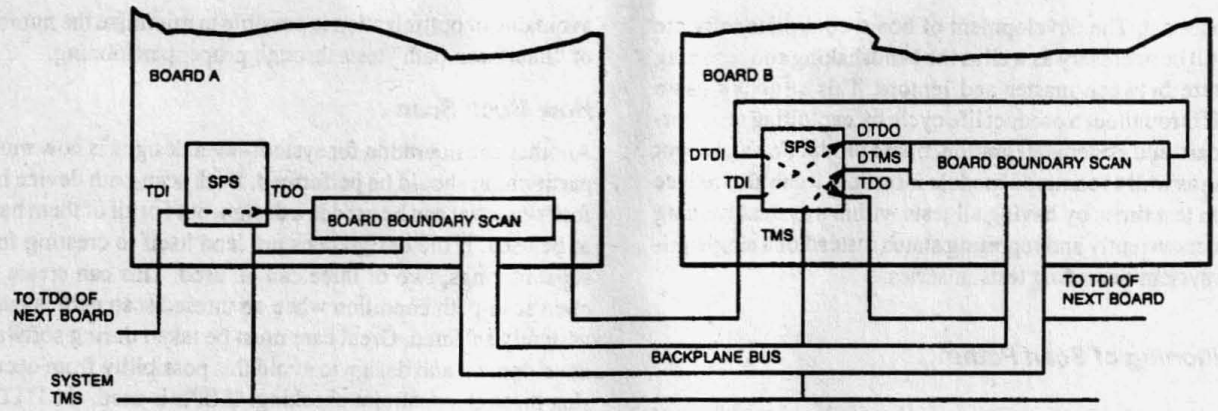


Figure 8. Board Boundary Element Scan-Path Options

Board A has the boundary elements placed on the primary scan path of the system. This would allow for two scenarios. First, if an RBC was also present on the board, the PBC could perform board boundary tests while the RBC performed board tests. Secondly, this implementation also allows selecting a scan path on the board and scanning the boundary elements to perform multiple tests concurrently. The disadvantage of this scheme is that the board is no longer isolated from the system by a single interface and some of the fault tolerance of the scan-path device architecture is lost. Board B places the boundary elements on a scan path of the scan-path device. This option retains all of the advantages of the scan-path device fault tolerance with the trade-off being the inability to run RBC concurrent tests if one is present in the design. In both cases board-to-board testing is still possible using the system scan-path architecture and the ability to open a scan path on each board.

Partitioning a Board Design – An Example

Memory Board Description

The example given is a simple memory board. It consists of a bus interface controller that could be an ASIC or discrete circuitry. The bus controller decodes address and control activity on the backplane and creates the necessary address and control signals required locally for memory and I/O cycles. The board also includes further decoding to create specific device selects for the memory and I/O arrays and any further control signal generation not performed within the bus controller. Finally, the board contains a memory array and I/O register array. The memory array could contain both static- and PROM-type devices.

Partitioning for Test

The buffers for the board are chosen from the 'BCT8XXX family of 1149.1-compatible octal devices ('BCT8244,8245,8373,8374). Referring to Figure 9, the placement of these devices partition the board into its three functions; bus controller, decode circuitry, and the memory and I/O space.

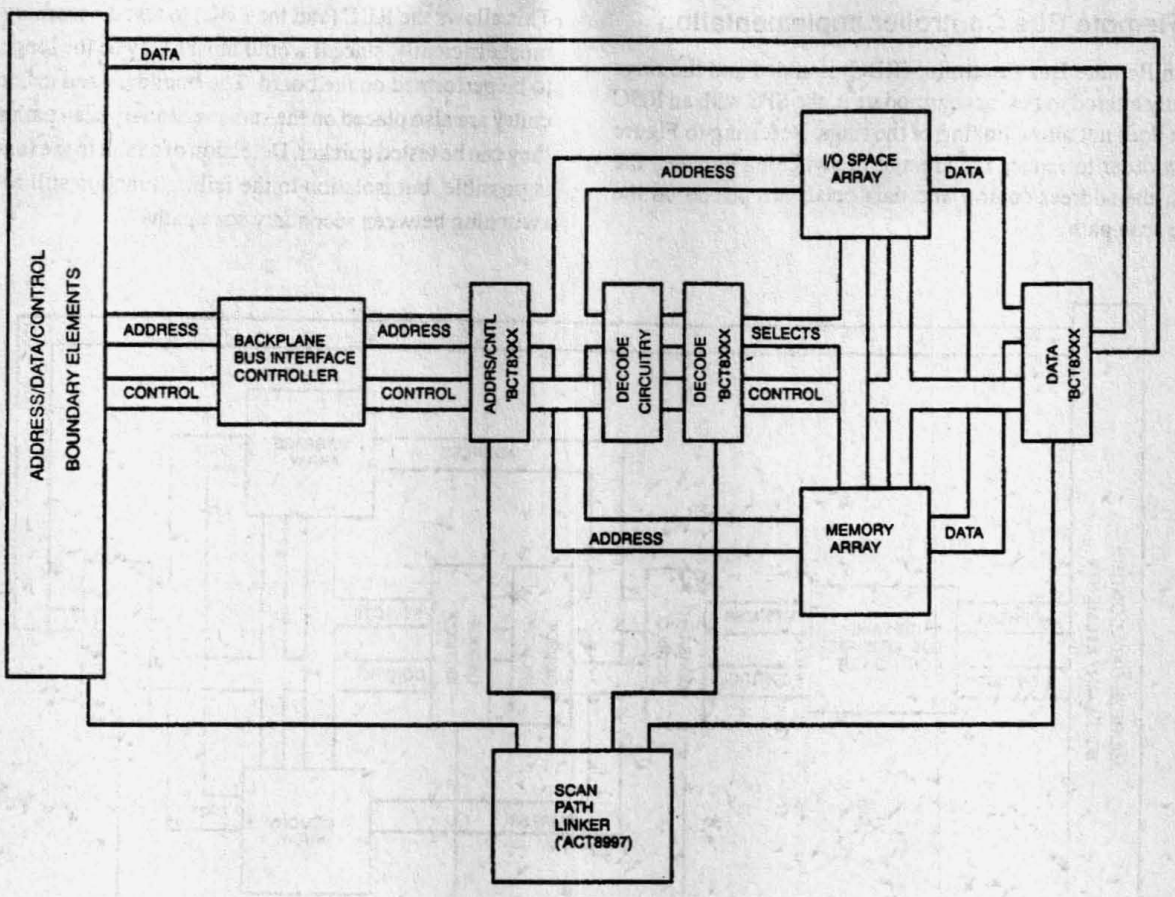


Figure 9. Memory Board Partition Example Using Scan-Path Linker

In addition, the backplane has been isolated by inserting the 1149.1-compatible octals for testing the interface to and from other boards using the test controller. These elements are on a scan path by themselves so that they can be scanned to perform the aforementioned tests without scanning the rest of the board. Next, 1149.1-compatible octals are placed between the bus controller and decode circuitry and between the decode circuitry and memory-I/O space arrays, each on its own scan path. Since tests of each of the functions relies on two of the scan-path device rings, the SPL is chosen. Thus, to test the memory array the control selects the address/control buffers and data buffers to be opened and links through the SPL; the boundary elements and address/control to test the bus interface controller; and so on. The address/control and decode octals could have been placed on the same scan path, but this would only serve to complicate the tests.

Remote Bus Controller Implementation

When Remote Bus Controller (RBC) is added and the rings slightly altered to best accommodate it, the SPS with an RBC input does not allow linking of the rings. Referring to Figure 10, in order to reduce the amount of switching between the rings, the address/control and data octals are placed on the same scan path .

This allows the RBC (and the PBC) to test the memory array most efficiently, since it would most likely be the longest test to be performed on the board. The boundary and decode circuitry are also placed on the same secondary scan path so that they can be tested quicker. Detection of a fault in the functions is possible, but isolation to the failing function still requires switching between secondary scan paths.

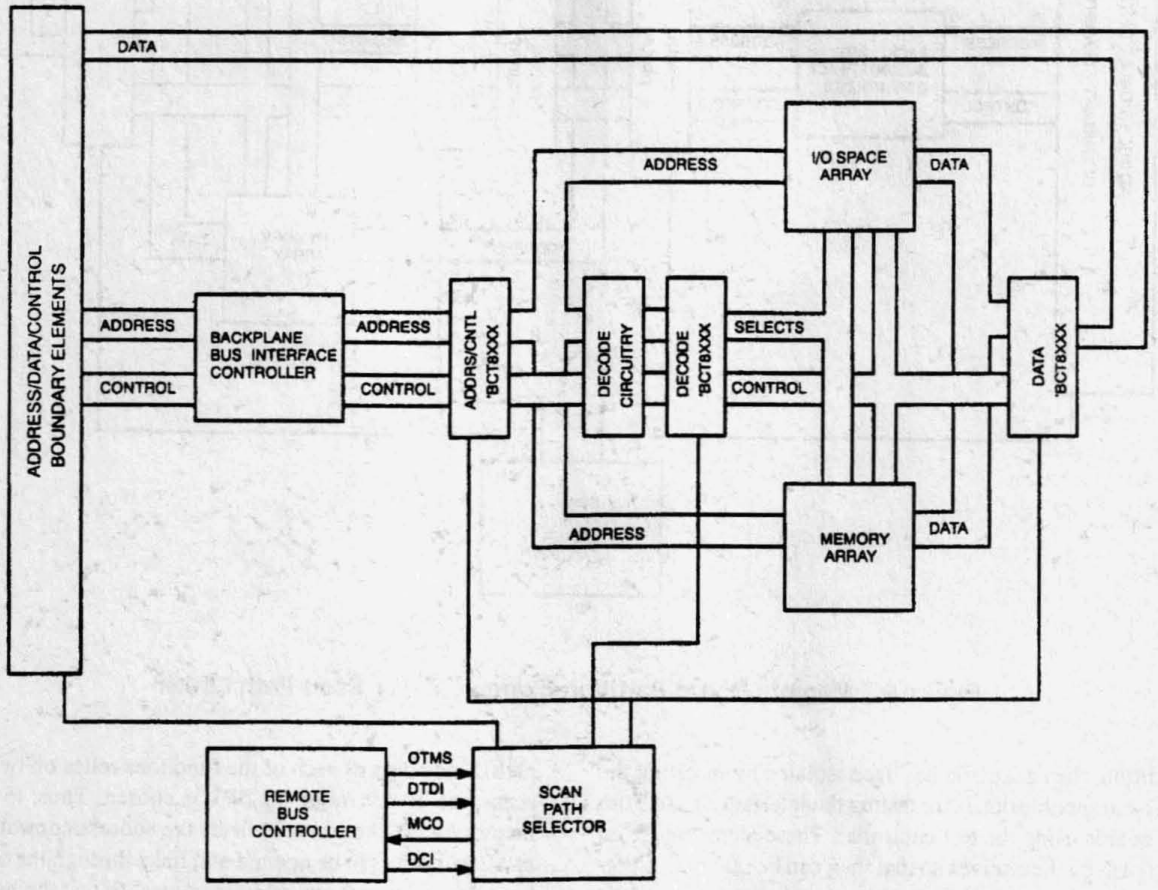


Figure 10. Memory Board Partition Example Using Scan-Path Selector

A Proposed Method of Accessing 1149.1 in a Backplane Environment

Lee Whetsel
Senior Member Technical Staff
Semiconductor Group

SCTA032
Reprinted with permission from Proceedings of International Test Conference,
Baltimore, Maryland, September 20–24, 1992.
© 1992 IEEE

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1992, Texas Instruments Incorporated

A Proposed Method of Accessing 1149.1 in a Backplane Environment

Lee Whetsel
Texas Instruments Inc.
P.O. box 869305, M/S 8407
Plano, Texas 75086

Abstract

This paper presents a novel circuit and protocol that can be used in system backplanes to provide a connection method between backplane and board level IEEE 1149.1 serial buses. While the basic objective of this approach is to provide a simple 1149.1 backplane to board connection method, it can be expanded to include other features, some of which are similar to those being developed in the IEEE P1149.5 and P1394 backplane serial bus standards.

1.0 Introduction

The concept of a simple, cost-effective serial bus protocol providing linkage between 1149.1 board and backplane environments has been developed. This serial bus protocol operates on the backplane, using the signal wires defined in 1149.1, to address and select one of the boards in a backplane. Once selected, the board can be communicated to using the standard 1149.1 bus protocol. In general, the technique described in this paper can be applied to any type of bus. However, in this paper it is described as a feature added to the IEEE/ANSI 1149.1 standard serial bus designed for boundary scan testing of ICs at the board level [1]. The author assumes the reader has a basic understanding of the 1149.1 standard.

The approach described in this paper is based on a unique protocol. This protocol can be embedded in existing serial bus protocols and invoked, during times when the buses are in an idle or non-operational state, to address and select a slave device for access by a serial bus master. After the protocol has been used to connect a serial bus slave up to a serial bus master, it relinquishes control of the bus, and allows the bus to revert back to its normal mode of operation. One of the advantages of this approach is that it does not require modifying the protocol of the serial bus it is used with. Therefore, upgrading a preferred or existing serial bus to include the connection method provided by the protocol can be less costly and time consuming than a complete redesign approach.

The term "serial bus slave" used in this paper represents any logic module capable of being interfaced to and controlled by a serial bus master. While this papers describes serial bus slaves as being boards in a backplane, they could also be: sub-circuits in an IC, ICs on a multi-chip module, ICs on a board, backplanes in a subsystem, or subsystems in a system. The term "serial bus master" used in this paper represents any logic module capable of interfacing to and controlling a serial bus slave. While this paper will illustrate the serial bus master as existing on the backplane wiring, it actually exists either in a backplane board or as an external tester connected to the backplane.

2.0 Background

As the use of 1149.1 continues to grow, more interest is being focused on how to access 1149.1 board designs in a backplane environment. Several methods of accessing 1149.1 boards in a backplane environment have been proposed. The following is a brief description of each of these methods.

2.1 Using 1149.1 at the Backplane Level

The 1149.1 standard describes a 4-wire serial bus that can be used to transmit serial data between a serial bus master and slave device. The 1149.1 bus consists of a test mode select (TMS) signal, a test clock (TCK) signal, a test data output (TDO) signal, and a test data input (TDI) signal. The TMS and TCK signals are output from the master and input to the slave. The TDO output from the master is input to the TDI input of the slave, and the TDO output from the slave is input to the TDI input of the master. During serial access, the master outputs control on TMS and clock on TCK to allow serial data to be transferred between the master and slave, via the TDO and TDI bus connections.

While 1149.1 was developed to serially access ICs on a board, it can be used at the backplane level to serially access boards. 1149.1 has two serial access configurations, referred to as "ring" and "star", that can be used at the backplane level. The following describes both configurations and identifies problems with each when used at the backplane level.

2.1.1 1149.1 Backplane Ring Configuration

In a backplane 1149.1 ring configuration, all boards directly receive the TCK and TMS control outputs from a primary serial bus master (PSBM) and are daisy chained between the PSBM's TDO output and TDI input. During scan operation, the PSBM outputs control on TMS and TCK to scan data through all boards in the backplane, via its TDO and TDI bus connections. The problem associated with the ring configuration, is that the scan operation only works if all the boards are included in the backplane and are operable to scan data from their TDI input to TDO output. If one of the boards is removed or has a fault, the PSBM will be unable to

Copyright IEEE, Reprinted, with permission, from Proceedings of International Test Conference, Baltimore, Maryland, September 20-24, 1992.

scan data through the backplane. Since the ring configuration does not allow access to remaining boards when one is removed or disabled, it does not fully meet the needs of a backplane serial bus.

2.1.2 1149.1 Backplane Star Configuration

In a backplane 1149.1 star configuration, all boards directly receive the TCK and TDI signals from the PSBM and output a TDO signal to the PSBM. Also each board receives a unique TMS signal from the PSBM. In the star configuration only one board is enabled at a time to be serially accessed by the PSBM. When a board is enabled, the TMS signal associated with that board will be active while all other TMS signals are inactive. The problem with the star configuration is that each board requires its own TMS signal. In a backplane with 50 boards, the PSBM would have to have 50 individually controllable TMS signals, and the backplane would have to have traces for each of the 50 TMS signals. Due to these requirements, star configurations are typically not considered for backplane applications.

2.2 Interfacing 1149.1 to other IEEE Buses

Two IEEE serial bus standards, P1149.5 and P1394, are in development for use in system backplanes. Since these standards are being specifically designed for backplane applications, they overcome the problems stated using 1149.1 as a backplane bus. However, the protocols of these anticipated standards are different from the 1149.1 protocol and therefore methods must be defined to translate between them and 1149.1. The following sections describe each backplane bus and identify problems with each when used to interface into 1149.1 board environments.

2.2.1 Interfacing P1149.5 to 1149.1

The P1149.5 standard working group is defining a module test and maintenance bus that can be used in system backplane environments [2,3]. P1149.5 is a single master/multiple slave bus defined by a 5-wire interface. Two of the wires are used for transferring serial data between the bus master and slave devices, one wire is used as a clock, one wire is used to control the operation of the bus, and one wire is used as a pause request from a slave to the master. The P1149.5 bus master initiates a data transfer operation by transmitting a data packet to all slave devices. The data packet consists of an address and command section. The slave device with a matching address is enabled to respond to the command section of the data packet as described in the P1149.5 standard proposal.

While the P1149.5 is a good data transfer type backplane bus for high-end commercial and military systems, its capabilities may exceed the requirements of some middle and low-end commercial systems that don't require or support its command set. Interfacing P1149.5 into an 1149.1 environment can be done but the system hardware and software designers must have an understanding of both bus types. One of the problems, therefore, in using P1149.5 to only interface into an 1149.1 environment, is that it adds an unnecessary complication to an otherwise simple serial access approach. Another problem is that the bandwidth of the 1149.1 serial data transfer may be adversely affected by the P1149.5 to 1149.1 protocol conversion process.

2.2.2 Interfacing P1394 to 1149.1

The P1394 standard working group is defining a 2-wire high-speed serial bus that can be used in either a cable or system backplane environment [4]. The P1394 standard, unlike P1149.5, is not a single master/multiple slave type bus. In P1394, all devices (nodes) connected to the bus are considered to be of equal mastership. Control of the bus is achieved by one node winning an arbitration contest with the other nodes in the network. Once a node wins control of the bus, it can transfer data to or from any other node in the network. The fact that P1394 can operate on a 2-wire interface makes this bus attractive in newer 32-bit backplane standards where only two wires are reserved for serial communication [5,6,7,8]. However, there are problems in using P1394 as a backplane test bus to access 1149.1 board environments.

The first problem is that P1394 is significantly more complex in operation than 1149.1, thus devices designed to translate between P1394 and 1149.1 may be costly. The second problem is that P1394 is not a full time test bus, but rather it is a general purpose serial communication bus. Its primary purpose in a backplane environment is to act as a backup interface in the event the parallel interface between boards becomes disabled. While 1149.1 test access can be achieved via P1394, it will be available only during time slices when the bus is not handling functional operations. Thus on-line 1149.1 test access will be limited and must be coordinated with other transactions occurring on the P1394 bus.

2.3 Extending 1149.1 for Backplane Usage

Another method of achieving a backplane to board level interface is to extend the protocol defined in the 1149.1 standard. Such an approach has been described in a paper presented at the 1991 International Test Conference by D. Bhavsar [9]. While the approach described in the paper has the same basic goal in mind as the one presented in this paper, they are fundamentally different in the method used to achieve the goal.

The Bhavsar paper describes a method of extending the protocol of 1149.1 to where it can be used to access an interface circuit residing between the backplane and board level 1149.1 buses. The interface circuit responds to 1149.1 protocol transmitted over the backplane bus to load an

address. If the address matches the address of the interface circuit, the interface circuit is connected to the backplane. After the interface circuit is connected to the backplane, additional 1149.1 protocol is input to the interface circuit to connect the backplane and board level 1149.1 buses. Following this connection procedure, the board level 1149.1 bus can be controlled by the backplane 1149.1 bus. While Bhavsar's approach is an interesting one, it has one problem that limits its effectiveness as a general purpose 1149.1 backplane to board interfacing method.

The problem is that the approach does not allow for selecting one board, then selecting another board without first resetting the backplane and board level 1149.1 buses, by transitioning them into their test logic reset (TLRST) state. Entering the TLRST state causes test conditions setup in the ICs of a previously selected board to be lost due to the test reset action of the 1149.1 bus on the test access ports (TAPs) of the ICs.

For example, if the interconnects between two boards are to be tested, it is necessary to select and setup one of the boards to output a test pattern, then select the other board to receive the test pattern. With the described approach, the only way to select the second board, after the first board has been selected and setup, is to place the backplane serial bus in its TLRST state. The action of placing the backplane 1149.1 bus in it TLRST state clears out the test pattern setup in the first selected board, so the second selected board cannot receive the intended test pattern.

In another example, it may be desirable to select and initiate self-tests in a selected group of backplane boards. However, since the approach requires resetting the 1149.1 bus each time a new board is selected, it is impossible to self-test more than one board at a time, because resetting the bus aborts any previously initiated self-test.

3.0 A New Backplane Access Approach

The backplane access approach described in this paper provides a method of using the 1149.1 bus at the backplane level without incurring the problems previously described. Using this approach, it is envisioned that one homogeneous serial bus may be used throughout a system design, rather than translating between multiple serial bus types. Employing a common serial bus in system designs can simplify software and hardware engineering efforts, since only an understanding of one bus type is required.

A circuit, called an addressable shadow port (ASP), and a protocol, called a shadow protocol, have been defined to provide a simple method of directly connecting 1149.1 backplane and board buses together. When the 1149.1 backplane bus is in either its run test/idle (RT/IDLE) or TLRST state, the ASP can be enabled, via the shadow protocol, to connect a target board's 1149.1 bus up to the backplane 1149.1 bus. After the shadow protocol has been used to connect the target board and backplane buses together, it is disabled and becomes transparent to the operation of the 1149.1 bus protocol.

A board example using the ASP is shown in Figure 1. The board consists of multiple ICs and an ASP. The ICs operate, when connected to the 1149.1 backplane bus, via the ASP, as described in the 1149.1 standard. The ASP has a primary port for connection to the backplane 1149.1 bus, a secondary port for connection to the board 1149.1 bus, and an address input. The primary port signals are labeled; PTDI, PTDO, PTCK, and PTMS. The secondary port signals are labeled; STDI, STDO, STCK, and STMS. The address input to the ASP is a binary value used to identify the board on which the ASP mounted.

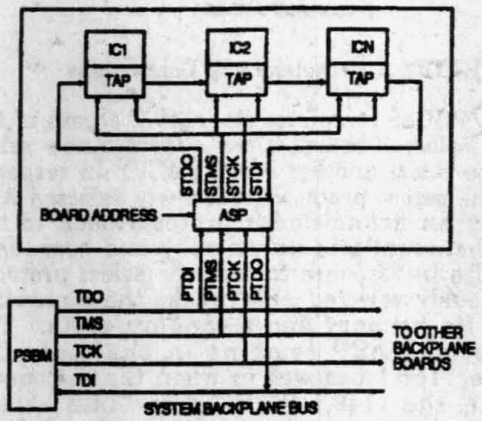


FIGURE 1 Board Using ASP Circuit

In Figure 2, multiple boards, similar the one in Figure 1, are shown interfaced to a PSBM via ASPs. When one of the boards needs to be accessed, the PSBM transmits a selection shadow protocol, called a select protocol, to address and enable the ASP of the selected board. The PSBM transmits the select protocol while the backplane 1149.1 bus is in either the RT/IDLE or TLRST state. The select protocol contains an address that is used to match against the address input to the ASP. All ASPs receive the select protocol, but only the one with the matching address is selected.

In response to the select protocol, the selected ASP transmits an acknowledgement shadow protocol, called an acknowledge protocol, to the PSBM to verify reception of the select protocol. The acknowledge protocol contains the address of the selected ASP to allow the PSBM to verify the correct ASP was selected. After transmitting the acknowledge protocol, the selected ASP makes a connection between its primary and secondary ports.

In response to the acknowledge protocol, the PSBM communicates to the selected board using the 1149.1 bus protocol. If the PSBM does not receive an acknowledge protocol, it assumes the board has been removed or is disabled and will not attempt to communicate to it using the 1149.1 protocol.

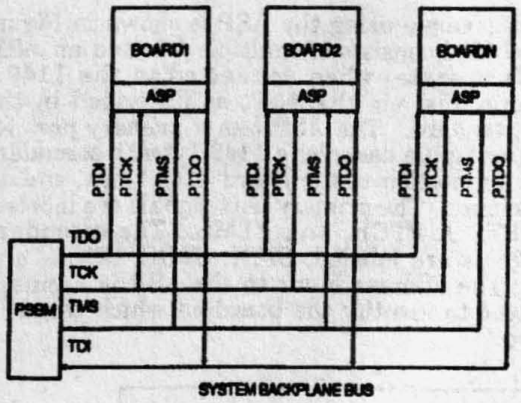


FIGURE 2 Backplane ASP Connections

After the PSBM completes its 1149.1 access of the currently selected board, it can output a new select protocol to select another board's ASP. In response to the new select protocol, the newly selected ASP transmits an acknowledge protocol back to the PSBM, then connects its primary and secondary ports. Also in response to the new select protocol, the previously selected ASP breaks the connection between its primary and secondary ports. The disconnecting ASP remains in the state the backplane 1149.1 bus was in when the disconnect occurs, i.e. the 1149.1 RT/IDLE or TLRST state. The ability to disconnect and leave a board level 1149.1 bus in the RT/IDLE state is very important since it allows leaving a board in a test mode while other boards are being selected and accessed.

A key objective in developing this backplane access approach was designing the select and acknowledge protocols so that they could be transmitted, via the 4-wire 1149.1 bus, without infringing upon the 1149.1 bus protocol. This objective was met by specifying that the select and acknowledge protocols could not use the 1149.1 TMS signal, and that the protocols could only be transmitted while the 1149.1 bus is idle in its RT/IDLE state or reset in its TLRST state.

In the RT/IDLE and TLRST states, TDO and TDI are disabled and pulled high (via pull-ups on TDI), TCK free runs, and TMS is held at either a logic zero or one state. While the 1149.1 bus is in one of these two states, the PSBM can output the select protocol from the PSBM's TDO output to the PTDI inputs of the ASPs, and receive the acknowledge protocol from the selected ASP's PTDO output on the PSBM's TDI input. Since the 1149.1 bus is inactive, the transmission of the select and acknowledge protocols is transparent to the 1149.1 bus, and does not infringe upon its protocol.

3.1 Design of Select/Acknowledge Protocols

To transmit the select and acknowledge protocols without using the TMS control signal, a bit-pair signaling method was designed to allow control and data to be transmitted together on a single wiring channel. During select protocols, the bit-pair signaling method allows the PSBM to transmit control and data from its TDO output to the ASP's PTDI input. During acknowledge protocols, the bit-pair signaling method allows the selected ASP to transmit control and data from its PTDO output to the PSBM's TDI input. Both protocols include control to indicate: an idle condition, a start data transfer condition, and a stop data transfer condition. In addition, both protocols include a method of transmitting data during the interval between the start and stop data transfer conditions.

The bit-pair signals are output from the transmitting device (PSBM or ASP) on the falling edge of the TCK and input to the receiving device (PSBM or ASP) on the rising edge of the TCK. Since this timing is consistent with 1149.1 timing, upgrading a PSBM to support this approach is simply a matter of forcing the TMS output to hold its present state ("0" for RT/IDLE and "1" for TLRST) while using normal 1149.1 scan operations to transmit and receive the select and acknowledge protocols. The simplicity of this approach makes it an attractive addition to the 1149.1 test bus. The bit-pair signals used in the select and acknowledge protocols are defined in the following list.

Idle Bit-Pair – an encoded control signal (I) identified by the transfer of two successive logic one bits from a transmitter to a receiver.

Select Bit-Pair – an encoded control signal (S) identified by the transfer of two successive logic zero bits from a transmitter to a receiver.

Logic 1 Bit-Pair – an encoded logic one signal (D) identified by the transfer of a logic zero bit followed by a logic one bit from a transmitter to a receiver.

Logic 0 Bit-Pair – an encoded logic zero signal (D) identified by the transfer of a logic one bit followed by a logic zero bit from a transmitter to a receiver.

3.2 Framing of Select/Acknowledge Protocols

A diagram of the select and acknowledge protocols being transmitted while the 1149.1 bus is in its RT/IDLE state is shown in Figure 3. The T signals shown in the protocol sequence indicate when the TDO to PTDI and PTDO to TDI wiring channels are tristate and pulled high. The first sequence framed between the first and second I signals is the select protocol output from the PSBM to the ASP (TDO to PTDI). The second sequence framed between the first and second I signals is the acknowledge protocol output from the selected ASP to the PSBM

(PTDO to TDI). The select protocol always precedes the acknowledge protocol as shown in the diagram.

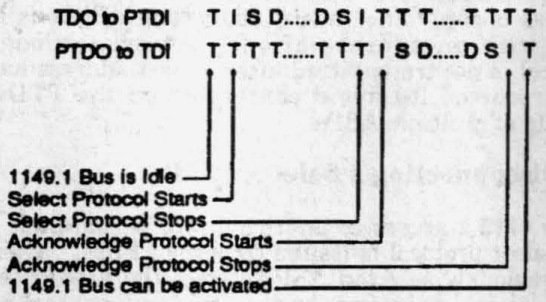


FIGURE 3 Select and Acknowledge Protocols

The I signal at the beginning of each protocol is designed to be indistinguishable from the preceding T signals. This avoids unintentional entry into a select or acknowledge protocol when the 1149.1 bus enters the RT/IDLE state after a scan operation. However, the I signal at the end of each protocol is designed to be distinguishable from the preceding S and D signals so that it can be used to terminate the protocol. Inside each protocol, first and second S signals are used to frame the address which is defined by a series of D signals. The logic zero and one D signals are distinguishable so that the binary address can be recovered.

3.3 ASP Circuit Description

A circuit example of the ASP is shown in Figure 4. The ASP consists of a receiver circuit (RCR), a transmitter circuit (XMT), a slave control circuit, multiplexers (MX1 and MX2), a power up reset circuit (PRST), and a reset address (RSTA). The primary port signals (PTDI, PTMS, PTCK, PTDO) connect to the backplane level 1149.1 bus. The secondary port signals (STDO, STMS, STCK, STDI) connect to the board level 1149.1 bus. The address input bus receives the board address.

3.3.1 ASP Receiver Circuit

The receiver circuit consists of a controller and a serial input/parallel output (SIPO) register. The PTDI signal from the PSBM is input to the receiver's SIPO register to supply the serial address during select protocols, and input to the receiver's controller to regulate the receiver during select protocols. The parallel address output from the SIPO is input to the slave control circuit via the address input (AI) bus. The status output from the receiver is input to the slave controller circuit to indicate when a select protocol has started, when the address is ready to read, and when the select protocol has completed. The control bus input to the receiver from the slave control circuit enables the receiver to respond to a select protocol input. The receiver is only enabled when the backplane 1149.1 bus is in the RT/IDLE or TLRST state.

The receiver's controller determines when a first "I-S-D" signal sequence occurs on PTDI, indicating the start of a select protocol and address input. In response to this input sequence, the controller enables the SIPO to receive the serial address input on PTDI. The controller determines when a first "D-S-I" signal sequence occurs on PTDI, indicating the end of the address input and select protocol. In response to this input sequence, the controller signals the slave control circuit, via the status bus, to read the address, then terminates the select protocol input operation.

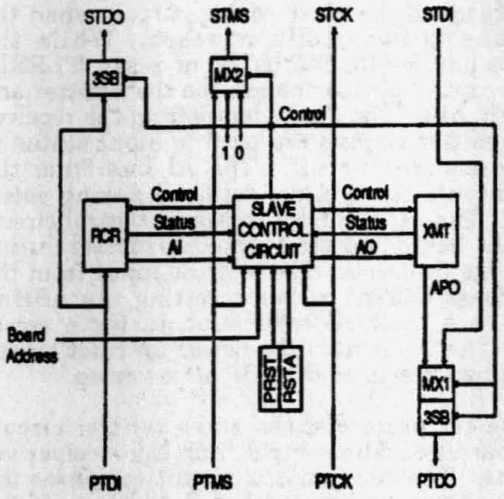


FIGURE 4 ASP Circuit Example

3.3.2 ASP Transmitter Circuit

The transmitter circuit consists of a controller and a parallel input/serial output (PISO) register. The transmitter's PISO register receives parallel data from the slave control circuit via the address output (AO) bus, and outputs the address serially to the PTDO output via the acknowledge protocol output (APO) signal and MX1. The transmitter's controller receives control input from the slave control circuit via the control bus, and outputs status to the slave control circuit via the status bus. The control input regulates the parallel to serial conversion process that takes place during the acknowledge protocol. The control input only enables the transmitter to output an acknowledge protocol when the backplane 1149.1 bus is in the RT/IDLE or TLRST state. The status output informs the slave control circuit of the transmitters status, i.e. whether the acknowledge protocol is in progress or complete.

At the beginning of an acknowledge protocol, the slave control circuit enables MX1 and the 3-state buffer (3SB) to pass the APO signal from the transmitter to the PTDO output. The slave control

circuit then inputs the board address to the transmitter via the AO bus. In response to the address input, the transmitter outputs an I and S signal on PTDO to start the acknowledge protocol, then transmits the address on PTDO. After the address is shifted out, the transmitter circuit outputs an S and I signal sequence to stop the acknowledge protocol.

3.3.3 ASP Slave Control Circuit

The slave control circuit regulates the operation of the transmitter, receiver, and multiplexers during select and acknowledge protocols. The slave control circuit is clocked by the PTCK input from the primary port. The PTMS input from the primary port indicates to the slave control circuit when the 1149.1 bus is busy, idle or reset. While the backplane bus is idle (RT/IDLE) or reset (TLRST), the slave control circuit enables the transmitter and receiver circuits. The status buses from the receiver and transmitter circuits are used to input status to the slave control circuit. The AI bus from the receiver inputs the address received during select protocols. The AO bus from the slave control circuit outputs the board address to the transmitter during acknowledge protocols. The address input from the reset address (RSTA) allows resetting the ASP in response to a reset address input during a select protocol. The input from the power up reset circuit (PRST) allows resetting the ASP at power up.

During select protocols, the slave control circuit receives parallel address input from the receiver via the AI bus. The slave control circuit compares the received address against the board address. If the addresses match, the ASP responds by outputting an acknowledge protocol.

During the acknowledge protocol, the slave control circuit outputs control to the transmitter to load the board address and initiate the acknowledge protocol. After the acknowledge protocol has been transmitted, the slave control circuit outputs control to connect the primary and secondary ports.

3.4 Resetting the ASP

When power is first applied to the ASP, the slave control circuit is reset by input from the power-up reset circuit (PRST). When reset, the transmitter and receiver circuits are initialized and the primary and secondary ports are disconnected by disabling the STDO and PTDO outputs and setting the STMS output high. The STCK output always outputs the PTCK input. If desired, a reset input could be used to reset the ASP as well.

The ASP can also be reset by inputting a select protocol with an address that matches the reset address (RSTA) inside the ASP. If the address input matches the reset address, the ASP is reset to the same state as described in the power-up reset. The reset address is the same for all ASPs so that a global reset of all ASPs can be achieved by the transmission of a single select protocol containing the reset address. The reset address is unique from the board addresses. A preferred value for the reset address is zero, since board addressing will usually start with an address of one. An acknowledge protocol is not transmitted after a reset address has been received, to avoid contention on the PTDO outputs of multiple ASPs.

3.5 Disconnecting a Selected ASP

When 1149.1 access to another board is required, a new select protocol is issued from the PSBM. When the previously selected ASP receives the new select protocol its primary and secondary ports are disconnected. If the new select protocol was issued while the backplane 1149.1 bus was in its RT/IDLE state (PTMS=0), MX2 of the disconnecting ASP outputs a logic zero on STMS, to force the board level 1149.1 bus to remain in the RT/IDLE state. If the new select protocol was issued while the backplane 1149.1 bus was in its TLRST state (PTMS=1), MX2 of the disconnecting ASP outputs a logic one on STMS, to force the board level 1149.1 bus to remain in the TLRST state. Once again, the ability to maintain the RT/IDLE state on a disconnected board is very important because it allows tests to be setup and executed on more than one board at a time.

3.6 Advantages in Using ASPs

When comparing the described 1149.1 star configuration against the ASP configuration of Figure 2, it is clear that the ASP approach eliminates the need for additional TMS signals required by the star configuration. Thus the ASP provides a method of overcoming the problem stated for the 1149.1 star configuration.

Also, when comparing the use of different backplane buses to interface into 1149.1 board environments vs using the ASP, it is clear that the ASP does not require use of sophisticated, and bandwidth reducing translation circuitry. Thus the ASP provides a method of overcoming the problems related with using different backplane buses to access 1149.1 board environments.

Further, since the select and acknowledge protocols can be transmitted while the 1149.1 bus is in either the RT/IDLE or TLRST states, the board being disconnected can be left in either an idle or reset state. Thus the ASP provides a method of overcoming the forced-reset-on-disconnect problem associated with the approach described by Bhavsar.

4.0 Commandable ASPs

In small backplanes, a single centralized PSBM may be all that is necessary to serially access boards for test and maintenance operations. However, as the number and complexity of boards in a backplane

grows, the serial access task increases to where a single centralized PSBM cannot handle the task in a timely manner. Anticipating the need for distributed test control, the ASP can be expanded to include a connection method and command set to enable board resident remote SBMs (RSBM) to autonomously test boards.

The addition of a command set, enables the ASP to perform other features in addition to its basic backplane to board connection function. Some of the commandable features include; (1) a method of connecting RSBMs to the board level 1149.1 bus, (2) a method of commanding RSBMs to independently test boards, (3) a method of non-intrusively monitoring the status of a remote test operation, and (4) a method of transferring data between a board resident memory and PSBM. The ASP's data transfer method achieves the same goal as the data transfer methods used in the P1149.5 and P1394 standard proposals. These commandable features further improve the ASPs ability to serve, in combination with 1149.1, as a system backplane test bus.

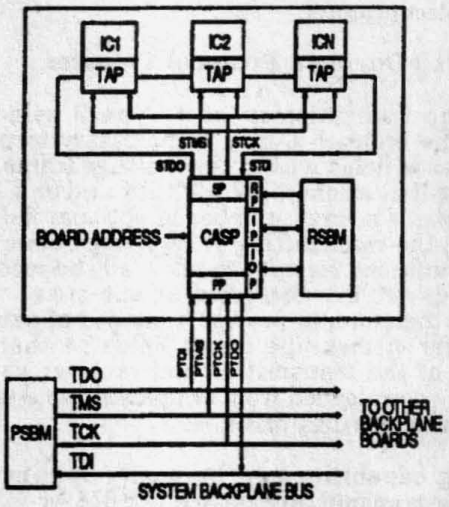


FIGURE 5 CASP Circuit Application

In Figure 5, a board is shown consisting of functional ICs (1-n), a commandable ASP (CASP), and a RSBM. The RSBM consists of a processor for executing local test programs, a memory for storage of test programs and data, an interrupt port, and an 1149.1 master interface port. The RSBM's processor and memory can either be dedicated for test or shared with the system logic on the board. The CASP consists of an 1149.1 primary port (PP) for interfacing to the backplane PSBM, an 1149.1 secondary port (SP) for interfacing to the functional ICs, an 1149.1 remote port (RP) for interfacing to the RSBM's master interface port, an interrupt port (IP) for interfacing to the RSBM's interrupt port, and an I/O port (IOP) for interfacing to the RSBM's memory. If required, additional I/O ports may be added to the CASP to provide parallel interfaces to other memories or I/O devices.

4.1 Expanded Select Protocol

To allow commands to be input to the CASP, the select protocol is expanded to allow for command transfer. In the ASP, a select protocol was defined by the transfer of a first I signal to start the select protocol, followed by the transfer of an address frame (of D signals) bounded by first and second S signals, followed by a second I signal to stop the select protocol. The select protocol of the CASP follows this format but expands the definition of the address frame into what is referred to as a message frame.

The select protocol message frame consists of a header containing an address (ADD) and command (CMD) field, and a cyclic redundancy check (CRC) field. The address field selects the CASP, the command field commands the CASP, and the CRC field is used for error detection. All fields within the message frame are separated by an S signal. The message frame may include optional fields between the header and the CRC field, as required by the command being sent. While the framing method allows fields to be transferred in either a fixed or variable D signal length, a fixed length field is preferred because it simplifies memory packing/unpacking operations, and improves error detection using simple signal counting techniques.

In Figure 6, examples of the two types of CASP select protocols are shown. Type 1 has a message frame containing the header's ADD and CMD fields, and the CRC field. Type 2 has a message frame containing the header's ADD and CMD fields, optional fields (OF) 1-N, and the CRC field.

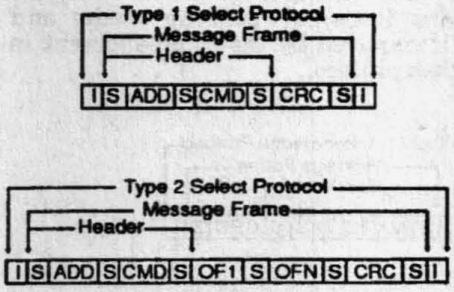


FIGURE 6 Expanded Select Protocols

In response to receiving either select protocol type (1 or 2) from the PSBM, the CASP checks its address against the received address field. If the addresses do not match, the CASP ignores the remainder of the select protocol and does not send an acknowledge protocol. If the addresses match, the CASP checks the command field against a set of

known commands to see what operation is to be performed. In response to an unknown command, the CASP ignores the remainder of the select protocol, sets a command error bit in its status register, then sends an appropriate acknowledge protocol type (1 or 2) to the PSBM, to indicate the command error. In response to a known command, the CASP receives the remainder of the select protocol, then matches the received CRC field against a CRC it calculates on the data received in the select protocol. If the CRCs do not match, the CASP ignores the command, sets a CRC error bit in its status register, then sends an appropriate acknowledge protocol type to the PSBM, to indicate the CRC error. If the CRCs match, the CASP sends an appropriate acknowledge protocol type to the PSBM, to indicate that an error-free select protocol was received.

4.2 Expanded Acknowledge Protocol

To allow the PSBM to verify that the command input to the CASP was received correctly, the acknowledge protocol is expanded to allow for status transfer. In the ASP, the acknowledge protocol was defined by the transfer of a first I signal to start the acknowledge protocol, followed by the transfer of an address frame bounded by first and second S signals, followed by a second I signal to stop the acknowledge protocol. The acknowledge protocol of the CASP follows this format but expands the definition of the address frame into a message frame.

The acknowledge protocol message frame consists of a header containing an address (ADD) and status (STS) field, and a CRC field. The address field identifies the CASP, the status field informs the PSBM of the CASP status, and the CRC field is used for error detection. All fields within the message frame are separated by an S signal. The message frame within the acknowledge protocol may include optional data fields between the header and the CRC field, if required by the command sent in the previous select protocol.

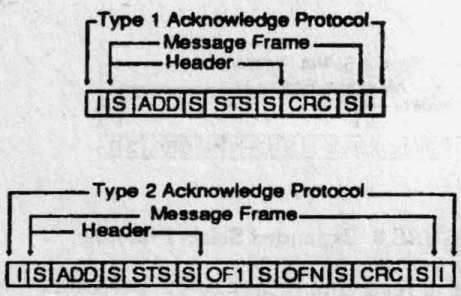


FIGURE 7 Expanded Acknowledge Protocols

In Figure 7, examples of the two types of CASP acknowledge protocols are shown. Type 1 has a message frame containing the header's ADD and STS fields, and the CRC field. Type 2 has a message frame containing the header's ADD and STS fields, optional fields (OF) 1-N, and the CRC field.

In response to receiving either acknowledge protocol type (1 or 2) from the CASP, the PSBM checks that the correct address field was received, then checks the status field for errors. After checking the address and status fields, the PSBM receives the remainder of the acknowledge protocol. At the end of the acknowledge protocol, the PSBM matches the received CRC field against a CRC it calculates on the received data. If the correct address field was received, the status field indicates no errors, and the CRCs match, the PSBM is assured that the CASP has properly received and executed the command sent in the previous select protocol. If a failure occurred in the address or status field test, the PSBM knows that the CASP did not properly receive the previous command select protocol. If the address and status fields test passed, but a CRC error occurred, the PSBM knows that an error in the optional data fields following the header fields occurred. In response to an acknowledge protocol error, the PSBM can resend the command via another select protocol.

4.3 Pausing During a Protocol Transfer

During the transmission of a Type 2 select or acknowledge protocol it may be necessary to pause the transfer of fields within the message frame, due to memory limitations of the PSBM and/or CASP. For example, if a large number of optional fields is being sent, the transmitting or receiving device may not have sufficient memory to allow all the message frame fields to be transferred at one time. It is necessary, therefore, to provide a method of pausing the transfer of message frame fields so that the memories of the transmitter and receiver can be periodically downloaded from or uploaded to a larger memory, such as a disk drive.

A pausing capability can be easily realized by having the transmitting device (PSBM or CASP) output additional S signals following the S signal that separates the fields. Using this approach, pausing can occur between any two field frames. The length of the pause is determined by the number of additional S signals output from the transmitter. The transferring of fields within the message frame is resumed when the transmitting device outputs a D signal to start the next field.

4.4 CASP Command Set

The following commands form the basic CASP command set. Some of the commands support connecting the CASP's secondary port up to either the primary or remote port, while other commands support data transfer operations between a PSBM and a board resident memory, via the CASP's I/O port. Other commands can be added as required.

4.4.1 Connect PSBM Command

When the PSBM needs to access the board ICs, it sends a connect PSBM command to the CASP via a type 1 select protocol. In response to the connect PSBM command, the CASP sets the "PSBM connected" status bit, sends a reply to the PSBM using a type 1 acknowledge protocol, then connects its primary and secondary ports.

After receiving the acknowledge protocol from the CASP and verifying the "PSBM connected" status bit is set, the PSBM can access the board ICs using the 1149.1 bus protocol. After the connect PSBM command has been input to the CASP, other commands that do not effect the connection between the primary and secondary ports, such as the read and write commands, can be input to and executed by the CASP.

4.4.2 Disconnect PSBM Command

When the PSBM completes its access of the board ICs, it sends a disconnect PSBM command to the CASP via a type 1 select protocol. In response to the disconnect PSBM command, the CASP resets the "PSBM connected" status bit, sends a reply to the PSBM using a type 1 acknowledge protocol, then disconnects its primary and secondary ports. After receiving the acknowledge protocol from the CASP, the PSBM verifies the "PSBM disconnected" status bit has been reset.

4.4.3 Connect RSBM Command

When the PSBM requires the RSBM to access the board ICs, it sends a connect RSBM command to the CASP via a type 1 select protocol. In response to the connect RSBM command, the CASP sets the "RSBM connected" status bit, sends a reply to the PSBM using a type 1 acknowledge protocol, then connects its remote and secondary ports. After receiving the acknowledge protocol from the CASP, the PSBM verifies the "RSBM connected" status bit is set.

After the connect RSBM command has been input to the CASP, other commands that do not effect the connection between the remote and secondary ports, such as the read and write commands, can be input to and executed by the CASP. For example, the PSBM can send a command to the RSBM, via the CASP's I/O port, to initiate the remote access operation using a write command. Further, the PSBM can monitor the status of the remote access operation, via the CASP's I/O port, using a read command.

4.4.4 Disconnect RSBM Command

When the PSBM determines that the remote access of the board ICs is complete, it sends a disconnect RSBM command to the CASP via a type 1 select protocol. In response to the disconnect RSBM command, the CASP resets the "RSBM connected" status bit, sends a reply to the PSBM using a type 1 acknowledge protocol, then disconnects its remote and secondary ports. After receiving the acknowledge protocol from the CASP, the PSBM verifies the "RSBM Connected" status bit has been reset.

4.4.5 Write Command

When data is to be transferred from the PSBM to a memory via the CASP's I/O port, the CASP receives a write command from the PSBM via a type 2 select protocol. The write command select protocol message frame contains: a header with the CASP address and write command, a starting address field where the first data field will be written, a count field indicating the number of data fields to be written, one or more data fields, and a CRC field.

At the beginning of the write command select protocol, the CASP checks its address against the received address field and the write command against known commands. In response to the write command, the CASP outputs the received starting address field on the I/O port and stores the write count field. Next, the CASP writes the first received data field to the addressed memory location and decrements the count field. If the count field is not zero after the first write operation, the ASP increments the starting memory address, writes the next received data field, and decrements the count field again. These steps are repeated until the count field decrements to zero.

When the count field decrements to zero, the CASP realizes that the last data field has been received and written to memory and the next field received is the CRC. The CASP compares the received CRC with a CRC it has calculated on the received data to check for errors, then sends an appropriate reply to the PSBM using a type 1 acknowledge protocol. After receiving the acknowledge protocol from the CASP, the PSBM verifies that the write command was successful by checking the address and status fields within the header and the CRC field for errors.

While multiple data fields will usually be transferred during the write command to upload a test program or data, a single data field can be transmitted by simply setting the count field to one. An example of a single data write command is when the PSBM sends a command to the RSBM instructing it to execute a remote test operation, such as "initiate self-test #1".

4.4.6 Read Command

When data is to be transferred from a memory to the PSBM via the CASP I/O port, the CASP receives a read command from the PSBM via a type 2 select protocol. The read command select protocol message frame contains: a header with the CASP address and read command, a starting address field where the first data field will be read, a count field

indicating the number of data fields to be read, and a CRC field.

At the beginning of the read command select protocol, the CASP checks its address against the received address field and the read command against known commands. In response to the read command, the CASP stores the received starting address and read count fields, then matches the received CRC against the calculated CRC.

After the read command select protocol completes, the CASP outputs the starting memory address from the I/O port, reads the first data field from memory, decrements the read count field, and starts a type 2 acknowledge protocol to transfer the data read from the memory to the PSBM. If the read count field is not zero after the first read operation, the CASP increments the memory address, and repeats the memory read and acknowledge protocol transfer sequence. When the read count field decrements to zero, the CASP realizes that the last data field has been read from memory. After sending the last data field to the PSBM, the CASP sends the calculated CRC field then terminates the acknowledge protocol.

In response to the read command acknowledge protocol, the PSBM checks the header's address and status fields, receives and stores a predetermined number of data fields, then matches the received CRC field against a calculated CRC. If no errors are found, the PSBM is assured that the read command has been executed and the data received is correct.

While multiple data fields will usually be transferred during the read command acknowledge protocol, to download test or system data, a single data field can be transmitted by simply setting the count field to one. An example of a single data read command is when the PSBM needs only to read the status of the RSBM.

4.4.7 Read Status Command

To allow the PSBM to read the CASP's internal status register, the PSBM sends a read status command to the CASP via a type 1 select protocol. The read status command select protocol message frame contains a header with the CASP address and read status command, and a CRC field. After checking the read status command select protocol's address, command, and CRC fields, the CASP sends a type 1 acknowledge protocol to the PSBM to transfer its status register field to the PSBM. In response to the read status command acknowledge protocol, the PSBM can check the settings of the CASP's status register bits.

The read status command, like the read and write commands, can be executed without effecting any of the connection type commands. The read status command allows the PSBM to monitor the internal status of CASP, as well as external status inputs, such as the RSBM's interrupt input. The following list defines the required status bits in the CASP's status register.

Command Error – A status register bit indicating an unknown command was received.

CRC Error – A status register bit indicating a mismatch between the received and calculated CRC.

Interrupt Request – A status register bit indicating the occurrence of an external interrupt request.

Primary Port Connected – A status register bit indicating a connection between the primary and secondary ports.

Remote Port Connected – A status register indicating a connection between the remote and secondary ports.

Secondary Port Idle – A status register bit indicating that the secondary port is idle (STMS=0).

Secondary Port Reset – A status register bit indicating that the secondary port is reset (STMS=1).

4.5 Global Commanding

To support a method of executing global commands, CASPs can include a global command address (GCA), similar to the reset address (RSTA) in Figure 4. During a global command select protocol, all CASPs respond to the GCA to execute the command that follows. To avoid bus contention on PTDO, CASPs do not output acknowledge protocols in response to global command select protocols.

5.0 Adapting the CASP for 2-wire Backplanes

As mentioned in the "Interfacing P1394 to 1149.1" section, newer 32-bit IEEE backplane standards only allocate two wires for a backplane level serial bus. If this trend continues, only a 2-wire serial bus, such as P1394, can be used in future backplanes, since both 1149.1 and P1149.5 require more than two bus wires. While P1394 is a good high speed 2-wire communications bus, its complex protocols and circuitry may be too sophisticated and/or costly for the simpler access applications involved in serial testing. To provide an alternate 2-wire serial bus for newer backplane standards, the primary port of the CASP can be easily adapted to communicate the select and acknowledge protocols using only two wires.

In Figure 8, the CASP's primary port is shown interfaced to a 2-wire PSBM via a serial input/output (SIO) wire and a clock (CLK) wire. The SIO wire combines the unidirectional TDO and TDI backplane wiring channels into a single bidirectional wiring channel. The SIO wire is capable of transferring the select and acknowledge protocols between the PSBM and CASP in response to the CLK output from the PSBM. The select and acknowledge protocols can both be transmitted on a single wire since they are transmitted at different times, as shown in Figure 3. When the CASP is

used in a 2-wire backplane, the connect and disconnect PSBM commands are no longer valid, since an 1149.1 connection is not possible in two wires. However, all the other CASP commands can be used, as previously described, to enable remote test access and data transfer operations.

Using this approach, a cost-effective 2-wire serial bus can optionally be used in newer backplane standards, in place of P1394, to provide a simple access method for test and data transfer operations. An important advantage of this approach is that it allows a common backplane test methodology to be developed and practiced, independent of the physical interfaces used in various system backplanes. For example, a backplane test access program, designed using a common CASP command set, could be used in either a 4 or 2-wire serial backplane environment. The combination of a common set of backplane test commands and a flexible serial interface, provides the building blocks from which a standard backplane test access language could be developed.

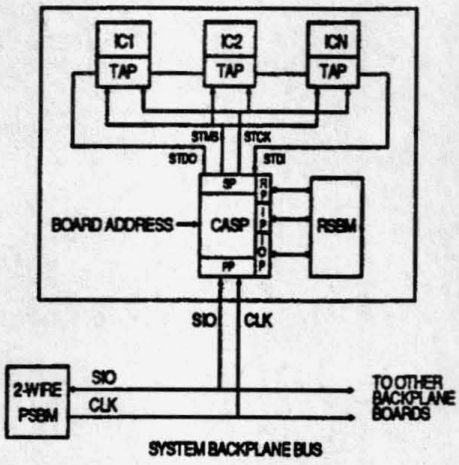


FIGURE 8 2-Wire CASP Backplane Interface

In future updates to the current 32-bit backplane buses, and in definitions of future 64-bit buses, it may be beneficial for test representatives to participate in backplane working groups to help specify backplane test bus requirements. Since a need will probably exist for both a 2-wire communications bus (like P1394) and a 2-wire test bus (like the one proposed here), an ideal scenario would be for backplane standards to specify two pairs of backplane wires so that both serial bus types could be supported. In this way, both serial buses could operate full-time in a backplane environment to optimally perform the task each was designed for. Also, since separate interfaces for the higher performance communications bus and lower performance test bus could be designed more efficiently, a lower cost of implementation would probably be achieved. Further, if separate serial buses existed at the backplane level for test and communication, the software for each bus could be designed more efficiently and executed in parallel.

6.0 Summary and Conclusion

This paper has described a new approach of accessing 1149.1 based boards in a backplane environment. The approach can be used as a simple backplane to board connection method or expanded to include commandable features considered useful in a backplane environment.

The ASP provides a simple backplane to board connection circuit to effectuate expanded use of the 1149.1 test bus. The select and acknowledge protocols can be transmitted between a PSBM and ASP using normal 1149.1 scan operations, assuming the PSBM can hold its TMS signal at a 1 or 0 during scan. Therefore, existing 1149.1 bus masters and software can easily be adapted to use this approach. The ASP circuit is simple and can be assembled in small footprint packages (20 pins), resulting in a low cost, low area overhead, backplane-to-board level 1149.1 test interface.

The commandable ASP (CASP) provides a way of expanding the basic ASP and protocols to suit the needs of more demanding applications, while maintaining protocol compatibility with the 1149.1 standard. The ability of the CASP to support board resident RSBMs, provides a structured method of designing systems capable of distributed test control. The ability of the CASP to support data transfer, provides a method of emulating the data transfer features being developed in the IEEE P1149.5 and P1394 serial bus standards. The ability of the CASP to operate in a 2-wire backplane environment, allows it to serve as an alternate serial bus to P1394 when only simple test access is required in a system.

The advantages offered by this new approach are: (1) direct compatibility with 1149.1, (2) improved serial data transfer bandwidth, (3) simple, cost effective implementation, (4) easily expandable to include other features useful in backplane applications, and (5) capable of being used in either a 4 or 2-wire serial bus backplane environment.

References

1 IEEE Std 1149.1-1990, Standard Test Access Port and Boundary Scan Architecture

2 IEEE P1149.5, Standard Module Test and Maintenance Bus Protocol.

3 J. Andrews, "IEEE's 1149.5 Bus Facilitates JTAG", ATE & Instrumentation Conference, January 1991.

4 IEEE P1394, High Speed Serial Bus

5 IEEE/ANSI 896, Futurebus+

6 IEEE/ANSI 960, FASTBUS

7 IEEE/ANSI 1014, VMEbus

8 IEEE/ANSI 1295, Multibus II

9 D. Bhavsar, "An Architecture for Extending the IEEE Standard 1149.1 Test Access Port to System Backplanes", International Test Conference, October 1991.

Built-In Self-Test (BIST) Using Boundary Scan

SCTA043A
December 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	*Page*
Abstract	**7–105**
Introduction	**7–105**
SCOPE Architecture	**7–105**
Adapting SCOPE to 1149.1	**7–106**
1149.1 Architecture and Test Bus	**7–106**
Interrupt Pin and Application	**7–107**
Test Bus and Interrupt Pin Connections	**7–107**
1149.1 Boundary Test Instructions	**7–108**
EXTEST Instruction	7–108
SAMPLE Instruction	7–108
BYPASS Instruction	7–108
SCOPE Boundary Test Instructions	**7–109**
TOGGLE/SAMPLE Instruction	7–109
HIGHZ Instruction	7–110
CLAMP Instruction	7–110
BOUNDARY SELF-TEST Instruction	7–110
BOUNDARY READ Instruction	7–110
BOUNDARY BIST Instruction	7–110
Summary	**7–111**
Acknowledgment	**7–112**
References	**7–112**

List of Illustrations

Figure	*Title*	*Page*
1	IEEE 1149.1 Architecture	7–106
2	IEEE 1149.1 Architecture	7–107
3	Using TOGGLE/SAMPLE to Test Path Delays	7–109
4	Testing Combinational Logic With IEEE 1149.1/BIST	7–111

SCOPE is a trademark of Texas Instruments Incorporated.

Abstract

The IEEE standard boundary-scan framework and four-wire serial testability bus have a positive impact on design for testability at all levels of electronic assembly, but do not solve all the testing problems facing the electronics industry. They form the basis from which other test techniques can be developed to further facilitate the testing of chips and systems. This paper describes a test architecture, based on the IEEE 1149.1 boundary-scan and test-bus standard. This architecture extends the capability of boundary testing from a purely scan-based structure into one that also supports a built-in self-test (BIST) capability.

Introduction

Before the formation of the Joint Test Action Group (JTAG) and the IEEE 1149.1 standard, the Test Automation Department of TI's Defense Systems and Electronics Group (DSEG), had considered boundary scan as a method to improve the test, integration, and maintenance of systems being designed for the Department of Defense (DoD). From this study, an architecture was developed, along with a library of specialized test cells particularly well-suited for boundary-scan and BIST applications.

SCOPE Architecture

The test architecture, referred to as System Controllability, Observability, and Partitioning Environment (SCOPE™), provides boundary scan and BIST capability to each input and output pin of the host IC. The architecture is supported by a library of modular bit slice called SCOPE cells that offer a range of boundary test capability. Some of the cells are targeted for simple boundary-scan applications. Other cells support the design of more sophisticated boundary test circuits such as pseudorandom and binary pattern generators and parallel signature analysis registers. During test, the SCOPE cells receive control from the test bus interface to execute a boundary scan or BIST controllability and observability test operation. One novel feature of the SCOPE architecture is its ability to activate the boundary test circuits while the host IC is in a normal operational mode. This capability provides boundary test features to support system integration, emulation, and at-speed testing.

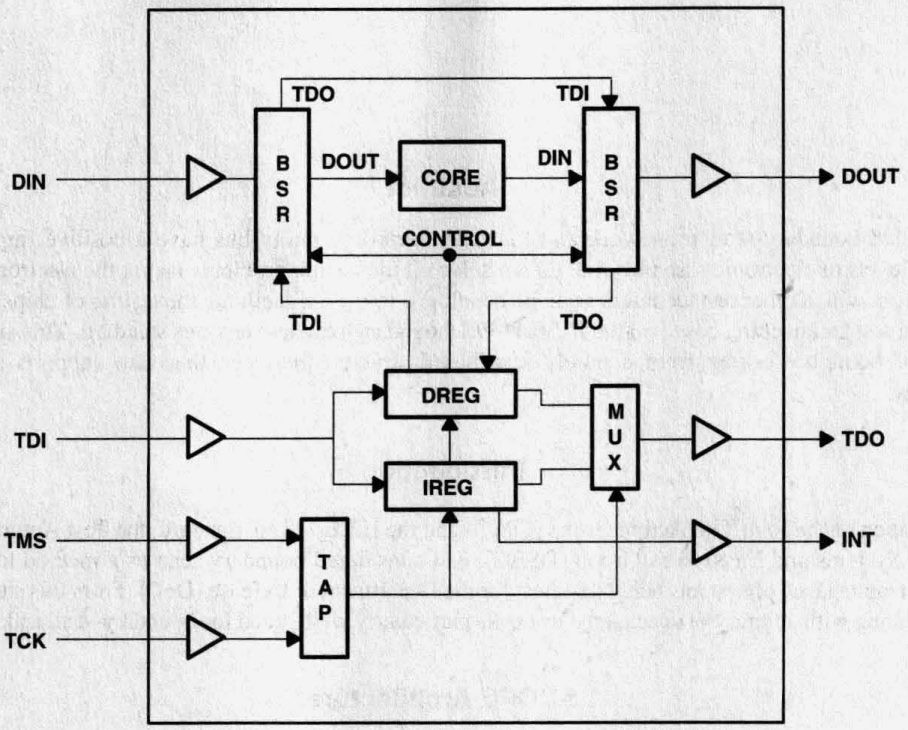


Figure 1. IEEE 1149.1 Architecture

Adapting SCOPE to 1149.1

Adapting the SCOPE architecture to the 1149.1 standard was simple because the existing test bus and architecture had similar functionality and required the same number of serial test bus pins. The following sections describe the boundary test features provided in the SCOPE architecture to support the mandatory test instructions required by the 1149.1 standard, as well as some of the internal test capabilities developed to extend the range of boundary testing.

1149.1 Architecture and Test Bus

The 1149.1 boundary-scan architecture and four-wire test bus interface is shown in Figure 1. The test architecture consists of a test access port (TAP), two separate shift register paths for data (DREG) and instruction (IREG) and a boundary-scan path bordering the IC's input and output pins. The boundary-scan path is one of two required scan paths residing in the DREG and is shown outside the DREG for clarity. The other required DREG scan path is a bypass register that consists of a single scan cell and is used to provide an abbreviated path through the DREG when testing is not being performed. In addition to these two required data registers, any number of user-defined shift registers can be included in the DREG to allow expanding the architecture to support additional test capabilities.

The 1149.1 test bus interface consists of a test data input (TDI), a test data output (TDO), a test mode select (TMS), and a test clock (TCK). The TDI is routed to both the DREG and IREG and is used to transfer serial data into one of the two shift registers during a scan operation. The TDO is selected to output serial data from either the DREG or IREG during a scan operation. The TMS and TCK are control inputs to the TAP. These control signals direct the operation of the architecture to perform scan operations to either the DREG or IREG, or to issue a reset condition to the test logic if test operations are not being performed.

Interrupt Pin and Application

The interrupt output signal is not defined in the IEEE 1149.1 specification but has been envisioned as a potential mode of operation for SCOPE architectures. Although this signal is not a standard function in every SCOPE IC product, it is a powerful function that can be implemented when using TI's ASIC library SCOPE cells.

In Figure 1, the interrupt (INT) output signal issued from the IREG is a signal defined in the SCOPE architecture. This signal can be used for, among other things, the output of a parity test indication of whether the instruction shifted into the IREG has the correct number of ones for even parity. The test instructions for the SCOPE architecture are all designed to a fixed length and include even parity. If an instruction is shifted in with odd parity, the interrupt output signal is set low when the TAP enters the pause-IR state to indicate the error back to a bus controller device. The pause-IR state is a steady state in the TAP controller's state diagram (see the IEEE 1149.1 specifications) that can be entered before terminating the instruction shift operation. The SCOPE architecture takes advantage of the pause-IR state to verify that the instruction shifted in has the correct parity. If the INT output is low, indicating a parity error condition, the bus master will repeat the instruction scan operation again. INT output high indicates a good parity condition. If so, the bus master will complete the instruction scan operation by updating the instruction into the IREG output latch to issue the appropriate test control to the architecture.

Test Bus and Interrupt Pin Connections

In the example circuit of Figure 2, three ICs are shown interconnected functionally via direct wiring bus paths. During normal operation, ICs 1, 2, and 3 receive input via their data input (DIN) buses and issue output via their data output (DOUT) buses to execute a designed circuit function. Also, the three ICs are shown interconnected in a serial ring configuration via the four-wire test bus. The TIC block in each IC stands for test interface and control and is representative of the TAP, IREG, and DREG sections shown in Figure 1. The 1149.1 test bus is designed to allow scan operations to occur through the TIC while the IC is operational. This is possible because the test pins and the required test logic of the boundary scan architecture (TAP, IREG, DREG boundary and bypass registers) are dedicated for test and cannot be reused for functional purposes.

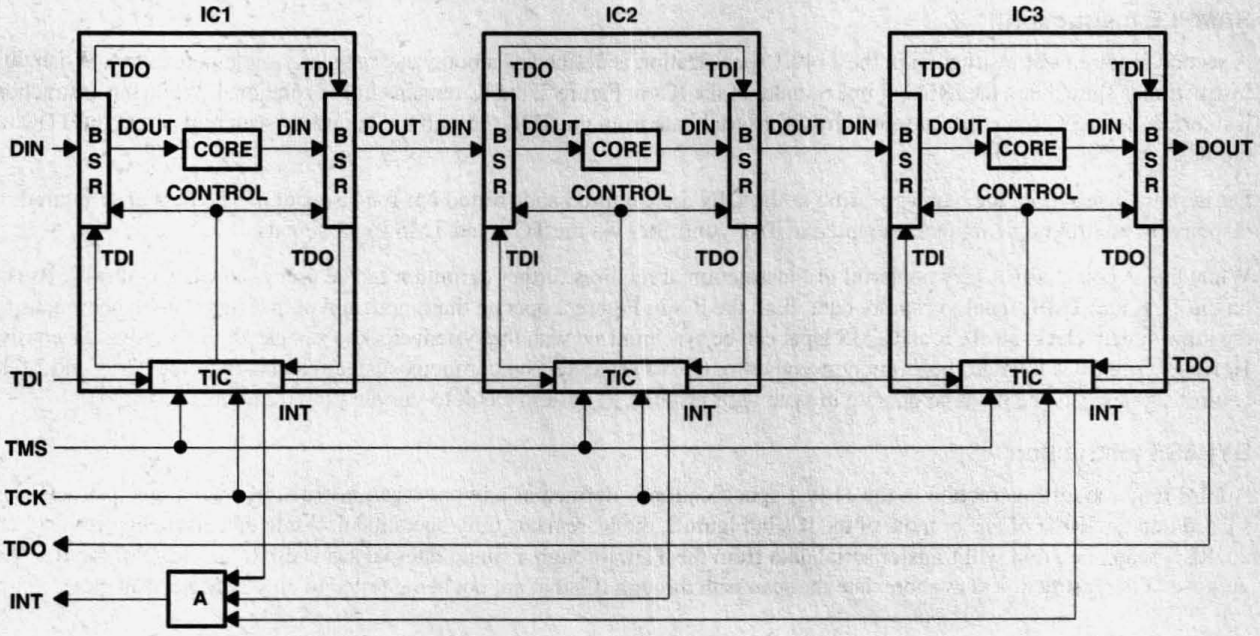


Figure 2. IEEE 1149.1 Architecture

The INT output signal from each IC is input to an external AND function to produce a global INT output signal. The global INT signal from the AND function is input to a bus master device. The device includes a five-pin interface to support the four required 1149.1 test bus signals and the additional INT signal. During the pause-IR state of an instruction register scan operation, each local INT signal outputs a parity pass or fail condition. If all local INT outputs are high, the AND function outputs a high to the bus master to confirm good parity. If one or more local INT outputs are low, the AND function outputs a low to the bus master to indicate an instruction parity failure. The advantage of using an active AND function to combine the local INT outputs versus a passive wired-OR configuration is speed. Speed is not a high priority for global parity testing. Other INT functions defined in the SCOPE architecture do require a minimum delay between the occurrence of one or more local INT outputs and a resulting global INT output signal to the bus master.

1149.1 Boundary Test Instructions

The following is a description of the required 1149.1 test instructions that are included in the SCOPE architecture. The other optional 1149.1 instructions (INTEST, IDCODE, RUNBIST) can be implemented as required.

EXTEST Instruction

One of the required test instructions in the 1149.1 specification is defined as an external boundary test (EXTEST) instruction. When this instruction is shifted into the IREG of the ICs in Figure 2, the ICs are forced into an off-line test mode. While this instruction is in effect, the test bus can shift data through the boundary scan registers of each IC to observe and control the external DIN and DOUT buses, respectively. As seen in the circuit of Figure 2, serialized test patterns can be shifted in and applied from the output boundary scan register's DOUT to drive the wiring interconnect to the DIN of neighboring ICs. After the test pattern is output, the DIN of the receiving ICs are captured. Following the data capture operation, the boundary registers are shifted to load the next external test pattern and to extract the response from the first test pattern. This process is repeated until the wiring interconnects are tested. This test provides a simple and thorough verification of the wiring connections between ICs in a circuit and is the key motivation behind the JTAG initiative.

SAMPLE Instruction

A second required test instruction in the 1149.1 specification is defined as a boundary register sample instruction. When this instruction is shifted into the IREG of one or more of the ICs in Figure 2, the IC remains fully operational. While this instruction is in effect, a DREG scan operation will transfer serial data from the TDI, through the boundary scan register, to the TDO of the IC.

During this instruction, the data appearing at the DIN are captured and shifted out for inspection. The data are captured in response to control being input to the internal TAP controller via the TCK and TMS input signals.

While this is potentially a very powerful test instruction, it requires further definition by the user as to when control is issued on the TCK and TMS signal to capture data. If all the ICs in Figure 2 operate their input and output functions synchronous to the same system clock, the TCK and TMS input can be synchronized with the system clock to sample all the ICs simultaneously. However, if all ICs operate their functions synchronous to separate asynchronous system clocks, then the TMS and TCK control signals must be made to operate in sync with just one IC system clock to sample each individual IC.

BYPASS Instruction

A third required test instruction in the 1149.1 specification is defined as a bypass scan instruction. When this instruction is shifted into the IREG of one or more of the ICs in Figure 2, the IC remains fully operational. While this instruction is in effect, a DREG scan operation will transfer serial data from the TDI, through a single internal scan cell, to the TDO of the IC. The purpose of the instruction is to abbreviate the scan path through ICs that are not being tested to only a single-scan clock delay.

SCOPE Boundary Test Instructions

To expand the test capability of a boundary-scan architecture and thus support a broader range of testing needs, additional test instructions and hardware capabilities are defined in the SCOPE architecture. Following is a description of some of these additional test instructions and the benefits gained from them.

TOGGLE/SAMPLE Instruction

The 1149.1 EXTEST instruction is excellent for testing the integrity of wiring interconnects between the ICs. However, it cannot be used effectively to test for timing delay problems that may occur between an output buffer of a driving IC and an input buffer of a receiving IC. To test for signal-path time delays, data must be applied from the outputs of one IC and be sampled rapidly into the inputs of another IC. To perform a delay test by transitioning through the TAP controller's state diagrams would take at least 1.5 TCK cycles from the time data are applied from one IC's output boundary in the update-DR state to when the data could be captured at the input boundary of another IC during the capture-DR state.

To perform faster, simple signal-path delay tests between an output and input boundary, SCOPE cells were designed to include a toggle mode. This mode can be invoked by a TOGGLE/SAMPLE test instruction to allow the output boundary of an IC to drive out alternating logic states on the falling edge of successive TCK inputs. The same instruction also configures the SCOPE cells on the IC input boundary into a sample mode. This allows the data appearing at the inputs to be captured on the rising edge of successive TCK inputs. Using this approach, signal-path delay testing can be performed over the time interval between a falling and rising edge of TCK. For example, with a 10-MHz, 50-percent duty-cycle TCK input, a signal-path delay exceeding 50 nanoseconds can be detected using this approach.

This instruction is executed while the TAP is in the run test/idle (RT/IDLE) state, so TAP state transitions are not required. After the input cells sample the toggled logic state, the data captured are shifted out for inspection. While this delay testing approach is still rather crude compared to the resolution of state-of-the-art test equipment, it still can serve a purpose at the circuit-board level. Using this technique, typical types of signal-path delays that can be identified are shown in Figure 3. These include combinational logic delays between the boundaries of larger ICs, delays associated with open collector-type output buffers, and delays associated with output buffers with high fanout loads.

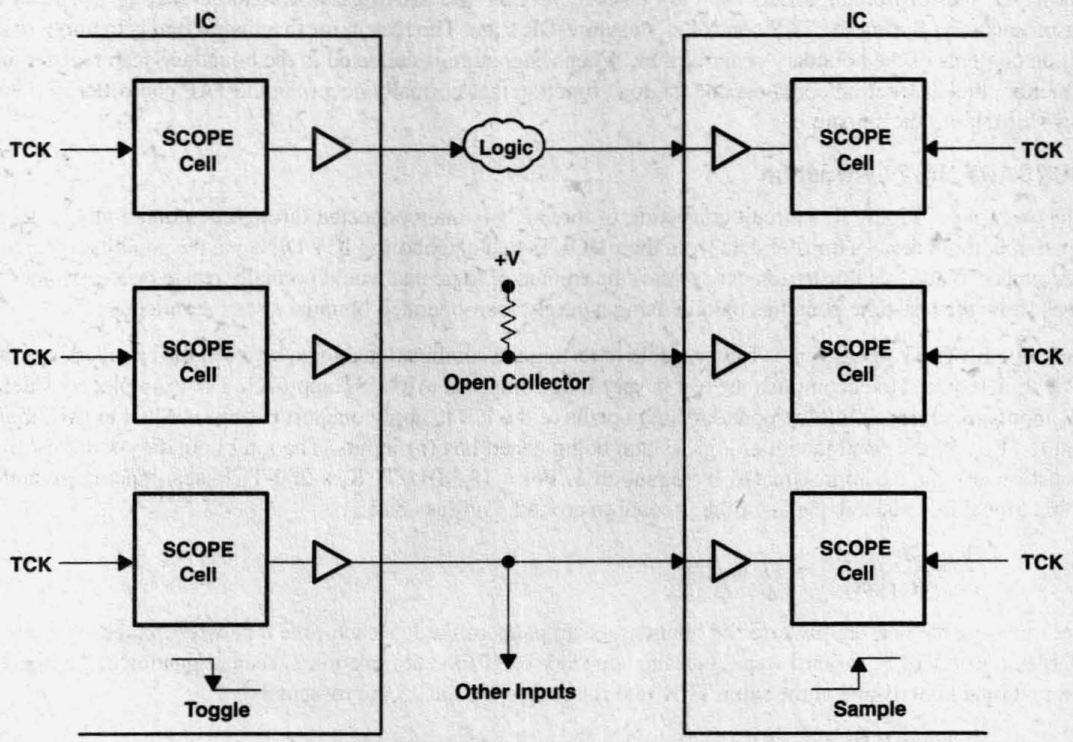


Figure 3. Using TOGGLE/SAMPLE to Test Path Delays

HIGHZ Instruction

When this instruction is shifted into the instruction register, the IC is set in an off-line test mode, and the output buffers are placed in a high-impedance state. While this instruction is in effect, the bypass register is selected to shift data through the DREG from the TDI to the TDO. This instruction is included to ease in-circuit testing of ICs in a circuit that does not incorporate boundary scan. Since the output buffers can be set tristate, the concerns with backdriving the output buffers of one IC to apply a test to a neighboring IC are reduced.

CLAMP Instruction

When this instruction is shifted into the instruction register, the IC is set in an off-line test mode. The input and output buffers are driven to a predetermined output pattern that has been scanned into the boundary register. While this instruction is in effect, the bypass register is selected to shift data through the DREG from the TDI to the TDO. This instruction allows the output signals of one or more ICs in a circuit to be set and left in a preferred output state while testing is being performed on one or more neighboring ICs in the circuit. The key to this instruction is that it allows the bypass register to be selected while the IC remains in a test mode with outputs set, as required, for testing. The 1149.1 clamp instruction forces the IC into normal operation when the bypass register is selected; thus, any preferred output signal setting for test cannot be maintained during the instruction.

BOUNDARY SELF-TEST Instruction

When this instruction is shifted into the instruction register, the boundary scan cells are configured to allow self-testing of each cell in the scan path. The self-test exercises most of the logic in each test cell. The test involves initializing the cells with a test pattern via a scan operation, followed by a second scan operation to shift out the test results. If the cells pass the self-test, the pattern shifted out during the second scan operation will be the inverse of the first pattern shifted in. During this instruction, the IC remains in its normal operation mode to allow self-testing to occur in the background, if desired.

BOUNDARY READ Instruction

When this instruction is shifted into the instruction register, the boundary-scan register is selected to shift data from the TDI to the TDO. This instruction differs from the 1149.1 EXTEST and SAMPLE instruction in that the boundary cells remain in their present state during the TAP controller's capture-DR state. The reason for this instruction is to allow shifting out of the existing contents of the boundary-scan register. When a signature is collected in the boundary-scan register during a run test instruction, this instruction could disable the load function that normally occurs in the TAP controller's capture-DR state to allow shifting out the signature.

BOUNDARY BIST Instruction

In the example of Figure 4, a circuit consisting of three ICs is interconnected through combinational logic islands. During normal operation, the ICs transfer data from their DOUTs to a neighboring IC's DINs via the combinational logic and wiring interconnect. While this illustration exaggerates the amount of logic that would normally reside between major ICs in a circuit, it does show the test-time penalties paid in using a purely scan-operated boundary-scan architecture.

The 1149.1 EXTEST instruction is fully capable of testing the combinational logic between the boundaries of the ICs in Figure 4. The time required to accomplish the test is very long compared to a BIST approach. For example, consider the number of TCK inputs required to shift the boundary-scan paths of the ICs to apply one test pattern is equal to (M), the TCK period is equal to (T), and the combinational logic island being tested has (n) inputs. The total boundary-scan test time to apply an exhaustive test can be approximated by Equation 1. For a 10-MHz TCK, a 200-TCK scan operation, and an 8-bit-wide combinational logic island, the test time is equal to around 5 milliseconds.

$$\frac{Boundary\ Scan}{Test\ Time} = (T\ M\ 2^n) \quad (1)$$

By eliminating the need to traverse the boundary-scan paths of the ICs each time a new test pattern is to be applied, the M variable drops out of Equation 1 to produce the boundary BIST time in Equation 2. Using Equation 2, the time to test the same combinational logic island at the same TCK rate is equal to around 25 microseconds.

$$\frac{Boundary\ BIST}{Test\ Time} = (T\ 2^n) \quad (2)$$

Comparing the 5-millisecond, scan-operated test time against the 25-microsecond BIST-operated test time results in a 99.5-percent reduction in test time using the BIST approach. That is why a boundary BIST capability is included in the SCOPE architecture.

To support a boundary BIST capability, the SCOPE cell library includes cells that can be used to construct boundary registers with pattern-generation and data-compression capabilities. The pattern-generation test cells can produce either pseudorandom or binary output test patterns. The data-compression test cells operate together as a parallel signature analysis (PSA) register. The cells also include programmable polynomial taps to allow modifying the feedback connections. This optimizes the operation of the pattern-generation and data-compression register for a particular external logic configuration.

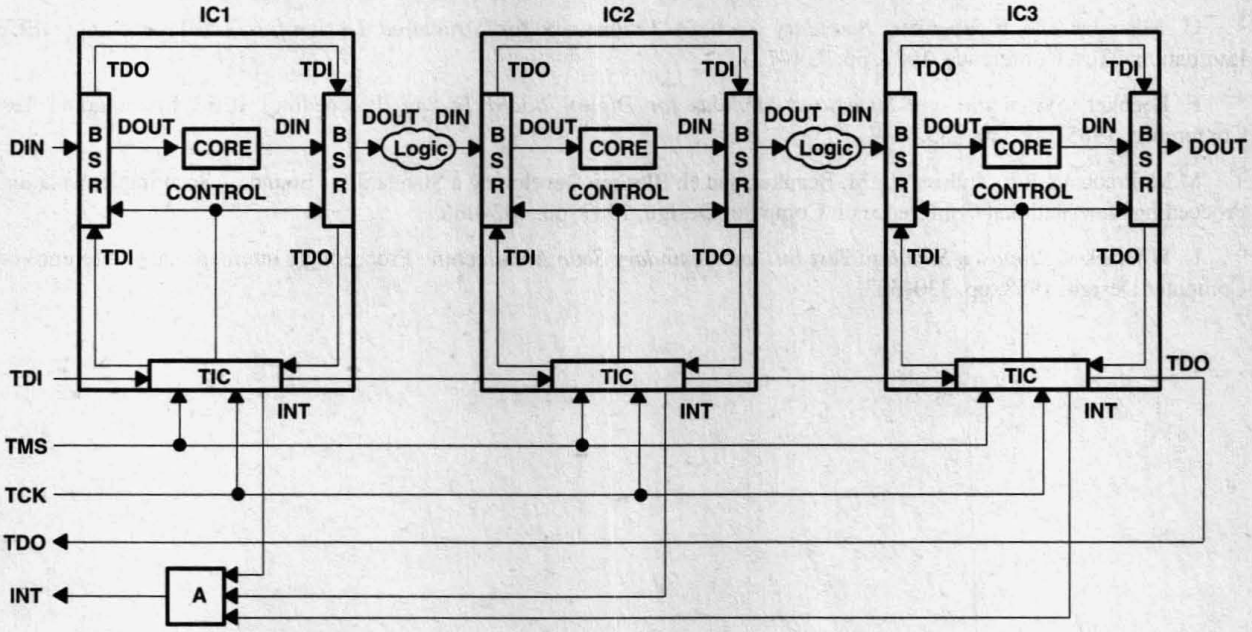


Figure 4. Testing Combinational Logic With IEEE 1149.1/BIST

When the boundary scan paths of the ICs in Figure 4 are designed using these advanced test cells, the combinational logic islands are tested much more easily and quickly. The boundary BIST test is set up by scanning seed values into the input and output boundary register sections that border the combination logic islands. After the boundary registers are set up, a run test instruction is shifted into the instruction register, and the test begins when the TAP controller enters its RT/IDLE state. During the test, the output patterns are applied from an IC's output boundary register on the falling edge of TCK to drive the combinational logic. The output response from the combinational logic is input to the IC's input boundary register, where it is sampled into the PSA register on the rising edge of TCK. When the test is complete, the TAP controller transitions from the RT/IDLE state and shifts a boundary read instruction into the instruction register. The boundary read instruction selects the boundary register to allow the signatures collected to be shifted out for inspection.

Summary

The 1149.1 standard provides a basic framework for boundary testing. A user may take this basic framework and use it as it is or build on top of it the types of test structures and operations required to satisfy particular testing needs. This paper illustrates how an existing architecture can be modified to conform to the 1149.1 architecture. Also, adapting to the new architecture does not require giving up any pre-existing test capabilities. In addition, a boundary BIST approach was described and compared to a purely scan-operated boundary test approach. This comparison shows the benefits of a boundary BIST approach to be a significant reduction in the time to test combinational logic residing between the boundaries of ICs in a circuit.

Acknowledgment

The author of this document is Lee Whetsel.

References

1 *Joint Test Action Group Specification,* Version 2.0. (Available from the author.)

2 *IEEE P1149.1, Draft 3, Proposal Specification.* (For information on obtaining a copy, contact the author.)

3 C. Maunder and F. Beenker. *Boundary Scan: A Framework for Structured Design-for-Test,* Proceedings IEEE International Test Conference, 1987, pp. 714–723.

4 F. Beenker. *Systematic and Structured Methods for Digital Board Testing,* Proceedings IEEE International Test Conference, 1985, pp. 380–385.

5 M.M. Pradham, R.E. Tulloss, F.P.M. Beenker, and H. Bleeker. Developing a Standard for Boundary Scan Implementation, Proceedings International Conference on Computer Design, 1987, pp. 462–466.

6 L. Whetsel. *A Proposed Standard Test Bus and Boundary Scan Architecture,* Proceedings International Conference on Computer Design, 1988, pp. 330–333.

Design Tradeoffs When Implementing IEEE 1149.1

SCTA045A
January 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	Page
Introduction	**7–117**
Test Considerations – Ad Hoc/Structured	**7–117**
What is IEEE 1149.1?	**7–117**
Overview	**7–118**
Design Costs Versus Test Costs	7–118
Use of Scannable Parts	**7–118**
Design Tradeoffs in Implementing IEEE 1149.1 IC Level	**7–119**
Controllability and Observability	7–119
BIST/Additional Hooks	7–119
IC Pins/Package Size	7–120
Gate Count	7–120
Propagation Delay	7–122
Reliability	7–122
Power	7–122
Test Costs	7–122
IC Costs	7–123
PWB Design	**7–123**
Partitioning	7–123
Real Estate	7–124
Test Points/Connector Size	7–124
Reliability	7–125
Test Costs	7–125
System Test	**7–125**
PWB-to-PWB Interfaces	7–125
Test-Bus Controllers (TBC)	7–126
Conclusion	**7–126**
Acknowledgment	**7–126**

List of Illustrations

Figure	Title	Page
1	IEEE 1149.1 Scan-Bus and Boundary-Scan Architecture	7–118
2	IEEE 1149.1 Pins-In and Pins-Out Testing Via Boundary Scan	7–119
3	Standard-Cell ASIC 1149.1 Overhead	7–121
4	Gate-Array ASIC 1149.1 Overhead	7–121
5	Simple Processor PWB Design	7–123
6	Design Partition Via Boundary Scan	7–124
7	Virtual Test Points Via IEEE 1149.1 Boundary Scan	7–124
8	IEEE 1149.1 TBCs	7–126

SCOPE is a trademark of Texas Instruments Incorporated.

Introduction

This paper explores the many design tradeoffs that occur when implementing the IEEE 1149.1 test bus in integrated circuits (IC), printed wiring boards (PWB), and systems. As with any design task, tradeoffs must be made to achieve the best mix of functionality, testability, reliability, producibility, and maintainability. As an industry-wide standard, the IEEE 1149.1 test bus and boundary-scan architecture allows a consistent method for circuit controllability and observability across all levels of development and test. Test and debug operations can be performed via the IEEE 1149.1 test bus and boundary-scan architecture in many areas including design verification, fault troubleshooting, factory board and system test, and field test without requiring actual physical access. Embedded test features, which previously could be accessed only at one test level, can be accessed easily at each level of integration (i.e., IC, board, subsystem, and system).

Test Considerations – Ad Hoc/Structured

There are two fundamental ways to apply testability to a design: ad hoc (or unstructured) and structured. Ad hoc testability is simply intended to solve a particular test problem (i.e., adding a test point to observe a signal line during board test). While this may be useful for a particular test environment, in this case factory board test, it may not be useful for any other test environment, such as IC or system test. Structured testability, on the other hand, is designed to be useful at several levels of test. For instance, an IC with built-in self test (BIST) and a standard test interface can be used for IC test, board test, and system test. This type of testability is considered structured because it is standardized and can be used in several test environments.

What is IEEE 1149.1?

The IEEE 1149.1 test bus and boundary-scan architecture allow an IC, and similarly a board or system, to be controlled via a standard four-wire interface. Each IEEE 1149.1-compliant IC incorporates a feature known as boundary scan that allows each functional pin of the IC to be controlled and observed via the four-wire interface. Test, debug, or initialization patterns can be loaded serially into the appropriate IC(s) via the IEEE 1149.1 test bus. This allows IC, board, or system functions to be observed or controlled without actual physical access.

The IEEE 1149.1 test bus comprises two main elements: a test access port (TAP), which interfaces internal IC logic with the external world via a four-wire (optionally, five-wire) bus; and a boundary-scan architecture, which defines standard boundary cells to drive and receive data at the IC pins. IEEE 1149.1 also defines both mandatory and optional opcodes and test features. The test bus signals are: Test Clock (TCK), Test Mode Select (TMS), Test Data In (TDI), Test Data Out (TDO), and the optional Test Logic Reset (TRST). The IEEE 1149.1 specification also specifies that the ICs can be connected in either a ring or star configuration. A simplified block diagram of the architecture is shown in Figure 1.

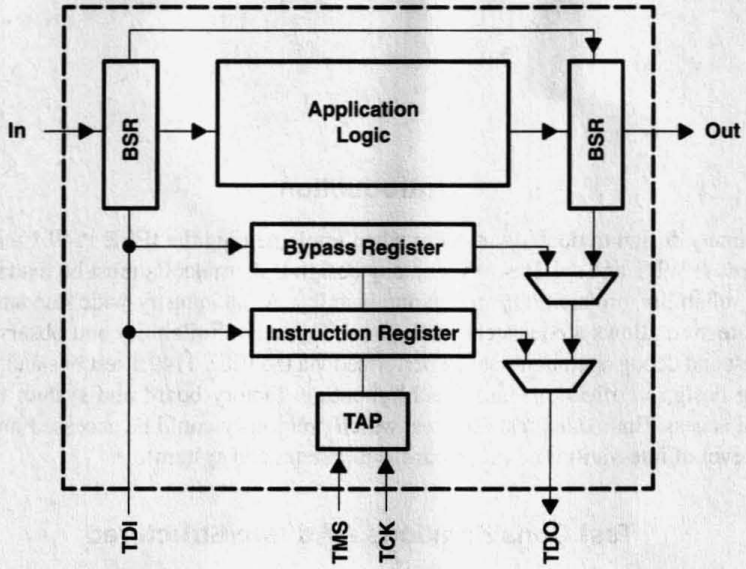


Figure 1. IEEE 1149.1 Scan-Bus and Boundary-Scan Architecture

Overview

Design Costs Versus Test Costs

Cost is a driving requirement when designing any system. Design costs are easily calculated in terms of part costs, manufacturing assembly, engineering design labor, etc. Test costs are also quantifiable but may not be done as easily. Certainly, test equipment and test software development costs can be readily calculated, but test times, troubleshooting, and repair are not as obvious. In complex designs or designs that have long service lives, the life-cycle costs (LCC) of the product are dominated by test and maintenance costs, not design and production costs. It is typical to "invest" time and money to design for test, which then saves production and maintenance costs. To provide an easy and cost-effective method to include IEEE 1149.1 testability into any design, Texas Instruments (TI) has developed a family of testable ICs and Application-Specific Integrated Circuit (ASIC) cells, These ICs and ASIC cells are members of the System Controllability, Observability, and Partitioning Environment (SCOPE™) family.

Use of Scannable Parts

Two complementary techniques are used when designing IEEE 1149.1 into a system: off-the-shelf parts (i.e., TI SCOPE bus-interface products) and ASICs. Each satisfies a particular application, but both can be used together in the same design. TI SCOPE bus-interface products and other off-the-shelf parts are suitable when testability is needed in a functionally equivalent device. Consider a simple PWB with a processor and memory. Without testable SCOPE bus-interface products, the address and data buses would have to be tested indirectly by writing and reading memory via the processor. The embedded address and data buses buffered by '244 and '245 parts can be replaced by functionally-equivalent IEEE 1149.1-compliant TI SCOPE bus-interface products. Now, tests of the address and data buses can be achieved by controlling and observing the SCOPE bus-interface products via the IEEE 1149.1 test bus. Addresses and data can be explicitly loaded and driven by the SCOPE bus-interface products or functionally-driven addresses and data can be captured and read via the IEEE 1149.1 test bus.

The other technique used to incorporate IEEE 1149.1 features into a design is by designing it into ASICs. If ASICs are used, adding IEEE 1149.1 is a straightforward and efficient method of implementing testability into a design.

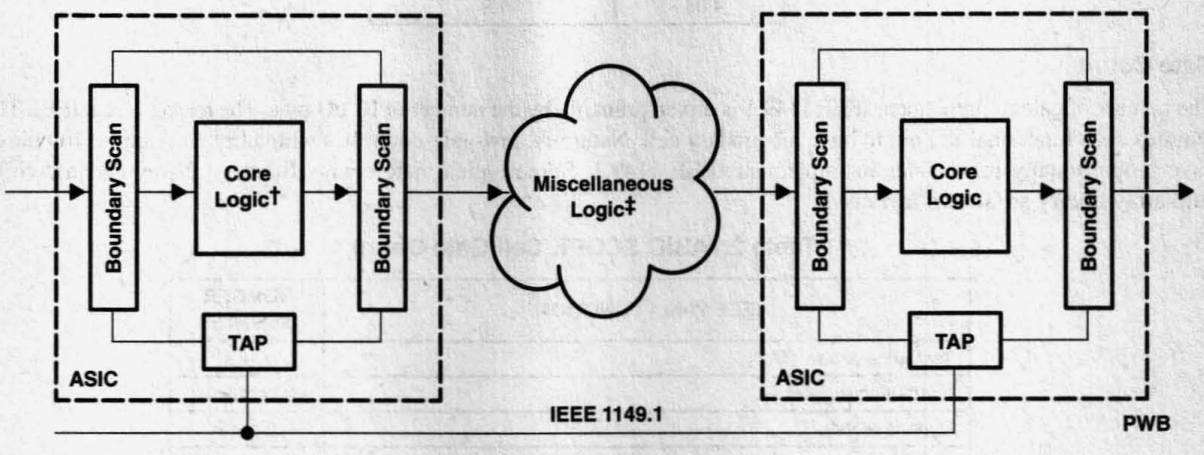
TI also produces several other IEEE 1149.1-compliant test ICs to support PWB and system test. A test-bus controller (TBC) is available to drive the IEEE 1149.1 test bus. Other members of the SCOPE family include scan-path selectors (SPS) to partition long scan paths into multiple small chains and a digital bus monitor (DBM) to monitor and capture data in real time.

Design Tradeoffs in Implementing IEEE 1149.1 IC Level

The following paragraphs present IEEE 1149.1 design tradeoff information at the IC level. While this data is useful in simply comparing IEEE 1149.1 ICs to non-IEEE 1149.1 ICs, this one-to-one comparison is not as useful as comparing the total advantages/disadvantages at the PWB and system levels. Total PWB and system-level tradeoffs, not IC tradeoffs, should be used to determine the final implementation strategy.

Controllability and Observability

Obviously, in addition to performing their functional tasks, the SCOPE family of test products provides a level of controllability and observability that was previously unachievable. During design verification, test, or troubleshooting, signal states may be sampled or controlled via the IEEE 1149.1 interface. Testing can be accomplished on the internal IC logic via pins-in testing, or tests on external IC logic or interconnects via pins-out testing. Pins-in testing is accomplished by loading IC input pins via the IEEE 1149.1 interface, driving the internal logic of the IC, capturing the output pin states, and scanning out the results. Pins-in testing is accomplished by loading IC output pins via the IEEE 1149.1 interface, driving the IC outputs and interconnects, capturing the data at the next IEEE 1149.1 ICs input pins, and scanning out the results. Pins-in and pins-out testing is shown in Figure 2.



† Pins-in testing is accomplished by loading test patterns at IC inputs, driving data across IC logic, and capturing patterns at IC outputs.
‡ Pins-out testing is accomplished by loading/driving test patterns at IC outputs and capturing patterns at the next IC's inputs.

Figure 2. IEEE 1149.1 Pins-In and Pins-Out Testing Via Boundary Scan

BIST/Additional Hooks

In addition to the standard four-wire interface and boundary-scan architecture that IEEE 1149.1 defines, other test or debug "hooks" can be implemented and controlled. For ASICs, it is very common to include some form of BIST to assist in device testing. IEEE 1149.1 provides a standard interface to initiate BIST and retrieve results. Two common BIST methods known as pseudorandom pattern generation (PRPG) and parallel signature analysis (PSA) are supported in the SCOPE bus-interface products and ASIC standard cell libraries. PRPG provides the capability to generate pseudorandom patterns to stimulate a circuit under test. PSA allows a stream of patterns to be collected and compressed into a unique signature. In addition to boundary scan, ASICs and other special-purpose ICs may incorporate internal scan within the IEEE 1149.1 architecture. Internal scan may be used to partition the IC into more easily testable functions, write/read internal registers, etc. TI's later generations of digital signal processors (DSPs) incorporate internal scan to provide built-in in-circuit-emulation features for test and debug. Via the IEEE 1149.1 interface, registers can be loaded/examined and the processor execution can be controlled to RUN/STOP, SINGLE-STEP, etc.

IC Pins/Package Size

The first requirement when implementing IEEE 1149.1 is the addition of four extra pins. This overhead is always required, but is less obvious in larger package devices. Table 1 shows the percent of additional pins per package size.

Table 1. 1149.1 IC Package/Pin Ratio

IC PACKAGE SIZE (NO. OF PINS)	IEEE 1149.1 IC PINS VS TOTAL IC PINS (%)
24	16.7
40	10
64	6.3
100	4
132	3
160	2.5
208	1.9

Gate Count

The number of gates to implement IEEE 1149.1 is driven primarily by the number of IC I/O pins. The reason is that IEEE 1149.1 requires each functional I/O pin to have a boundary cell. Naturally, low-gate-count ICs with a high number of I/O pins will have proportionally more gates to implement IEEE 1149.1. Some typical gate counts from a 1.0-μm standard-cell and gate-array library are shown in Table 2.

Table 2. ASIC SCOPE Cell Gate Count

IEEE 1149.1 FUNCTION	NUMBER OF GATES
Test access port (TAP)	≈183
Instruction register	≈20 gates/bit
Bypass register	≈8 gates
Unidirectional SCOPE boundary cell (hard macro) (standard cell)	≈15 gates/pin
Bidirectional SCOPE boundary cell (standard cell)	≈19 gates/pin
Unidirectional SCOPE boundary cell (soft macro) (standard cell)	≈24 gates/pin

The formula below can be used to estimate the IEEE 1149.1 gate count overhead. (Remember to count only the number of functional I/O pins, not power, ground, or unused pins).

$$\text{Total IEEE 1149.1 gate count} = \text{TAP} + (\text{IR} \times \text{IR bit width}) + \text{BR} + (\text{no. I/O pins} \times \text{no. gates/pin}) \quad (1)$$

Figures 3 and 4 show the relationship between functional gate count versus IEEE 1149.1 test logic versus pin-count increase for both standard-cell and gate-array designs.

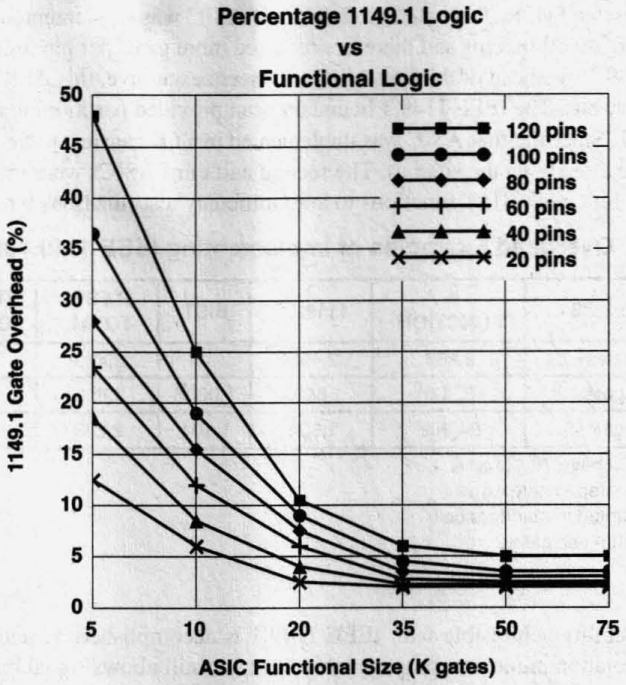


Figure 3. Standard-Cell ASIC 1149.1 Overhead

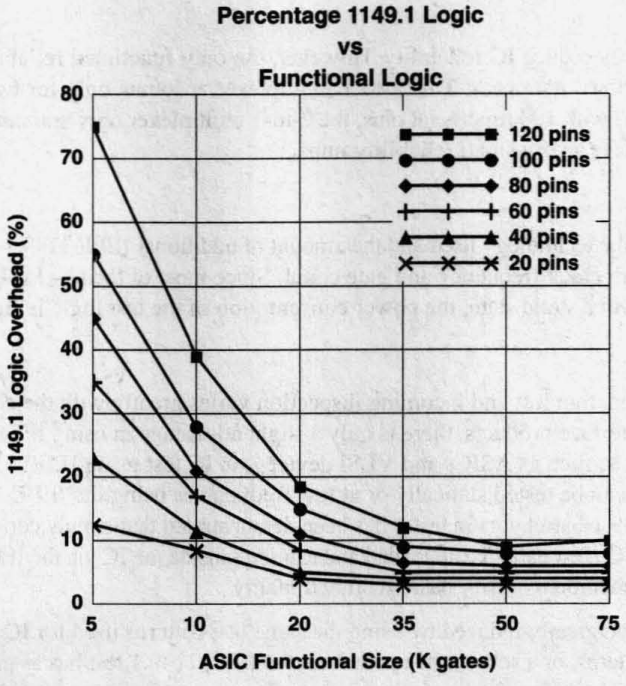


Figure 4. Gate-Array ASIC 1149.1 Overhead

Some actual ASIC examples are shown in Table 3. The first small ASIC was implemented in a gate array. The gate-array boundary cells were constructed as soft macros and therefore required more gates per pin to implement than the SCOPE hard macros. Although the IEEE 1149.1 overhead of the first ASIC may seem excessive, this ASIC acted as a translator and buffer between a processor and memory bus. The IEEE 1149.1 boundary scan provided partitioning and allowed independent testing of the functions via IEEE 1149.1. Since the first ASIC was implemented in a 6K gate array, the gates to implement IEEE 1149.1 were essentially free (they were already on the silicon). The second and third ASICs were implemented as standard-cell hard macros. Also notice that they implement BIST functions to autonomously test functions within the ASICs.

Table 3. Overhead Examples of Implementing IEEE 1149.1 and BIST

ASIC SIZE	IC FUNCTION	1149.1†	BIST	TEST TOTAL	TEST AS % OF TOTAL
4,753 gates‡	2,263	2,490	0	2,490	52.4
20,000 gates§¶	18,350¶	1,650¶	1,000¶	2,650	13.3
87,000 gates§	84,262	1,634	1,104	2,738	3.1

† All ASICs have 70 I/O pins.
‡ Implemented in gate array
§ Implemented in standard cell
¶ Gate count estimated.

Propagation Delay

The controllability and observability achievable with IEEE 1149.1 is accomplished by adding a 2-to-1 multiplexer in the normal data path. This simple solution minimizes propagation delays, yet still allows signal lines to be sampled or driven. The propagation delay of the 2-to-1 multiplexer is dependent on the technology used to implement the device. The propagation delays for a 1.0-µm CMOS ASIC library are approximately 1.0 ns (typical) for a standard-cell hard macro and approximately 1.8 ns (typical) for a gate-array soft macro. Propagation delays will naturally continue to decrease as technology matures.

Reliability

Increased gate count will slightly reduce IC reliability. However, the only functional reliability impact will come from the 2-to-1 multiplexer in the functional data path. This 2-to-1 multiplexer accounts only for two gates per boundary cell. For example, in an 8,000-gate ASIC with 100 functional pins, the 2-to-1 multiplexer only amounts to a 2.5% gate-count increase in the functional data path. This is a very small reliability impact.

Power

Power dissipation is driven by the technology used and the amount of additional IEEE 1149.1 logic. For CMOS technologies, power dissipation increases with clock frequency and gate count. Since most of the test logic (except the 2-to-1 multiplexer in the functional path) remains in a static state, the power consumption of the test logic is small.

Test Costs

The costs of IC test for IC production test and incoming inspection varies greatly with the complexity of the IC. For simple ICs, such as the SCOPE bus-interface products, there is only a slight advantage in using IEEE 1149.1 in an IC-level test. For medium- to high-complexity ICs, such as ASICs and VLSI devices, an IC test using IEEE 1149.1 provides several benefits. First, ASIC and VLSI devices can be tested statically or at low frequencies using the IEEE 1149.1 pins-in and pins-out test methods. Actually, an IEEE 1149.1-based pins-in tester has been demonstrated that simply consists of an IC socket with power, ground, and an IEEE 1149.1 TBC. Test patterns are loaded and captured inside the IC via the IEEE 1149.1 test bus. This method provides a quick, inexpensive method to verify basic IC functionality.

IC test-development costs can be greatly reduced by using the same test patterns used for IC design verification, simulation, and IC tests. The simulation patterns, or a subset, are applied via the IEEE 1149.1 test bus as previously described. The second major benefit of the IEEE 1149.1 test bus is the ability to control and examine internal nodes or states of ASIC and VLSI devices. Hard-to-test functions can be partitioned via internal scan and tested independently with smaller, easier-to-test partitions. An ASIC that may require 2^{20} (1 million) test patterns just to test a 20-bit counter can be tested in a fraction of the patterns by implementing internal scan on the counter. Patterns can be downloaded directly via scan to test any count sequence. A recently developed ASIC with very long counter chains saved over four-million test patterns by implementing internal partitioning controlled via the IEEE 1149.1 test bus.

IC Costs

IC purchase costs with IEEE 1149.1 are higher than their equivalent untestable versions. The cost delta varies, depending on the proportion of IC pins and test logic to functional pins and logic. For larger ASICs, the cost increase is small, but even in small ASIC designs the PWB and system test benefits are realizable. For I/O-limited ASICs (ASICs that have unused core gates), the cost increase is typically less than the proportional gate increase. For core-limited ASICs (ASICs that do not have spare gates), the cost may be proportional to the increase in gates, or possibly higher.

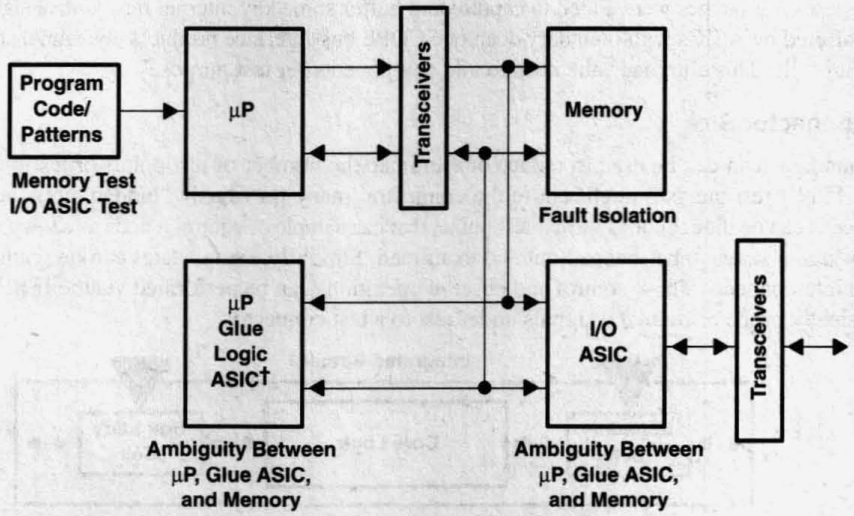
PWB Design

The following paragraphs review PWB-level advantages/disadvantages when implementing designs with the IEEE 1149.1 test bus. PWB test advantages using the IEEE 1149.1 test bus are much more obvious since PWB test problems are more challenging.

Partitioning

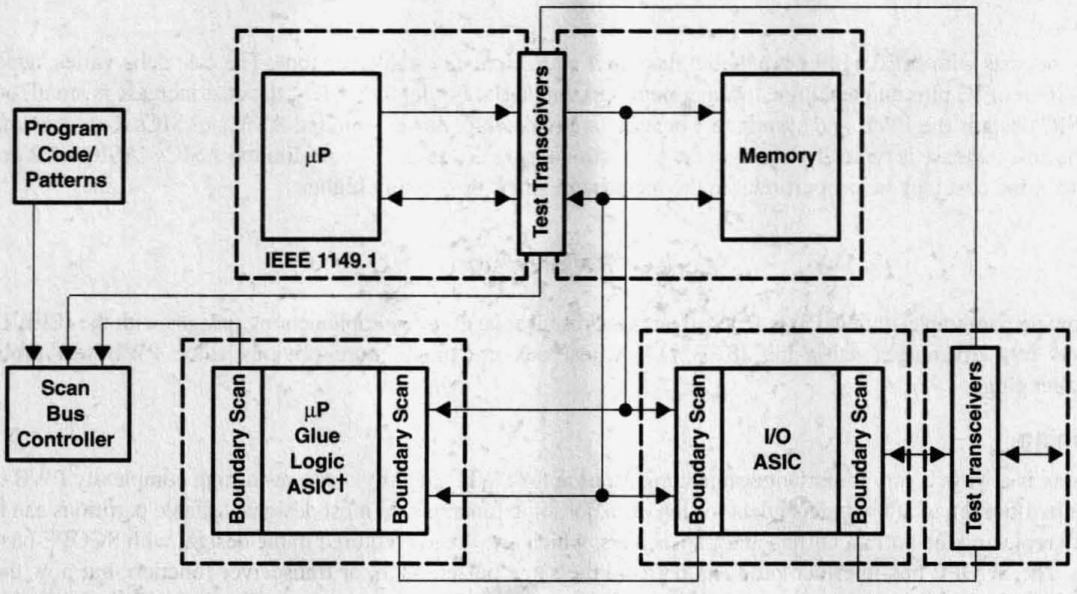
Partitioning is always a very important design consideration for PWB test. Any medium-to-high complexity PWB must have adequate partitioning to allow independent testing of major logic functions. In most designs, testable partitions can be created by simply replacing the normal buffers and transceivers, which are already required in the design, with SCOPE bus-interface products. The SCOPE bus-interface products perform the same buffer, latch, or transceiver function, but now they can be controlled via the IEEE 1149.1 test bus to load or sample signal states during design verification, test, and debug.

For instance, consider the simple microprocessor board design shown in Figure 5. In order to execute test software, the processor, memory, glue-logic ASIC, IC, and PWB interconnects must be fault free. If a fault exists on the memory data bus, the processor will execute bad code and control will be lost. By adding boundary scan in the ASICs and replacing the bus transceivers with SCOPE bus-interface products, as shown in Figure 6, the processor, memory, and ASICs can be tested independently. This reduces the ambiguity group and results in better fault isolation. Repair and replacement savings can be realized by faster troubleshooting and fault isolation to fewer components. By using the partitioning provided by the SCOPE bus-interface products and ASICs with IEEE 1149.1, PWB failures can be detected and isolated with less probing or arbitrary part substitution.



† Memory, decode, I/O decode, etc.

Figure 5. Simple Processor PWB Design



† Memory, decode, I/O decode, etc.

Figure 6. Design Partition Via Boundary Scan

Real Estate

The PWB test-logic real-estate impact can be minimized and, in some cases, PWB real estate can be gained by using IEEE 1149.1 to test functions. PWB real-estate savings can be accomplished by replacing an IC added for test purposes with boundary scan embedded in the IC silicon. Test logic that is added to meet fault detection or fault isolation can be efficiently implemented and controlled via the IEEE 1149.1 test bus.

In a recent design, several latches were added to capture and buffer some key internal bus-control signals for PWB test. If the internal bus is buffered by ASICs with boundary-scan or SCOPE bus-interface products, the signal states can be observed via the boundary-scan cells. This eliminates the need to add components for test purposes.

Test Points/Connector Size

IEEE 1149.1 boundary scan can be used to reduce or eliminate the number of test points or test pins on a PWB. When the four-wire IEEE 1149.1 test bus is brought out to the connector, many previously "hidden" internal nodes become visible. Boundary-scan cells can be thought of as virtual test points that can sample or control a node as shown in Figure 7. These virtual test points allow signal states to be scanned out and examined. Similarly, signal states can be scanned in and driven across circuit logic and interconnects. These control and observe operations can be performed via the IEEE 1149.1 test bus without the need to physically probe or route the signals under test to a test connector.

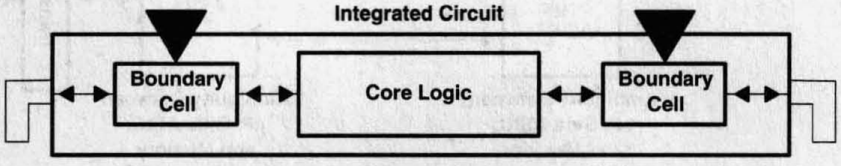


Figure 7. Virtual Test Points Via IEEE 1149.1 Boundary Scan

Two main advantages are obvious when using IEEE 1149.1 boundary scan as virtual test points. The first advantage is that fewer test points are required if critical signals are buffered by SCOPE bus-interface products or ASIC boundary cells. The second advantage is that boundary cells are not subject to the potential noise problems that may be caused by additional etch and pins of test points.

Reliability

PWB reliability usually will not increase significantly by adding IEEE 1149.1 to the design. The small increase in silicon gates may not be notable when compared at the PWB level. In fact, reliability may increase when ad hoc testability is replaced by IEEE 1149.1. Also, remember that the only impact to device functional logic reliability is the addition of the 2-to-1 multiplexer in the data path.

Another key factor to consider along with reliability is system availability. A small decrease in system reliability may not be important if system availability increases. Consider a system with a 200-hour MTBF and a repair time of ten hours. The system will have an availability of 1-10/200 = 95 percent. Now consider a more testable system that has a 195-hour MTBF and a repair time of only five hours. The system will have an availability of 1-5/195 = 97.5 percent.

Test Costs

PWB test costs can vary greatly with the complexity and testability of the design. Even simple designs without adequate testability can cause production slowdowns and cost overruns. Production test costs can account for a significant portion of the final product costs. In some businesses, it is estimated that 25% of the product costs result from test costs. Consider the following PWB-production test scenarios. A PWB has an ambiguity group of three high-cost parts using conventional functional-based test techniques. If the failure can be isolated to one device with boundary scan, savings can be realized because several good parts were saved as well as the labor and time required for unnecessary replacement. In another scenario, an hour of technician's labor, including overhead, is $20/hour, and a PWB test requires 10 minutes per PWB, producing 5,000 PWBs/month. If the added testability of IEEE 1149.1 provides a 20% reduction in PWB test times, the production test savings equal $3340 ($20 × 0.167 × 5,000 × 0.2) per month.

System Test

IEEE 1149.1 can also be used for system-level tests. The increased access afforded by the test and boundary scan allow control and observability in a closed system. Tests that previously required physical access using probe clips or extender boards can be performed via the IEEE 1149.1 bus. This reduces faults caused by the additional loading of test probes, electromagnetic interference, and manually-inducted removal and replacement.

PWB-to-PWB Interfaces

Extending the IEEE 1149.1 bus between PWBs can be accomplished by two basic methods: ring and star. The ring configuration allows a simple method to extend the PWB-level scan ring. However, this method has several drawbacks; the scan bus may become very long, which can slow test throughput, and a single-point failure caused by a broken connection or missing PWB will break the scan ring. The ring configuration from PWB-to-PWB interfacing is most practical for a small number of PWBs, typically four or less.

An IEEE 1149.1 star configuration between PWBs allows each PWB scan ring to be addressed without the overhead of additional PWBs in the scan path. However, this method requires additional backplane signals and allows only one PWB at a time to be addressed. Multiple PWBs cannot be scanned simultaneously with a star configuration.

There are several methods to efficiently partition scan rings from PWB to PWB. The simplest solution is to use the 'ACT8997 scan-path linkers or 'ACT8999 scan-path selectors to partition PWB scan rings. These devices allow a complete PWB scan ring to act as one device in bypass mode. This shortens a PWB scan ring to just one bit in the scan path. For more information on using scan-path selectors, see the article *Partitioning Designs With 1149.1 Scan Capabilities*.

Test-Bus Controllers (TBC)

Control of the IEEE 1149.1 test bus for system test can be accomplished via either an external TBC or via an internal embedded TBC. Figure 8 shows an example system with internal and external TBCs. For factory- or maintenance-type testing, a single external TBC will suffice as the IEEE 1149.1 master. Naturally, in this configuration, scan-based test can be performed only under external control.

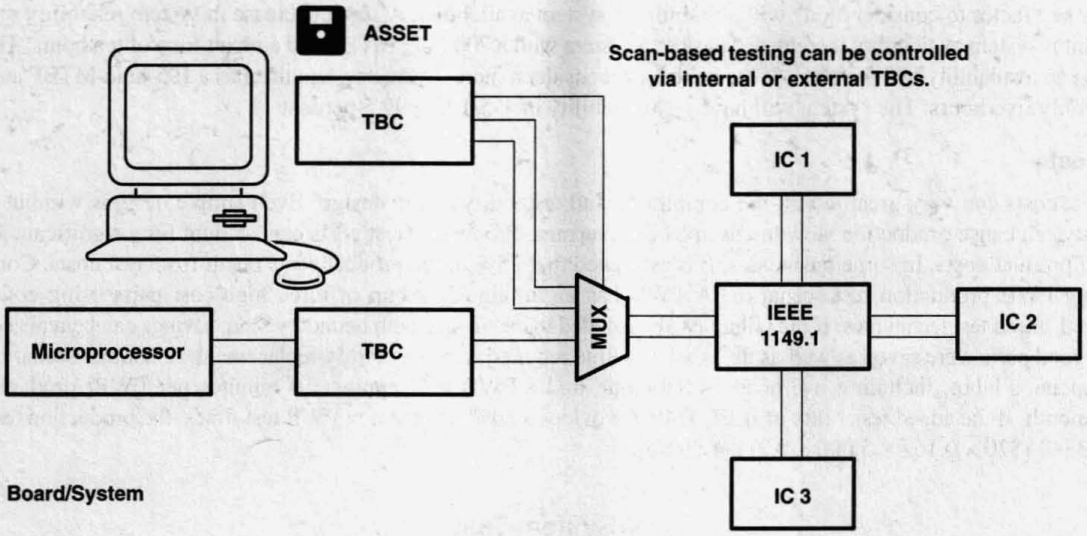


Figure 8. IEEE 1149.1 TBCs

The other option, an embedded TBC, allows autonomous testing under control of the embedded TBC. For small systems (less than four boards), a single TBC may be sufficient to test the system quickly. For larger or more complex systems, multiple TBCs may be required to test the system within an allocated time limit. The actual implementation method depends on the requirements for test execution time, real-estate limits, and fault tolerance.

Conclusion

Considering all the advantages that a standard test-bus and boundary-scan architecture provides, IEEE 1149.1 should be seriously considered as a test solution. While the capabilities gained are not free, the tradeoffs should be investigated. Advantages include increased controllability and observability, test reuse, better fault detection and isolation, and consistent test methods across multiple test environments. Impacts include cost, propagation delay of one 2-to-1 multiplexer in the signal path, and increased gate count for test logic. Although IEEE 1149.1 is suitable for all logic design sizes, implementing IEEE 1149.1 typically is easier to justify on larger designs. In the tradeoff analysis consider hidden costs such as fault-isolation size, test-development time, test-execution time, repair time, and life-cycle repair and maintenance cost. These costs should not be underestimated. Using the capabilities of the IEEE 1149.1, test bus and boundary scan provide advantages that help reduce the total cost of ownership.

Acknowledgment

The original author of this paper is Wayne Daniel.

Impact of JTAG/1149.1 Testability on Reliability

SCTA041A
January 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	Page
Introduction	**7–131**
JTAG/1149.1 Overview	**7–131**
Testability Design Tradeoffs	**7–131**
Memory-Board Example	**7–132**
Baseline Memory-Board Design	**7–134**
Ad Hoc Testability Memory Board	**7–135**
1149.1-Compliant Memory Board	**7–136**
Analysis of Results	**7–137**
Conclusion	**7–138**
Acknowledgment	**7–138**
References	**7–138**

List of Illustrations

Figure	Title	Page
1	No-Testability Baseline Design	7–132
2	Ad Hoc Testability Design	7–133
3	1149.1 Testability Design	7–133

List of Tables

Table	Title	Page
1	Feature Comparison for Standard Octal and SCOPE Testability Octal Parts	7–132
2	Baseline Memory Parts List With Failure Rates	7–134
3	Baseline Memory-Board Test Flow and Fault-Isolation Ambiguity Groupings	7–135
4	Ad Hoc Memory-Board Parts List With Failure Rates	7–135
5	Ad Hoc Memory-Board Test Flow and Fault-Isolation Ambiguity Groupings	7–136
6	1149.1-Compliant Memory-Board Parts List With Failure Rates	7–136
7	1149.1-Compliant Memory-Board Test Flow and Fault-Isolation Ambiguity Groupings	7–137
8	Reliability Comparisons	7–137
9	Percentage Added Because of Testability Circuit	7–137

Introduction

Increasingly aggressive testability requirements on modern electronics development programs are being imposed by the industry. These requirements usually increase the size of the hardware design. Traditionally, the addition of hardware for testability functions such as readback, pattern generation, pattern insertion, and functional hardware test control is known as ad hoc testability. In general, testability hardware can increase design factors such as part count, connector pins, board "real estate," cost, and power.

JTAG/1149.1 Overview

Advances in testability methodology have led to the development of bus-based observability and controllability systems instead of the traditional ad hoc methods. One of these bus-based systems was proposed by the Joint Test Action Group (JTAG). The specification developed by JTAG evolved into IEEE Std 1149.1 (1149.1)[1] for a four-wire test-bus interface and boundary-scan architecture. Boundary scan is a specialized scan path that provides observability and controllability to device or board input/output pins. The 1149.1 architecture is designed to improve a circuit's fault detection and isolation capabilities. Products such as test-bus transceivers have been developed to incorporate the boundary-scan protocols.

Testability Design Tradeoffs

Testability can impact related design-support disciplines such as reliability, maintainability, or predictability. The addition of testability circuitry can reduce test costs and time, improving the ease and accuracy of fault detection and isolation. Testability can improve maintainability calculations for mean time to repair (MTTR) by decreasing the test isolation time but can impact the reliability calculation for mean time between failure (MTBF) negatively by increasing the failure rate.

The ad hoc testability approach typically adds 10 to 15 percent extra hardware to the functional design. The Texas Instruments (TI) approach to the application of 1149.1 is to place testability features into already required functional parts.

TI offers specialized test buffers, latches, transceivers, and registers that conform to 1149.1. The bus-interface products offered by TI also incorporate additional testability features such as Parallel Signature Analysis (PSA) and Pseudo-Random Pattern Generation (PRPG) (see Table 1).

Comparing products compliant to 1149.1, a System Controlability and Observability Partitioning Environment (SCOPE) test octal to a standard article, the test octal has approximately 800 gates compared to fewer than 100 gates in a standard octal. The majority of the additional gate count in the scan parts is not in the functional path but in the scan-path control logic. The addition of boundary scan to a buffer places only two gates in each functional signal path. Only 16 gates are added to the normal operational mode. A failure in the scan-path logic does not affect the chip's normal function in most cases. A failure in the scan-path control and scan logic can be isolated by using the inherent parallelism of the boundary-scan logic. The extra gate count impacts the chip-level failure rate, but the benefits for board- and system-level testing can justify the increased failure rate.

Table 1. Feature Comparison for Standard Octal and SCOPE Testability Octal Parts

FEATURES	STANDARD OCTAL PARTS	TESTABILITY OCTAL PARTS
Pin count	20	24
Gate count	< 100	~800
Failure rate: at 0°C at 60°C	 0.0401 0.1500	 0.0563 0.2762
Normal functions	Buffer, latch, transceiver, register	Buffer, latch, transceiver, register
Internal test functions for testing of other parts	None	Signature analysis Pseudorandom pattern generation Boundary scan Readback and latch (245) 1/0 toggle mode
External test purposes	Readback latch control register	Readback latch Control register Pattern generator

Memory-Board Example

This paper illustrates the impact of 1149.1 on reliability using a basic memory-board example. The memory-board example was selected because it is a common design architecture, and because it requires additional testability for fault detection and isolation. To fully illustrate the design tradeoffs involved, the memory board is implemented in the following three different configurations:

- No-testability baseline design (see Figure 1)
- Ad hoc testability design (see Figure 2)
- 1149.1 testability design (see Figure 3)

Each of these three designs has different trade-offs for reliability, testability, and other design considerations.

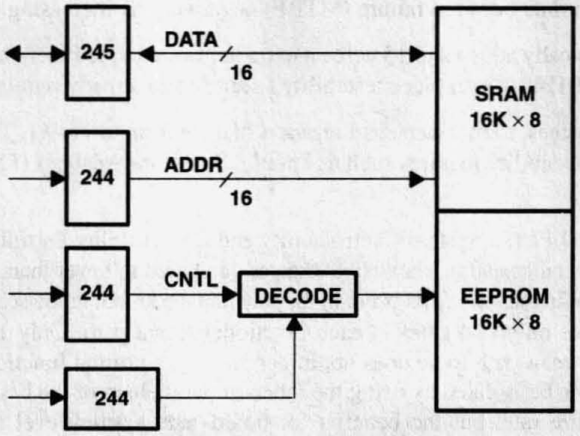


Figure 1. No-Testability Baseline Design

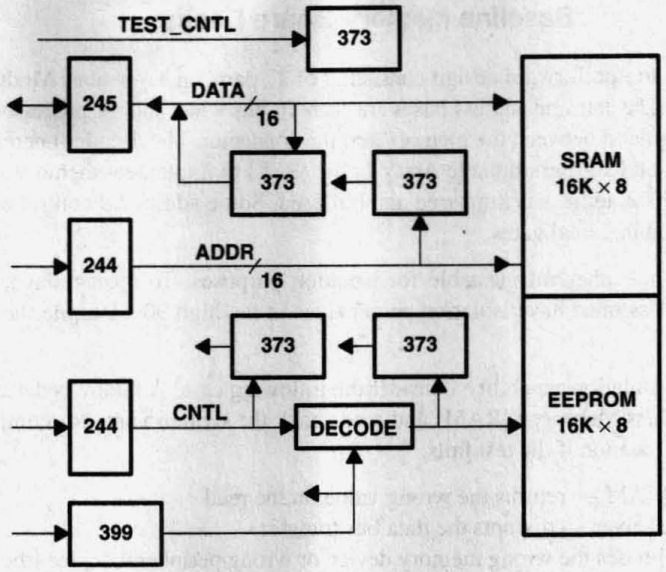


Figure 2. Ad Hoc Testability Design

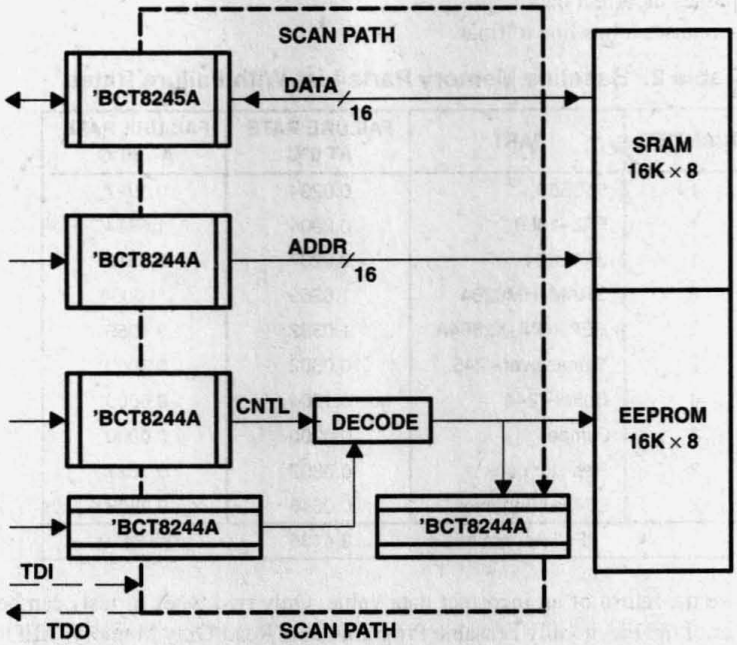


Figure 3. 1149.1 Testability Design

Baseline Memory-Board Design

The baseline memory board is a straightforward design consisting of 17 parts on a Versabus Modular European (VME) type board (see Figure 1 and Table 2). The data and address buses are each 16-bits wide, and the processor control bus is 8-bits wide. These buses are pulled up and buffered between the memory and the connector. The decode function consists of a comparator for the board base address select and a Programmable Array Logic (PAL) to implement memory select, address decode, and read/write control. The board's base address is jumpered and buffered. Some additional control logic (such as write-protect enable) is implemented with combinational gates.

The baseline memory board is not inherently testable for isolation purposes. To meet today's requirements, component ambiguity groupings of four or less must have isolation percentages in the high 90s. Despite the simplicity of the board, it cannot meet these requirements.

For an example of the poor fault-isolation capability, consider the following case. A failure is detected by a test sequence that writes to the Static Random-Access Memory (SRAM) and reads back the written value for comparison. The following are possible candidates for the fault location if the test fails.

- A stuck-at bit in the SRAM — returns the wrong value on the read
- The bidirectional transceiver — disrupts the data bus transfer
- The decode logic — chooses the wrong memory device or wrong peripheral device [the identification (ID) buffer]
- The address decode — chooses the wrong memory location
- The control logic — chooses wrong memory action (read versus write)
- Identification jumper/buffer — chooses the wrong board in the system or maps memory incorrectly
- The connector — passes incorrect data
- The resistor pack — causes a bus line to float

Table 2. Baseline Memory Parts List With Failure Rates

QUANTITY	PART	FAILURE RATE AT 0°C	FAILURE RATE AT 60°C
1	54LS85	0.0294	0.0997
1	PAL–16L8	0.2904	1.6314
1	54ALS04	0.0237	0.0519
2	SRAM–HM6264	1.6259	23.6086
2	EEPROM–X2864A	1.0582	9.4955
2	Transceiver–'245	0.0802	0.3000
4	Buffer–'244	0.1604	0.6000
1	Jumper	0.0000	0.0000
2	Resistor pack	0.0807	0.7631
2	96-pin connector	0.0646	0.2908
	Failure-rate totals:	3.4135	36.8410

Any of these failures can cause the return of an incorrect data value. Only two types of tests can be run on this board: an end-to-end test of the SRAM or of the Electrically Erasable Programmable Read-Only Memory (EEPROM). An intermediate test cannot be performed to reduce the ambiguity groupings. All testing requires a memory storage and retrieval to detect a fault. The ambiguity for most faults is most of the board (see Table 3).

To reduce the ambiguity requires long, complicated testing algorithms that run specific pattern sequences through the memory space to characterize the fault. This only can reduce the ambiguity in some cases and results in long test times because of extended pattern generation.

Table 3. Baseline Memory-Board Test Flow and Fault-Isolation Ambiguity Groupings

BASELINE TEST FLOW	AMBIGUITY GROUPINGS
SRAM tests	17 — Connector, pullups, buffer, comparator, PAL, SRAM, EEPROM, ID buffer, jumpers, transceiver, NANDs
EEPROM tests	17 — Connector, pullups, buffer, comparator, PAL, SRAM, EEPROM, ID buffer, jumpers, transceiver, NANDs

Ad Hoc Testability Memory Board

The ad hoc version of the memory board is derived from the baseline board by placing readback latches on the data, address, and control buses; by replacing the ID buffer with a 4-bit multiplexer/latch; and by placing a test-control register on the board (see Figure 2 and Table 4). The design contains the minimum testability required to bring the ambiguity groupings to four components or less. The testability improvement results in adding seven parts to the board and replacing another.

Table 4. Ad Hoc Memory-Board Parts List With Failure Rates

QUANTITY	PART	FAILURE RATE AT 0°C	FAILURE RATE AT 60°C
1	54LS85	0.0294	0.0997
1	PAL–16L8	0.2904	1.6314
1	54ALS04	0.0237	0.0519
2	SRAM–HM6264	1.6259	23.6086
2	EEPROM–X2864A	1.0582	9.4955
2	Transceiver–'245	0.0802	0.3000
3†	Buffer–'244	0.1604	0.6000
1	Jumper	0.0000	0.0000
2	Resistor pack	0.0807	0.7631
1†	Multiplexer latch	0.0564	0.1267
7†	Octal D-register	0.2807	1.0500
2	96-pin connector	0.0646	0.2908
†	>60 extra pins used		
	Failure-rate totals:	3.7105	37.8677

† Differences from the baseline memory board

The ad hoc testability simplifies the isolation of a detected fault. Table 5 identifies a specific test sequence that will result in the minimum ambiguity groupings.

The first test should be to write a base address to the ID latch through the added multiplexer. This allows the tester to test all memory boards identically, regardless of the jumpered address. Next, all buses should be written to and read back by the '373 latches. This intermediate test allows faults on the connectors, buffers, and transceiver to be isolated. The next test should ensure that the decode function selects the correct memory and addresses. Finally, the memory is tested.

By partitioning the test as shown in Table 5, the fault can be isolated by a divide-and-conquer approach. The benefits are fewer patterns, faster test time, and a higher confidence of isolating a fault. The cost is seven added parts and the related design penalties.

Table 5. Ad Hoc Memory-Board Test Flow and Fault-Isolation Ambiguity Groupings

AD HOC TEST FLOW	AMBIGUITY GROUPINGS
ID overwrite	1 — Latched multiplexer
Pattern data	4 — Connector, buffer, latch, pullup
Pattern address	4 — Connector, latch, transceiver, pullup
Pattern control	4 — Connector, buffer, latch, pullup
Pattern decode	2 — Comparator, PAL
SRAM tests	3 — SRAMs, NANDs
EEPROM tests	3 — EEPROMs, NANDs

1149.1-Compliant Memory Board

In this case, scannable buffers and transceivers replaced the original buffers and transceiver (see Figure 3 and Table 6). One additional part provides observability and controllability on the memory side of the decode block. Then, the SCOPE octal parts were connected into a single scan path.

Table 6. 1149.1-Compliant Memory-Board Parts List With Failure Rates

QUANTITY	PART	FAILURE RATE AT 0°C	FAILURE RATE AT 60°C
1	54LS85	0.0294	0.0997
1	PAL–16L8	0.2904	1.6314
1	54ALS04	0.0237	0.0519
2	SRAM–HM6264	1.6259	23.6086
2	EEPROM–X2864A	1.0582	9.4955
2†	Test transceiver–'BCT8245A	0.1126	0.2762
5†	Test buffer–'BCT8244A	0.2815	1.3810
1	Jumper	0.0000	0.0000
2	Resistor pack	0.0807	0.7631
2	96-pin connector	0.0646	0.2908
†	Four extra pins used		
	Failure-rate totals:	3.5670	37.8744

† Differences from the baseline memory board

The 1149.1-compliant board is more inherently testable than the ad hoc board since the boundary scan allows the insertion and overwrite of signals on the device output pins. The ID jumpers can be reconfigured without using a discrete multiplexer. The scan path allows patterns to be read back between the buffer and the connector. This removes the connector from the ambiguity group. By inserting the patterns through the scan path and following the same test sequence as the ad hoc board, the isolation percentages are improved. No ambiguity group has more than two components (see Table 7).

Table 7. 1149.1-Compliant Memory-Board Test Flow and Fault-Isolation Ambiguity Groupings

1149.1 TEST FLOW	AMBIGUITY GROUPINGS
Scan path	1 — Each test part
ID overwrite	1 — ID register
Pattern connector	1 — Connector
Pattern data	2 — Test buffer pullup
Pattern address	2 — Test transceiver, pullup
Pattern control	2 — Test buffer, pullup
Pattern decode	2 — Comparator, PAL
SRAM tests	3 — SRAMs, NANDs
EEPROM tests	3 — EEPROMs, NANDs

An additional advantage of the scan-path method is that the memories do not have to be tested last in the sequence. The generated patterns and control of the memory can be done via the scan path directly, without having to use the decode logic. This allows isolation without the restriction of a specific test sequence. The test sequence can be redesigned to a failure-rate priority that would have a probability of finding a fault earlier in the test sequence.

The overall advantages of using the SCOPE octal parts versus an ad hoc solution is a reduction in board space and the ability to modify the test sequence.

Analysis of Results

The failure-rate analysis was conducted in accordance with MIL-HDBK-217E.[2] Each of the three boards described above was analyzed using a ground mobile model at 0°C ambient (with an equivalent junction temperature of 50°C) and at 60°C ambient (with an equivalent junction temperature of 110°C). The devices were modeled as full MIL-qualified parts. To keep the comparison similar, all the added parts involved were bipolar complementary metal-oxide semiconductor (BiCMOS) process.

The overall reliability comparison figures for the three boards are shown in Table 8.

Table 8. Reliability Comparisons

RELIABILITY COMPARISON	BASELINE BOARD	AD HOC BOARD	1149.1 BOARD
Failure rate at 0.0°C at 60.0°C	 3.4135 36.8410	 3.7105 37.8677	 3.5670 37.8744
Mission failure (FM) f/mh	20.1273	20.7891	20.7207
MTBF hours	49,700	48,100	48,300

The percentage of test circuitry added to the baseline board is shown in Table 9.

Table 9. Percentage Added Because of Testability Circuit

IMPACT OF TESTABILITY	AD HOC BOARD (%)	1149.1 BOARD (%)
Part count	41.17	5.88
Failure rate at 0.0°C at 60.0°C	 8.70 2.79	 4.45 2.80

Conclusion

The memory-board examples analyzed above are a single, small test case. Therefore, the testability modifications have a greater impact on reliability than when used on more realistic designs.

As shown in Table 8, the ad hoc solution has a higher failure rate at low temperature where the predominant failure mode is the interconnect. The 1149.1 solution has a slightly higher failure rate at the high temperature where the predominant failure mode is the silicon process. These results are expected since the ad hoc solution adds parts to the board and the 1149.1 solution adds gates to the parts.

From a reliability point of view, the ad hoc and 1149.1 solutions have similar impacts on board failure rate (see Table 9). For this example, 1149.1 has an improved overall numerical impact. In terms of percentage of failure rate added to the board, the 1149.1 actually has the least maximum impact with 4.45 percent additional failure rate versus the ad hoc maximum of 8.70 percent.

The 1149.1-compliant board surpassed the isolation requirement of four components with no ambiguity group larger than two (see Table 7), whereas the ad hoc board just met the requirement (see Table 5).

If the ad hoc board were implemented with all of the testability functionality contained within the test octals, the part count would increase significantly. The ad hoc board failure rate would then surpass the 1149.1 solution significantly.

Another advantage the 1149.1 solution has over the ad hoc solution is the number of test points required. The 1149.1 requires only four connector pins to be added. In this case, the ad hoc solution required more than 60 test points at the connector.

The 1149.1 solutions, as compared to ad hoc testability solutions, offer the following advantages:

- Improved observability and controllability
- Improved fault detection and isolation
- Improved reliability
- Fewer test points
- Reduced part count
- Reduced pattern sets
- More flexible test-flow structure
- Lower power consumption
- Better thermal profile

Acknowledgment

The authors, Alfred L. Crouch and Carol Pyron, recognize the contributions and assistance provided by Bill Grimes and Bill Waite of Texas Instruments Incorporated.

References

1 IEEE Std 1149.1–1990, *IEEE Standard Test Access Port and Boundary-Scan Architecture.*

2 MIL-HDBK-217E. *Reliability Prediction for Electronic Equipment.*

System Testability Using Standard Logic

SCTA037A
October 1996
Reprinted with permission of IEEE

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	Page
Introduction	**7–143**
IEEE 1149.1	**7–143**
An Overview of SCOPE/Boundary Scan	**7–143**
SCOPE Bus-Interface Products	**7–144**
Using SCOPE Bus-Interface Products to Improve Testability	**7–148**
Verifying Wiring Interconnects	**7–148**
Logic Verification	**7–149**
System Partitioning	**7–151**
Summary	**7–153**
References	**7–153**
Acknowledgment	**7–153**

List of Illustrations

Figure	Title	Page
1	SN74BCT8244A Block Diagram	7–144
2	TAP-Controller State Diagram	7–145
3	SCOPE Bus-Interface Product Pinouts	7–147
4	Simple Two-Device Scan Path	7–147
5	PRPG and PSA	7–149
6	PSA/PRPG Algorithm of the 'BCT8244A	7–150
7	Partitioning a Shared-Memory Configuration	7–152

SCOPE is a trademark of Texas Instruments Incorporated.

Introduction

The use of more sophisticated ASICs and microprocessors and a steadily increasing move toward surface-mount packaging has led to the increasing complexity and density of digital systems. These advances improve system performance and decrease the physical size of printed-circuit boards (PCBs) but complicate the task of system testing. Access to test nodes using bed-of-nails testing is reduced or eliminated, and the modern automated test equipment necessary to fully exercise complex chips can be prohibitively expensive. One way of circumventing these problems is to use a boundary-scan test method, which can control and observe any node in a system through a dedicated test bus. An IEEE standard currently under development defines a four-wire test bus and protocol that implements a boundary-scan methodology. Standard logic functions, called System Controllability, Observability, and Partitioning Environment (SCOPE™) bus-interface products that incorporate this four-wire bus can be strategically placed in a digital system design. These products greatly enhance overall testability in areas from design and prototype debug to final test and field service of production systems. This paper presents some examples that illustrate the expanded test capabilities available in the earlier bus-interface products – the SCOPE test octals.

IEEE 1149.1

An IEEE 1149.1 document defines a four-wire boundary-scan test protocol that can be implemented in any digital integrated circuit (IC) (see Reference 1 for details of the boundary-scan methodology). Chips designed to comply with this protocol can be interconnected to form one or more serial shift register chains, or scan paths, within a system. Texas Instruments (TI) has designed four octal ICs that adhere to the IEEE 1149.1 protocol. These include many additional capabilities that increase their effectiveness in board, subsystem, or system test.

An Overview of SCOPE/Boundary Scan

Boundary scan is a design-for-testability method that allows signals to be captured and/or forced at the I/O pins of a digital device. All test data is serially shifted from the test data input (TDI) to the test data output (TDO) through some register in the device specifically designated for boundary-scan operations. The current instruction defines which of the registers in the device are connected between the TDI and TDO. Only one register at a time may be connected and accessed.

A primary advantage of boundary-scan testing is that the only physical access required is the four-wire test bus. Through this test bus, the user can access any testable node or signal in the system. The boundary-scan method has built-in safeguards to make it relatively fault tolerant. The test protocol allows for a hierarchical approach to test in which the system is subdivided into standalone subsystems that are convenient for the design and test engineers to use.

SCOPE Bus-Interface Products

A block diagram for a SCOPE bus-interface product, the SN74BCT8244A, is shown in Figure 1. The device is operated in two modes, normal and test. In the normal mode, the '8244A functions identically to an SN74F244, an eight-wide noninverting buffer. In the test mode, additional circuitry is activated to perform a specified test operation.

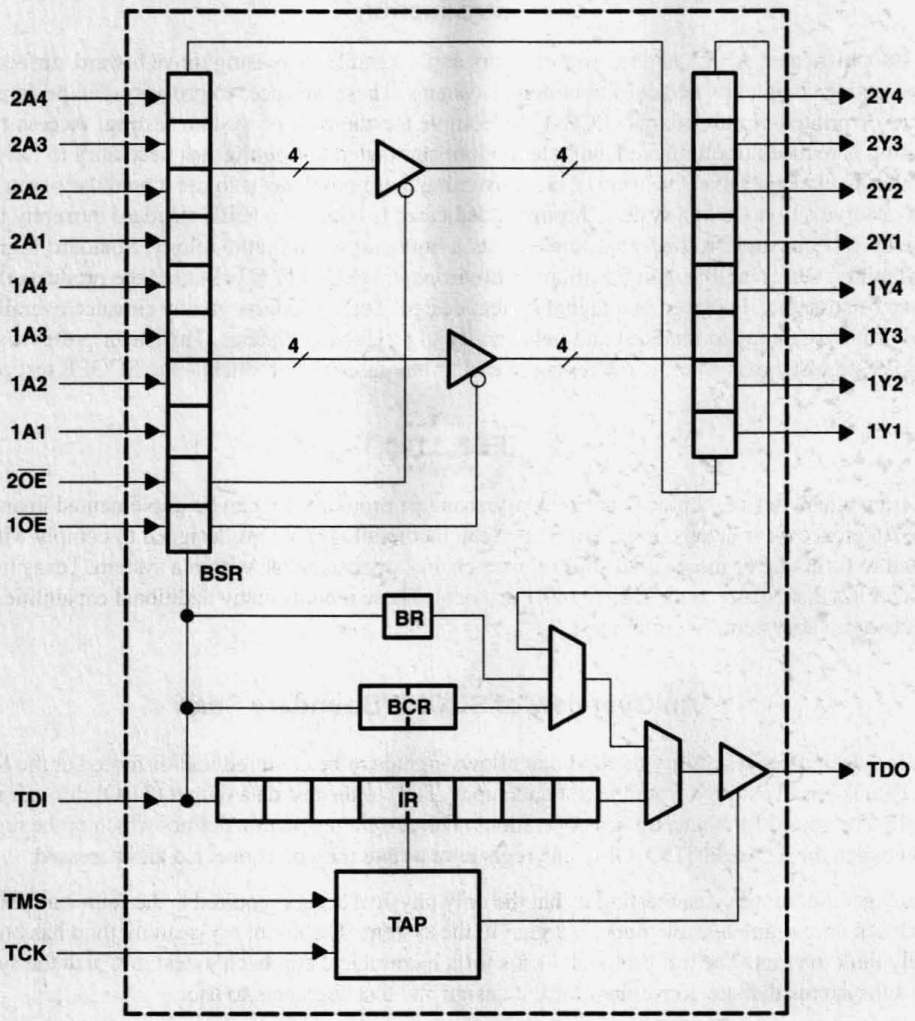


Figure 1. SN74BCT8244A Block Diagram

Figure 1 shows that the chip contains four serial registers, with each square block representing one bit of the register. One register is the 8-bit instruction register (IR), which determines the test operation to be performed. The other three are data registers used to capture, load, and shift the serial test information. The 18-bit boundary-scan register (BSR) contains one boundary-scan cell (BSC) for each functional input and output on the device. The 2-bit boundary-control register (BCR) is an indirect instruction register that is used to implement special test operations that are not part of the standard SCOPE instruction set. The 1-bit bypass register (BR) effectively removes the device from the scan path by providing a short (one clock cycle) delay through the chip. Operation of the test circuitry is synchronous to the test clock (TCK). The 'BCT8244A advances through its state machine (see Figure 2) according to the value of the test mode select (TMS) pin at each TCK rising edge. Inputs are captured on the rising edge of TCK, and outputs change on the falling edge of TCK. Control instructions are issued by the test access port (TAP). The TDI and TDO pins are the serial test data input and output pins, respectively. By connecting the TDO pin of one device to the TDI pin of the next device in the scan path, a serial chain is formed through which all information is passed.

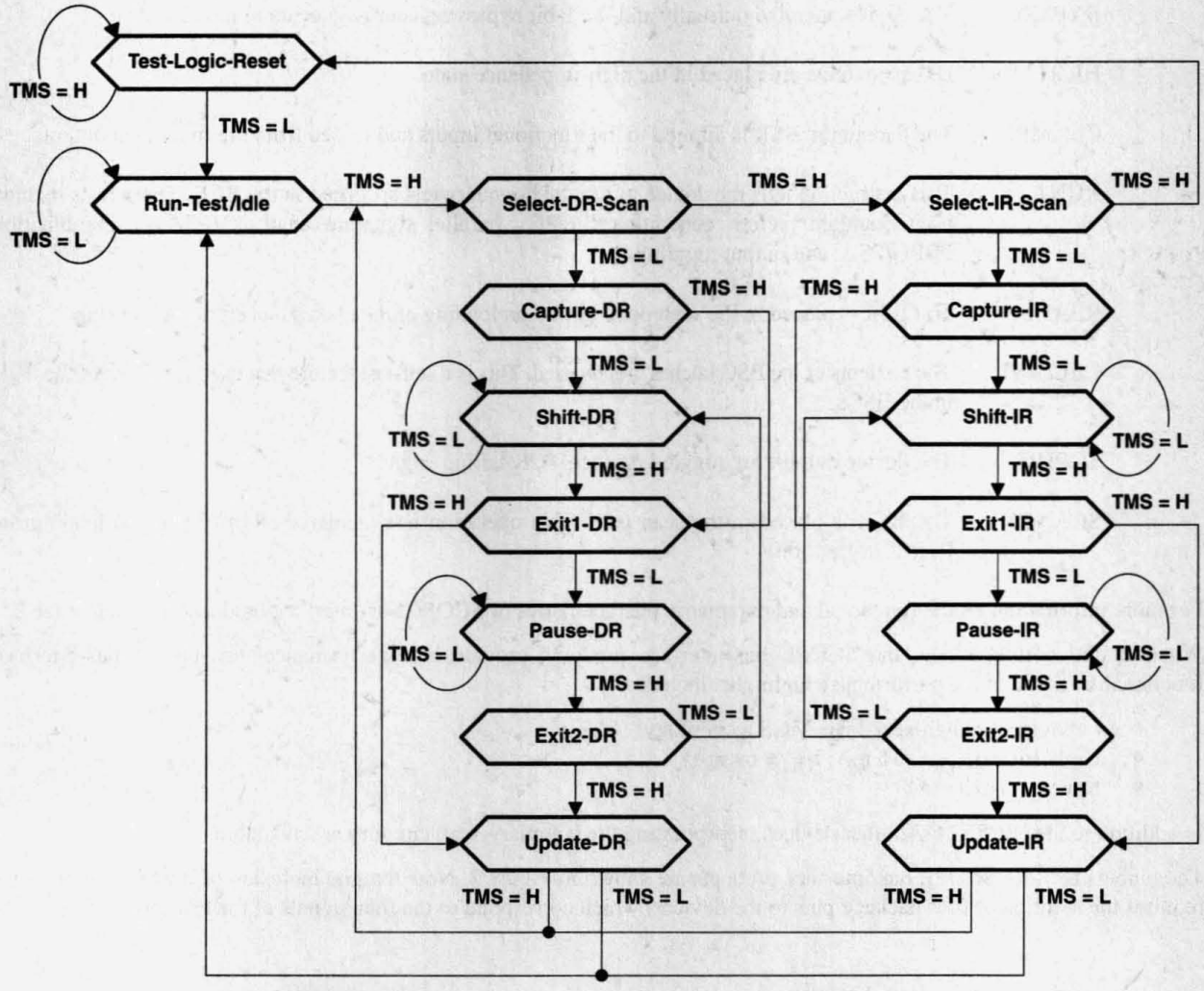


Figure 2. TAP-Controller State Diagram

The SCOPE bus-interface products conform to the IEEE 1149.1 protocol and perform the mandatory instruction of the document. Several other test operations, part of TI's SCOPE instruction set, are also implemented to greatly enhance the testing capabilities of the devices. The instructions implemented in the SCOPE bus-interface products, along with a brief description of the operation(s) performed, are as follows:

EXTEST	Data appearing at device inputs is captured. Data previously loaded into the output BSCs is forced.
SAMPLE	Data appearing at device inputs and outputs is captured without affecting the normal operation of the device.
INTEST	Data previously loaded into the input BSCs is applied to the device's internal logic, and the result is captured at the output BSCs. Data previously loaded into the output BSCs is forced.
BYPASS	The device operated normally and the 1-bit bypass register is selected in the scan path.
HIGHZ	Device outputs are placed in the high-impedance state.
CLAMP	The data in the BSR is applied to the functional inputs and forced from the functional outputs.
RUNT	This instruction tells the device to run the boundary test specified in the BCR. These tests include pseudorandom pattern generation (PRPG), parallel signature analysis (PSA), a combination PRPG/PSA, and output toggling.
READBN	The BSR is placed in the scan path, but no preloading of data takes place prior to shifting.
CELLTST	The contents of the BSC latches are inverted. This is a self-test feature that exercises most of the logic in the BSCs.
TOPHIP	The device outputs are toggled on each TCK falling edge.
SCANCN	The BCR is placed in the scan path. This operation is typically performed prior to loading the RUNT instruction.

For more information on the functional and parametric characteristics of SCOPE bus-interface products, see Reference 2.

When in the normal mode, the SCOPE bus-interface products provide high-performance, low-power, bus-interface functionality. Some of the performance highlights include:

- Fabricated in high-speed BiCMOS technology
- High drive (I_{OH} = –15 mA, I_{OL} = 64 mA)
- Low I_{CC} (<10 mA)

In addition to the 'BCT8244A, other devices incorporating the boundary-scan circuitry are available.

The pinouts for four SCOPE bus-interface products are shown in Figure 3. Note that the inclusion of the SCOPE circuitry requires the addition of four package pins to the devices, which correspond to the four signals of the test bus.

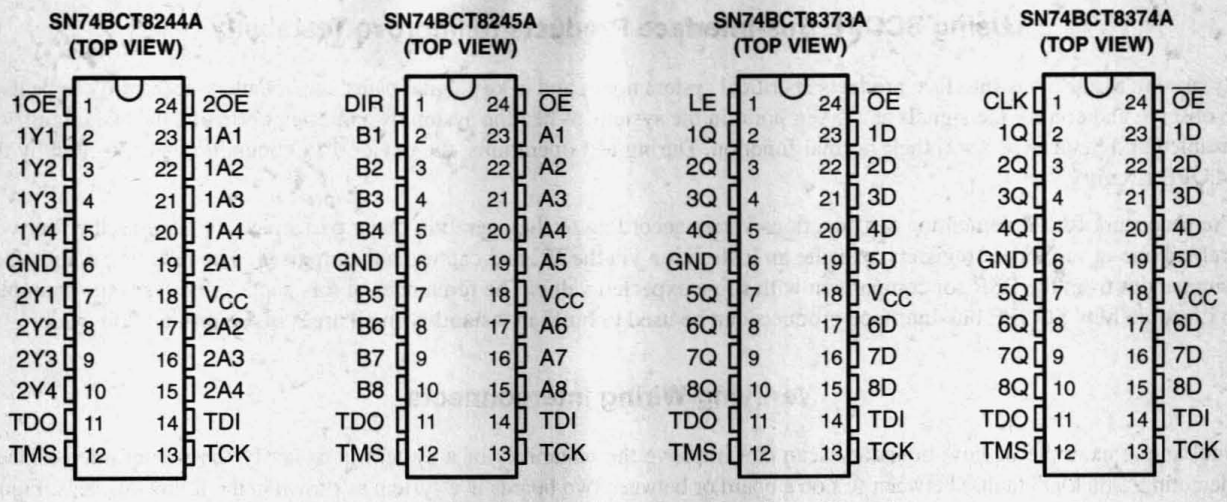


Figure 3. SCOPE Bus-Interface Product Pinouts

In the example of Figure 4, U1 is buffering data being received by U2. The scan path, in this case, consists of only U1 and U2, so U1's TDI pin is driven by the controller's TDO pin, and U2's TDO pin drives the controller's TDI pin. The integrity of the interconnect between U1 and U2 can be easily verified by using the ability of the SCOPE bus-interface products to force and capture data through the I/O periphery of the devices. The following procedure is one way (although not the only way) to verify that there are no opens or shorts between the outputs of U1 and the inputs of U2.

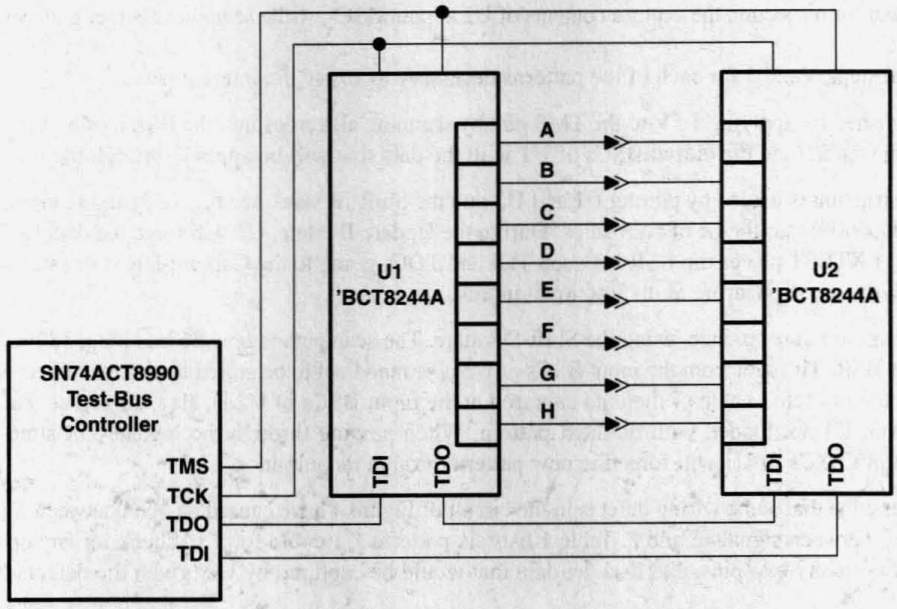


Figure 4. Simple Two-Device Scan Path

Using SCOPE Bus-Interface Products to Improve Testability

By placing SCOPE bus-interface products at critical system nodes and in key signal paths, the boundary-scan path can be used to observe and control the signals at a given point in the system. When the system is operating normally, the test circuitry is disabled and devices perform their normal function. During test operations, the device's I/O boundary is controlled by the SCOPE circuitry.

The procedure for implementing test functions varies according to the operation being performed. In general, the user will preload one or more data registers, execute an instruction via the IR, and capture a data register. The resulting data is then scanned out from the BSR for comparison with some expected value. The remainder of this paper provides some examples to illustrate how SCOPE bus-interface products can be used to build in testability in all areas of the product life cycle.

Verifying Wiring Interconnects

One simple example of how boundary scan can improve the testability of a system is to verify the wiring interconnects (detecting "stuck-at" faults) between ICs on a board or between two boards in a system as shown in the following steps. Figure 4 shows two 'BCT8244As being used to buffer signals between two separate parts of a system. They could be on either side of an edge connector, separated by PCB trace, or in any number of other configurations.

1. Initialize the scan path through a reset operation.
2. Scan all zeroes into the output BSCs of U1. This can be done with any of several instructions. ("Scan" means put the TAP in the appropriate shift state and serially load data through the TDI pin.)
3. Scan the EXTEST instruction into both U1 and U2.
4. Capture the BSR of U2.
5. Scan out for inspection the capture contents of U2's input BSCs, while scanning another pattern into the output BSCs of U1.
6. Repeat steps 4 and 5 for each of the patterns necessary to verify the interconnects.

Step 1 is accomplished by applying 10 V to the TMS pin, by scanning all zeroes into the BSRs, or by a power-down/power-up sequence. During step 2, load the output BSCs of U1 with the data that will be applied through the functional outputs.

The EXTEST instruction is loaded by putting U1 and U2 into the Shift-IR state (see Figure 2) and scanning the SCOPE opcode for EXTEST (00000000) into the IR of both chips. During the Update-IR state, U1 will force the data loaded in step 2 through its outputs. Since EXTEST places the BSR between TDI and TDO, going to the Capture-DR state (step 4) will load the input BSCs of U2 with the data appearing at its functional inputs.

In step 5, two things are done at once, using the Shift-DR state. The scan path is now 36 bits long, 18 bits from U1's BSR and 18 bits from U2's BSR. The data from the input BSCs of U2 is scanned out to be stored and/or examined. Since all zeroes from U1 were forced, the expected value of the data captured at the input BSCs of U2 is, also, all zeroes. During this same shift, the output BSCs of U1 are loaded with the next pattern. When passing through the Update-DR state after the shifting is complete, the output BSCs of U1 will force the new pattern through its outputs.

As an example, assume that some wiring defects in the circuit of Figure 4 have caused an open between U1 and U2 on signal C and a short circuit between signals E and F. Table 1 lists six patterns U1 could force to check for any opens between U1 and U2, or shorts between any two pins, and lists the data that would be captured by U2 (given the defects of this example).

Table 1. Shorts/Opens Verification

PATTERN	PATTERN FORCED BY U1 (A–G)	PATTERN CAPTURED BY U2 (A–G)†
1	00001111	00*1*01111
2	11110000	11110000
3	00110011	00110011
4	11001100	11*1*01100
5	01010101	01*1*10*0*01
6	10101010	10100*0*10

† Those bits indicating the presence of a defect appear in *italic* type.

Logic Verification

An application of two features of the SCOPE bus-interface products not included in the IEEE 1149.1 document is shown in Figure 5. PRPG and PSA can be used to verify the logic implementation of a design during the debug, prototype, or manufacturing test operations.

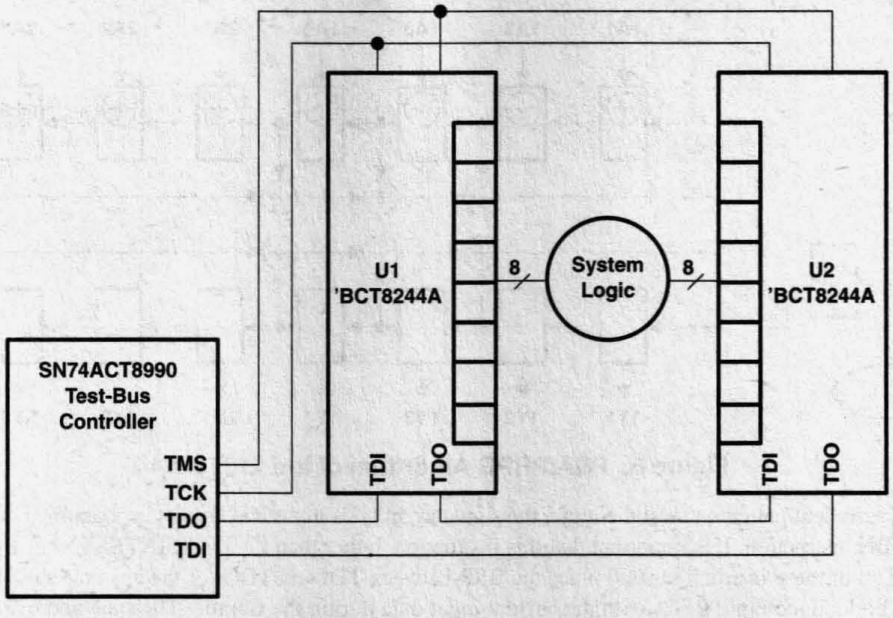


Figure 5. PRPG and PSA

During a PRPG or PSA operation, the BSRs of a device are configured as linear feedback shift registers. In this configuration, the registers perform either a pattern-generation or data-compression operation on each TCK cycle. By loading a known seed value (other than all zeroes) into the BSR and knowing the algorithm used, the user can determine the patterns that will be generated and/or the signature resulting from the data compression of inputs.

To exercise the system logic shown in Figure 5, the BSCs of U1 can be configured to output pseudorandom patterns and the input BSCs of U2 configured to compress data by performing the following operations:

1. Initialize the scan path.
2. Load the BSRs of both U1 and U2 with the seed values to be used during PRPG and PSA. Any value except all zeroes is acceptable.
3. Scan the SCANCN instruction into both U1 and U2.
4. Scan the PRPG code into U1's BCR and the PSA code into U2's BCR.
5. Scan the RUNT instruction into both U1 and U2.
6. Go to the Run-Test/Idle state of the TAP's state machine.
7. Execute the PRPG and PSA instructions for the desired number of TCK cycles.
8. Scan U2 with the READBN instruction.
9. Scan out the contents of U2's input BSCs and compare the resulting signature with the expected value.

To illustrate the concept, assume that a seed value of all ones is loaded into the BSRs of both U1 and U2 during step 2. Also assume there is no logic between U1 and U2 (i.e., U2's 1A1 = U1's 1Y1, U2's 1A2 = U1's 1Y2, etc.).

During steps 3–5 the SCOPE bus-interface products are loaded with the proper data and instruction to perform the pattern-generation and data-compression operations. SCANCN places the BCR between TDI and TDO so the simultaneous PSA/PRPG code (11) can be loaded using the Shift-DR TAP state. RUNT is loaded into the IR, and tells the SCOPE bus-interface products to examine their BCRs and run the test specified. In this example, the simultaneous PSA/PRPG function is being used. Figure 6 shows the algorithm used during the simultaneous PSA/PRPG operation.

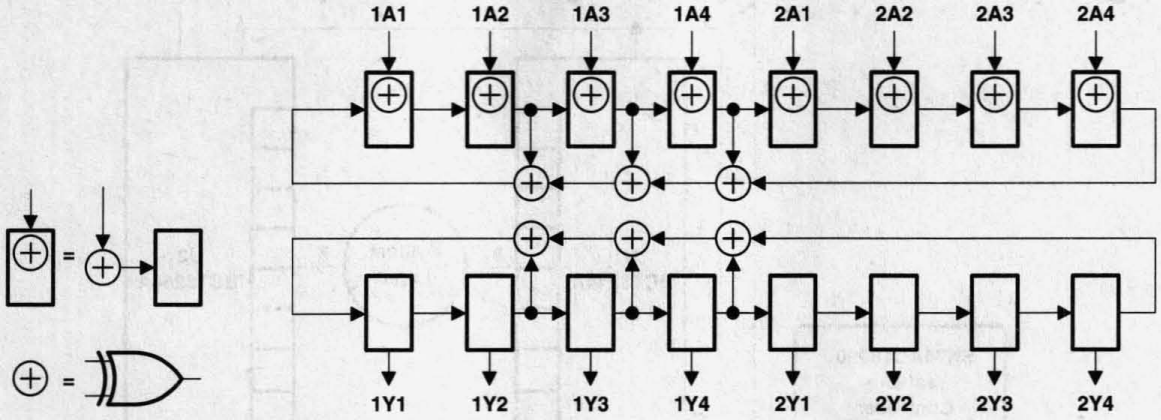


Figure 6. PSA/PRPG Algorithm of the 'BCT8244A

After generating sufficient patterns to test the logic, the signature in U2's input BSCs must be examined. This is accomplished using the READBN instruction. It is important that this instruction, rather than EXTEST, INTEST, or SAMPLE, be used. This is because, while all of these instructions will place the BSR between TDI and TDO for the ensuing Shift-DR TAP state, other instructions will preload the input BSCs with the current input data during the Capture-DR state and overwrite the signature. READBN does not preload the BSR during Capture-DR, so the signature is preserved.

Table 2 shows the pseudorandom patterns generated, and the resulting signature after each pattern, for the first 15 TCK cycles of this verify-wiring example. The first pattern, applied during the falling edge of TCK in Update-IR, is the seed value of all ones. The first signature (generated on the first rising edge of TCK after entering Run-Test/Idle) is based on that seed value. On the first falling edge of TCK after entering Run-Test/Idle, the first pseudorandom pattern is generated and applied. The last signature is generated on the rising edge of TCK as the TAP state changes from Run-Test/Idle to Select-DR-Scan. Note that there is one TCK cycle (as the TAP state changes from Update-IR to Run-Test/Idle) in which no patterns or signatures are generated.

Table 2. PRPG/PSA Sequence

CYCLE	PATTERN AFTER TCK↓ (1Y1–1Y4, 2Y1–2Y4)	SIGNATURE AFTER TCK↑ (1A1–1A4, 2A1–2A4)
0 (seed)	11111111	10000000
1	01111111	00111111
2	00111111	10100000
3	10011111	01001111
4	01001111	01101000
5	00100111	00010011
6	00010011	00011010
7	00001001	10000100
8	10000100	11000110
9	01000010	10100001
10	10100001	11110001
11	01010000	00101000
12	00101000	10111100
13	10010100	11001010
14	11001010	00101111
15	11100101	11110010

Although this verify-wiring example (Figure 4) contains no logic between U1 and U2, the same principles are applicable in more complex cases. This method can also be used to verify address decoding to memories, or to apply patterns to the input of a complex ASIC. By placing SCOPE bus-interface products in the critical paths, the user can control the signals being applied to any node in the system.

System Partitioning

Using SCOPE bus-interface products to buffer key signals allows for the effective partitioning of a system or board during test to remove unneeded or unwanted components. Partitioning a system into separate standalone test cells reduces the number of patterns required to test the section(s) of interest.

In Figure 7, the SCOPE bus-interface products are used to partition a shared-memory configuration in which a digital signal processor (DSP) and graphics signal processor (GSP) use the same memory. The 'BCT8245As (U1 and U3) are used to buffer data transmission between the processors and memory, and the 'BCT8373As (U2 and U4) are used as address latches. The four SCOPE bus-interface products are connected in a serial scan path with common TCK and TMS signals.

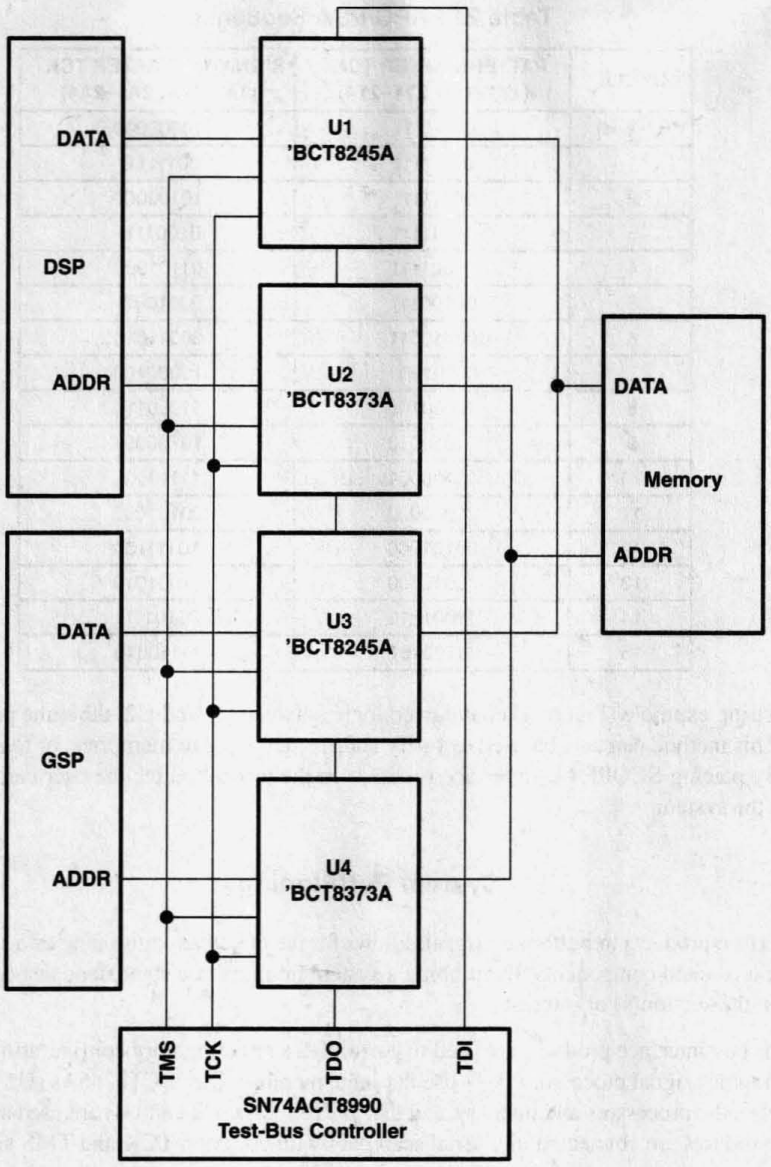


Figure 7. Partitioning a Shared-Memory Configuration

Using the SCOPE bus-interface products in this configuration creates many testing possibilities that go far beyond simple interconnect verification. For example, one or both processors can be effectively removed from system operation by scanning and executing the HIGHZ instruction on the units buffering it. This will cause the functional outputs of the SCOPE bus-interface products to go into the high-impedance state. This instruction also protects the SCOPE bus-interface products if some type of fixtured testing, such as bed-of-nails test, is to be used by ensuring that the functional outputs are not backdriven.

The status of the SCOPE bus-interface products can also be captured at any time by using the SAMPLE instructions. This operation does not disturb the normal operation of the devices and will not affect the system, but will capture the logic levels at all inputs and outputs. This information can be scanned out and compared to an expected value. The SAMPLE instruction is also useful for preloading the BSR prior to another test operation, since the SCOPE bus-interface products will continue to function in a normal mode during the preload scanning.

The circuitry in Figure 7 also allows the contents of any, or all, memory locations to be written to, or read from. A memory location can be verified by using the EXTEST instruction to force an address using U2 or U4 and capture the data appearing using U1 or U3. This illustrates the ability of the devices to both control and observe the signals to which they are connected. If the entire contents of the memory are known, the PRPG and PSA operations could unload the entire memory using a minimum number of clock cycles, with the final signature being scanned out for inspection.

Summary

Standard logic functions with boundary-scan circuitry provide a means for thorough testing of digital systems. By using a four-wire test bus compatible with IEEE 1149.1 protocol, the SCOPE bus-interface product family allows testability to be built into a system. Thus configured, the system will have complete controllability and observability of any node that can be addressed by a device in the scan path. Boundary-scan techniques are useful in system design, debug, and manufacturing test operations.

References

(1) *Proposed IEEE P1149.1, Standard Test Access Port and Boundary-Scan Architecture*, Draft D6, November 22, 1989

(2) *SCOPE Octal Data Sheets*

(3) Lee Whetsel and Greg Young, *Hardware Based Extensions to the JTAG Architecture*

Acknowledgment

The author of this article is R. J. Morgan.

What's an LFSR?

SCTA036A
December 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1996, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**7–159**
LFSR	**7–159**
Pseudorandom Pattern Generation	**7–160**
Maximal-Length LFSRs	**7–160**
PRPG and Fault Grading	**7–160**
External LFSRs	**7–163**
Pattern-Resistant Logic	**7–163**
PSA	**7–163**
Aliasing	**7–164**
Summary	**7–165**
Definitions	**7–165**
References	**7–165**
Acknowledgment	**7–165**

List of Illustrations

Figure	*Title*	*Page*
1	A 3-Bit Shift Register	7–159
2	Linear Feedback Shift Register	7–159
3	LFSR With Outputs Multiplexed With ASIC Inputs	7–161
4	Flowchart for Designing an LFSR Into an ASIC	7–162
5	A Parallel Signal Analyzer	7–164

SCOPE is a trademark of Texas Instruments Incorporated.

Introduction

The purpose of this article is to explain what a Linear Feedback Shift Register (LFSR) and a Parallel Signature Analyzer (PSA) are and how to use them to test a TI Application-Specific Integrated Circuit (ASIC) using SCOPE™ cells. This article begins with a description of an LFSR, goes into Pseudorandom Pattern Generation (PRPG) and fault grading, describes a PSA, and, last, shows how to implement the PSA and LFSR functions using SCOPE boundary-scan cells, which are compatible with IEEE 1149.1.

LFSR

An LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit (see Figure 1). Some of the outputs are combined in exclusive-OR configuration to form a feedback mechanism. A linear feedback shift register can be formed by performing exclusive-OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip-flops as shown in Figure 2.

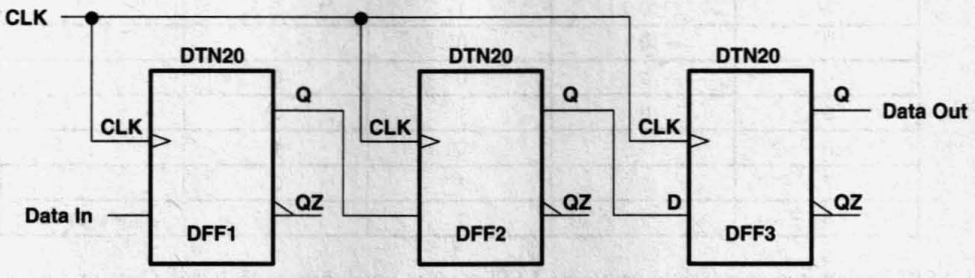


Figure 1. A 3-Bit Shift Register

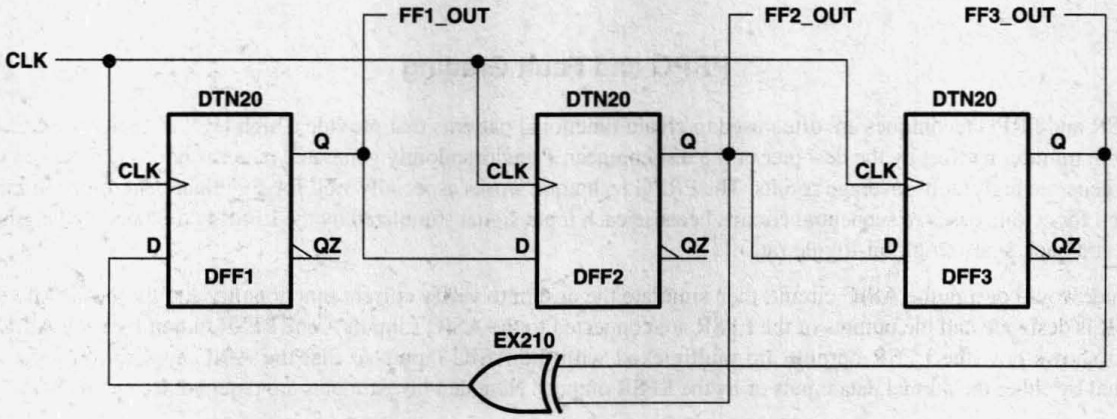


Figure 2. Linear Feedback Shift Register

Pseudorandom Pattern Generation

Linear feedback shift registers make extremely good pseudorandom pattern generators. When the outputs of the flip-flops are loaded with a seed value (anything except all 0s, which would cause the LFSR to produce all 0 patterns) and when the LFSR is clocked, it will generate a pseudorandom pattern of 1s and 0s. Note that the only signal necessary to generate the test patterns is the clock.

Maximal-Length LFSRs

A maximal-length LFSR produces the maximum number of PRPG patterns possible and has a pattern count equal to $2^n - 1$, where n is the number of register elements in the LFSR. It produces patterns that have an approximately equal number of 1s and 0s and have an equal number of runs of 1s and 0s.[1]

Because there is no way to predict mathematically if an LFSR will be maximal length, Peterson and Weldon[2] have compiled tables of maximal-length LFSRs to which designers may refer. Table 1 shows the patterns produced by the LFSR in Figure 2, assuming that a pattern of 111 was used as a seed.

Table 1. Pattern-Generator Seed Values

CLOCK PULSE	FF1_OUT	FF2_OUT	FF3_OUT	COMMENTS
1	1	1	1	Seed value
2	0	1	1	
3	0	0	1	
4	1	0	0	
5	0	1	0	
6	1	0	1	
7	1	1	0	
8	1	1	1	Starts repeat

In a practical ASIC design, the user would create an LFSR that is much bigger than three bits to get a large number of pseudorandom patterns before the patterns repeated. However, there are some practical restrictions to the length of the LFSR. A 32-bit maximal-length LFSR would create over 4 billion patterns that, at a 16-MHz clock rate, would take almost 5 minutes to generate the whole pattern set.

PRPG and Fault Grading

The LFSR and PRPG techniques are often used to create functional patterns that provide a high level of fault coverage for the ASIC with minimum effort by the designer or the test engineer. Pseudorandomly generated patterns have been proven to very quickly generate high-fault-coverage results. The PRPG technique works especially well for combinational logic but may also work well for certain cases of sequential circuits because each input signal stimulated by the LFSR is frequently changing from a 1 to 0 and back again (high bit-toggle rate).

A designer would design the ASIC circuit, then simulate the design to verify correct functionality and timing. Once verified, the LFSR is designed and the outputs of the LFSR are connected to the ASIC's inputs – one LFSR output for each ASIC input. Figure 3 shows how the LFSR outputs are multiplexed with the ASIC inputs so that the ASIC application logic can be stimulated by either the normal data inputs or by the LFSR outputs. Note that no extra pins are required to implement the LFSR.

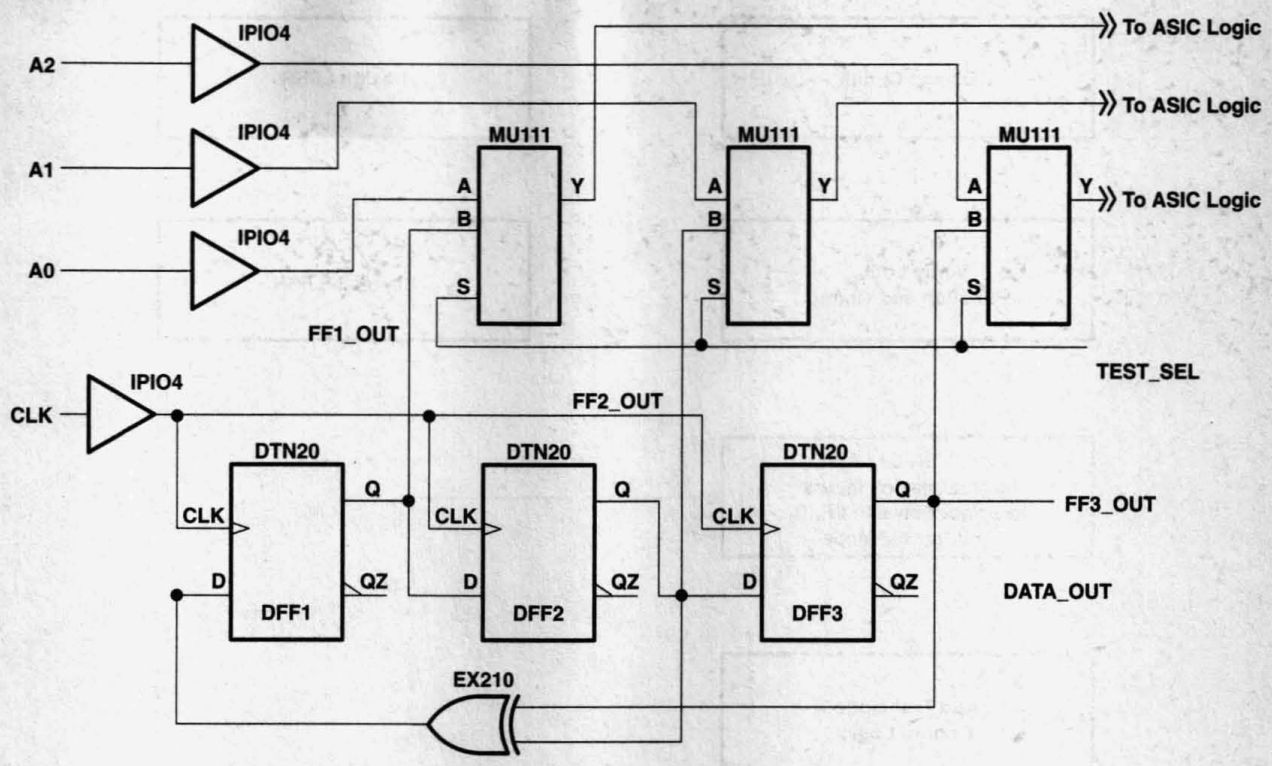


Figure 3. LFSR With Outputs Multiplexed With ASIC Inputs

Typically, a designer would capture the LFSR (or PSA) and simulate it by itself to evaluate and verify this subcircuit without having to simulate the total design. The designer could then easily examine the effects of different seed values on the patterns produced. This is particularly important if not all the $2^n - 1$ patterns that the LFSR could produce will be used in circuit testing. A designer would typically print out a sample of the patterns (every tenth or hundredth pattern, etc.) and use the printout when simulating the LFSR in the complete circuit to verify that the LFSR is generating the correct signals. Since the logic of the circuit has already been verified, the device would be put in the test mode to let the LFSR generate the inputs to the ASIC. Next, the outputs would be sampled every clock cycle to generate the expected outputs, given the inputs that the LFSR has created.

After verifying that the LFSR is generating the correct circuit inputs, the designer uses the resulting simulation vectors to fault grade the design. Fault grading enables the customer to ensure that the test vector set supplied for the design will catch manufacturing defects, such as shorted transistors and open metal lines (stuck-at faults, SA0, SA1). If the fault grade that results from applying the LFSR-generated simulation pattern is lower than required, the designer must generate additional patterns to raise the fault-grade level to the required value.

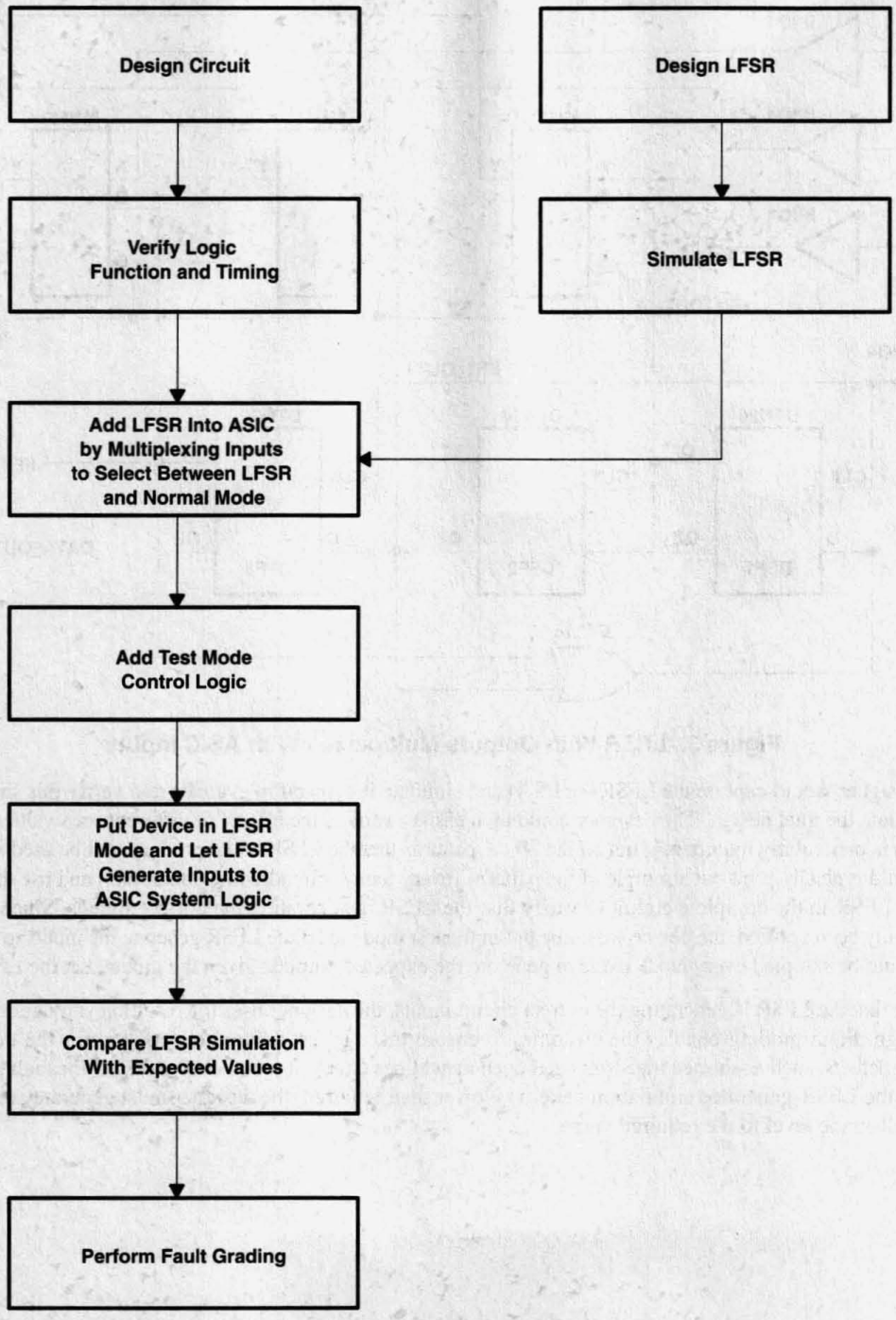


Figure 4. Flowchart for Designing an LFSR Into an ASIC

External LFSRs

While the previous section focused on how to use the LFSR for built-in test (BIT) of an ASIC, it should be noted that the LFSR logic incorporated in an ASIC can also be used to drive external logic. This is especially easy to do if TI's SCOPE cells have been used to incorporate boundary scan into the design. (See the SCOPE and LFSRs section.) In this scenario, the LFSR would be multiplexed with the ASIC outputs so that when the device is placed in a test mode, pseudorandom patterns would be generated and applied to the board logic. Board faults could then be detected by monitoring the board's edge connector or by capturing the logic's outputs and scanning the information out through the IEEE 1149.1 test bus.

Pattern-Resistant Logic

A major potential problem with the LFSR approach is that some logic, such as an NA810 (an 8-input NAND gate), is pattern resistant. When any of the eight inputs is a 0, the output is a 1. Only when all eight inputs are 1s does the logic change state. A manufacturing defect, such as a stuck-at-0 fault on the output of the NA810, is extremely difficult to detect using random patterns. Another problem is that some control signals might not toggle as often as they would when stimulated by an LFSR. A system reset or a clear terminal is a good example. If this signal toggled all the time, the logic would keep resetting and poor fault detection might result. Sequential logic circuits also present a problem. For example, if state 3 in a state machine can only be achieved if the device first enters into state 1, then state 2, a random-pattern sequence may have difficulty in creating inputs that move the circuit from one state to another in the correct order.

These problems can be solved by a variety of techniques, including using longer LFSRs to generate virtually every possible input, holding key control signals to a fixed value during the test stage, and augmenting the patterns with hand-generated patterns to improve fault grading.

PSA

As discussed previously, an LFSR of any significant length will generate a large number of patterns. To avoid having to test the outputs of several-hundred thousand or more vectors, a parallel signal analyzer (PSA) is used to compress the data at the outputs of the ASIC. As Figure 5 indicates, the PSA is nothing more than an LFSR with exclusive-OR gates between the shift register elements. In fact, a PSA can be used as an LFSR if the A_IN, B_IN, and C_IN inputs are all held at 0. If the inputs are held at 0, the PSA will generate exactly the same patterns as the LFSR in Figure 2.

Historically, however, the PSA is most often used as a parallel-to-serial compression circuit. The A_IN, B_IN, etc. inputs are multiplexed with the ASIC outputs. As each pattern is applied to the ASIC by the LFSR connected to the ASIC inputs, the output state of the ASIC is read into the PSA. As each new pattern is applied, the PSA will perform an exclusive-OR of the last pattern's outputs with the current pattern's output to create a new value in the PSA. This, conceptually, is very similar to a calculator adding a series of numbers. For example, if adding 2 + 3 + 6 + 9 + 1 + 1 using a calculator, first add the first state, 2, to the second state, 3, to get 5. Then add the new state, 6, to the old state, 5, to get the new result 11, etc. Instead of using addition, the PSA performs an exclusive-OR of the series of 1s and 0s together to get the new result.

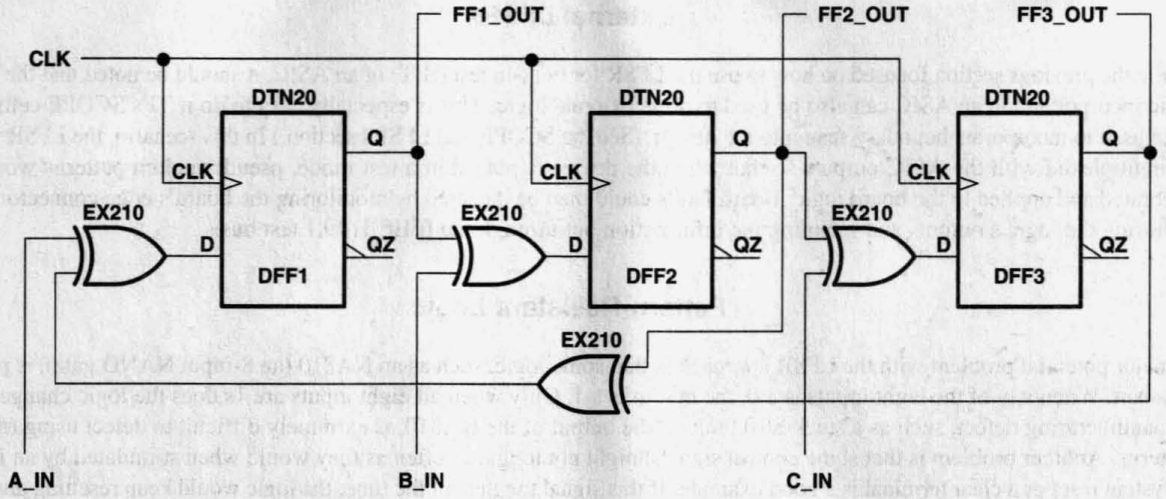


Figure 5. A Parallel Signal Analyzer

After a predefined number of patterns, the results in the PSA are read out of the ASIC (via FF1_OUT, FF2_OUT, and FF3_OUT) and compared to the expected value. Table 2 shows the signature that would be read out of the PSA if the inputs to the PSA were the outputs of the LFSR in Table 1.

Table 2. PSA Signatures

INPUTS					OUTPUTS		
CLOCK PULSE	A_IN	B_IN	C_IN		FF1_OUT	FF2_OUT	FF3_OUT
				SEED VALUE	1	0	0
1	1	1	1		1	0	1
2	0	1	1		1	0	1
3	0	0	1		1	1	1
4	1	0	0		1	1	1
5	0	1	0		0	0	1
6	1	0	1		0	0	1
7	1	1	0		0	1	0
8	1	1	1		0	1	0

Final signature = pattern 8, output results = 010

Aliasing

One major problem in compressing the results of a number of patterns into one pattern, called a signature, is aliasing. Aliasing occurs when the signature of the PSA is the same as expected, but the identity was caused by a cancellation of errors in the patterns. Thus, the silicon fault that caused the incorrect circuit response to the input pattern is never detected. To use the calculator example, 2 + 3 + 6 + 9 + 1 + 1 = 22, but so does 2 + 2 + 7 + 9 + 1 + 1. In this example, the second and third values that represent incorrect circuit values cancel each other out. Note that aliasing can occur only when there are two or more incorrect output patterns.

A way to minimize the aliasing problem is use maximal-length PSAs and to frequently read out the PSA signature for comparison to a known value or to monitor the most-significant PSA bit (FF3_OUT, in this case) continuously.

Summary

The LFSR is a shift register that has some of its outputs together in exclusive-OR configurations to form a feedback path. LFSRs are frequently used as pseudorandom pattern generators to generate a random number of 1s and 0s. Each output of the LFSR is multiplexed with an ASIC input and, when the device is placed in the LFSR (test) mode, the random, high-toggle-rate patterns produced are extremely good for generating high-fault coverage. To minimize the number of results that need to be compared to expected results, a PSA is used. The PSA compresses multiple parallel patterns into a single pattern signature that is compared to the expected value. If the signatures match, it is assumed that the ASIC passed the test vectors applied and there are no manufacturing defects.

Definitions

Sequential logic – logic functions whose next state depends on both the inputs to the function and its current state.

Combinatorial logic – logic functions that depend only on the inputs to the function.

Pattern-resistant logic – logic for which the pseudorandom pattern generation technique is not well suited because the random patterns will not cause a stuck-at fault to be caught.

Signature – the final result of the compression of a number of patterns using a PSA.

Aliasing – when the signature of a PSA is correct because two or more errors cancelled each other.

Stuck-at faults – manufacturing defects (such as a shorted transistor or an open metal line) that cause an input or an output of a logic function to be permanently stuck at a high or low logic level.

References

1 *Self-Test Services,* The STS ASIC Testability Seminar, Self-Test Services, Ambler, PA, 1989.

2 W.W. Peterson and E.J. Weldon, Jr. *Error Correcting Codes,* MIT press, Cambridge, MA 1972.

3 Texas Instruments, *SCOPE Cell Design Manual,* Texas Instruments Incorporated, Dallas, TX, 1990.

Acknowledgment

The author of this document is John Koeter.

General Design Considerations 1
Backplane Design 2
Device-Specific Design Aspects 3
5-V Logic Design 4
3.3-V Logic Design 5
Clock-Distribution Circuits (CDC) 6
Boundary-Scan IEEE Std 1149.1 (JTAG) Logic 7
Packaging 8
Index 9

Contents

	Page
Medium-Pin-Count Surface-Mount Package Information	8–3
Comparison of the Packages DIP, SOIC, SSOP, TSSOP, and TQFP	8–13
Recent Advancements in Bus-Interface Packaging and Processing	8–37
Thin Very Small-Outline Package (TVSOP)	8–49
Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices	8–95

Medium-Pin-Count Surface-Mount Package Information

First-In, First-Out (FIFO) Technology

SSPA001B
February 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**8–7**
Thermal Impedance	**8–7**
Package Moisture Sensitivity	**8–9**
Packing Methods/Quantities/Moisture Sensitivity/Dry Pack	**8–10**
Package Dimensions and Area Comparison	**8–11**
Test Sockets	**8–12**
Acknowledgment	**8–12**

Introduction

Texas Instruments (TI) provides ten types of plastic surface-mount packages for CMOS FIFO memory devices. These packages and the data bus width that each package supports are listed in Table 1.

Table 1. Plastic Surface-Mount FIFO Packages

PACKAGE	NO. OF DATA BITS
24-pin SOIC (DW)	1
28-pin SOIC (DW)	1
44-pin PLCC (FN)	9
64-pin TQFP (PM or PAG)	9
56-pin SSOP (DL)	18
68-pin PLCC (FN)	18
80-pin TQFP (PN)	18
80-pin PQFP (PH)	18
120-pin TQFP (PCB)	32 or 36
132-pin PQFP (PQ)	32 or 36

PLCC = plastic leaded chip carrier
PQFP = plastic quad flat package
SOIC = small-outline integraged circuit
SSOP = shrink small-outline package
TQFP = thin quad flat package
(xx) = TI package nomenclature

This application report discusses several topics concerning the FIFO packages listed in Table 1:

- Thermal impedance, Θ_{JA}, and the chip junction temperature of the device
- The need for dry packing to maintain safe moisture levels inside the package
- Three kinds of packing used by TI to ship FIFOs to customers
- Package dimensions, including two-dimensional drawings that show areas, heights, and lead pitches
- Area comparison of surface-mount packages used for commercial FIFO memories
- Test sockets available for surface-mount FIFO packages

Thermal Impedance

Thermal impedance is defined as the ability of a package to dissipate heat generated by an electronic device and is abbreviated as Θ_{JA}. Θ_{JA} is the thermal impedance from the integrated-circuit chip junction to the free air (ambient). By far the most common measure of package thermal performance is Θ_{JA}. Θ_{JA} values are also subject to interpretation. Factors that can greatly influence the measurement and calculation of Θ_{JA} are:

- Board mounted (yes or no)
- Traces (size, composition, thickness, and geometry)
- Orientation (horizontal or vertical)
- Ambient (volume)
- Proximity (any other surfaces near the device being measured)

In August 1996, the Electronics Industries Association released Standard EIA/JESD51-3, "Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages." This standard provides guidelines for designing the test board used in taking thermal-impedance measurements of integrated-circuit packages. Prior to the release of this standard, thermal-impedance data for similar packages varied greatly across the industry because of the use of different test-board designs. In particular, the characteristics of the test board were found to have a dramatic impact on the measured Θ_{JA}. As the industry converts to this standard test-board design, the variation in thermal characteristics data caused by the board should be minimized.

Key features of the standard test-board design are:

- Board thickness: 0.062 in.
- Board dimension: 3.0 in. × 4.5 in. for packages < 27.0 mm in length
- Board dimension: 4.0 in. × 4.5 in. for packages > 27.0 mm in length
- Trace thickness: 0.0028 in.
- Trace length: 0.984 in. (25.0 mm)

TI's Standard Linear and Logic (SLL) product group uses EIA/JESD51-3 to design the test boards for thermal-impedance measurements. The parameters outlined in this standard are used to set up thermal models.

The unit for Θ_{JA} is degrees Celsius per watt. Table 2 lists Θ_{JA} for SOIC, SSOP, PLCC, TQFP, and PQFP packages under four different air-flow environments: 0, 150, 250, and 500 linear feet/minute. The chip junction temperature (T_J) can be determined using equation 1.

$$T_J = \theta_{JA} \times P_T + T_A \quad (1)$$

Where:

T_J = chip junction temperature (°C)
Θ_{JA} = thermal resistance, junction to free-air (°C/watt)
P_T = total power dissipation of the device (watts)
T_A = free-air (ambient) temperature in the particular environment in which the device is operating (°C)

Table 2. Thermal Impedance, Θ_{JA}, for FIFO Packages

PACKAGE†	LEAD FRAME	Θ_{JA} (°C/W)				ACTUAL/ MODEL
		0 LFPM	150 LFPM	250 LFPM	500 LFPM	
24-pin SOIC (DW)	Copper	80.7	53.7	47.5	40.7	Model
28-pin SOIC (DW)	Copper	78.2	54.3	48.4	41.9	Model
44-pin PLCC (FN)	Copper	46.2	38.6	35.4	31.6	Model
56-pin SSOP (DL)	Copper	73.5	62.3	59	54.6	Actual
64-pin TQFP (PM)	Copper	66.9	53.6	47.6	40.6	Model
64-pin TQFP (PAG)	Copper	58.2	48.8	45.2	40.3	Actual
68-pin PLCC (FN)	Copper	39.3	33	30.5	27.6	Model
80-pin TQFP (PN)	Copper	61.5	52.8	49.3	44.6	Actual
80-pin PQFP (PH)	Alloy 42	76.1	67.9	61.4	53.6	Model
120-pin TQFP‡ (PLB)	Copper	28.1	22.3	21	18	Model
132-pin PQFP (PQ)	Copper	38.8	27.3	25.1	22.4	Model

† (xx) = TI package nomenclature
‡ Heat slug molded inside the package

Θ_{JA} generally increases with decreasing package size, but this is not true with the 120-pin SQFP package. A heat slug molded inside the package absorbs a large amount of heat dissipated by the device. As a result, this package provides a relatively low Θ_{JA} (as low as 18°C/W at 500 LFPM air flow).

Package Moisture Sensitivity

When a plastic surface-mount package is exposed to temperatures typical of furnace reflow, infrared (IR) soldering, or wave soldering (215°C or higher), the moisture absorbed by the package turns to steam and expands rapidly. The stress caused by this expanding moisture results in internal and external cracking of the package that leads to reliability failures. Possible damage includes the delamination of the plastic from the chip surface and lead frame, damaged bonds, cratering beneath the bonds, and external package cracks.

To prevent potential damage, packages that are susceptible to the effects of moisture expansion undergo a process called dry pack. This dry-pack process helps reduce moisture levels inside the package. The process consists of a 24-hour bake at 125°C followed by sealing of the packages in moisture-barrier bags with desiccant to prevent reabsorption of moisture during the shipping and storage processes. These moisture-barrier bags allow a shelf storage of one year from the date of seal at < 40°C and < 90% relative humidity. Once the moisture-barrier bag is opened, the devices in it must be handled by one of the following four methods, listed in descending order of preference:

- The devices may be mounted within x hours (see Table 3), depending on the moisture-sensitivity level of the package (see Table 4) in an atmospheric environment of less than 60% relative humidity and less than 30°C.
- The devices may be stored outside the moisture-barrier bag in a dry-atmospheric environment of less than 20% relative humidity until future use.
- The devices may be resealed in the moisture-barrier bag adding new fresh desiccant to the bag. When the bag is opened again, the devices should be used within the x-hour time limit or resealed again with fresh desiccant.
- The devices may be resealed in the moisture-barrier bag using the original desiccant. This method does not allow the floor life of the devices to be extended. The cumulative exposure time before reflow must not exceed a total of x hours.

Plastic surface-mount FIFO devices are tested for moisture sensitivity in accordance with JESD A112-A, "Moisture-Induced Stress Sensitivity for Plastic Surface Mount Devices" and IPC SM-786A, "Procedures for Characterizing and Handling of Moisture/Reflow-Sensitive IC's."

Table 3. Exposure Time Versus Moisture-Level Classification

MOISTURE LEVEL	X HOURS
2	8,760 (1 year)
3	168
4	72
5	48
6	6

Packing Methods/Quantities/Moisture Sensitivity/Dry Pack

TI uses three kinds of packing to ship FIFOs to customers: tubes, tape/reel, and trays. The quantities for each kind of packing are listed in Table 4. The shipping quantity is defined as the maximum number of packages that can be packed in a single shipping unit (e.g., the maximum number of 56-pin SSOP packages that can be packed in a tube is 20). Whether or not the packages require dry pack before shipping is noted in the dry-pack column.

Table 4. Packing Methods and Quantities

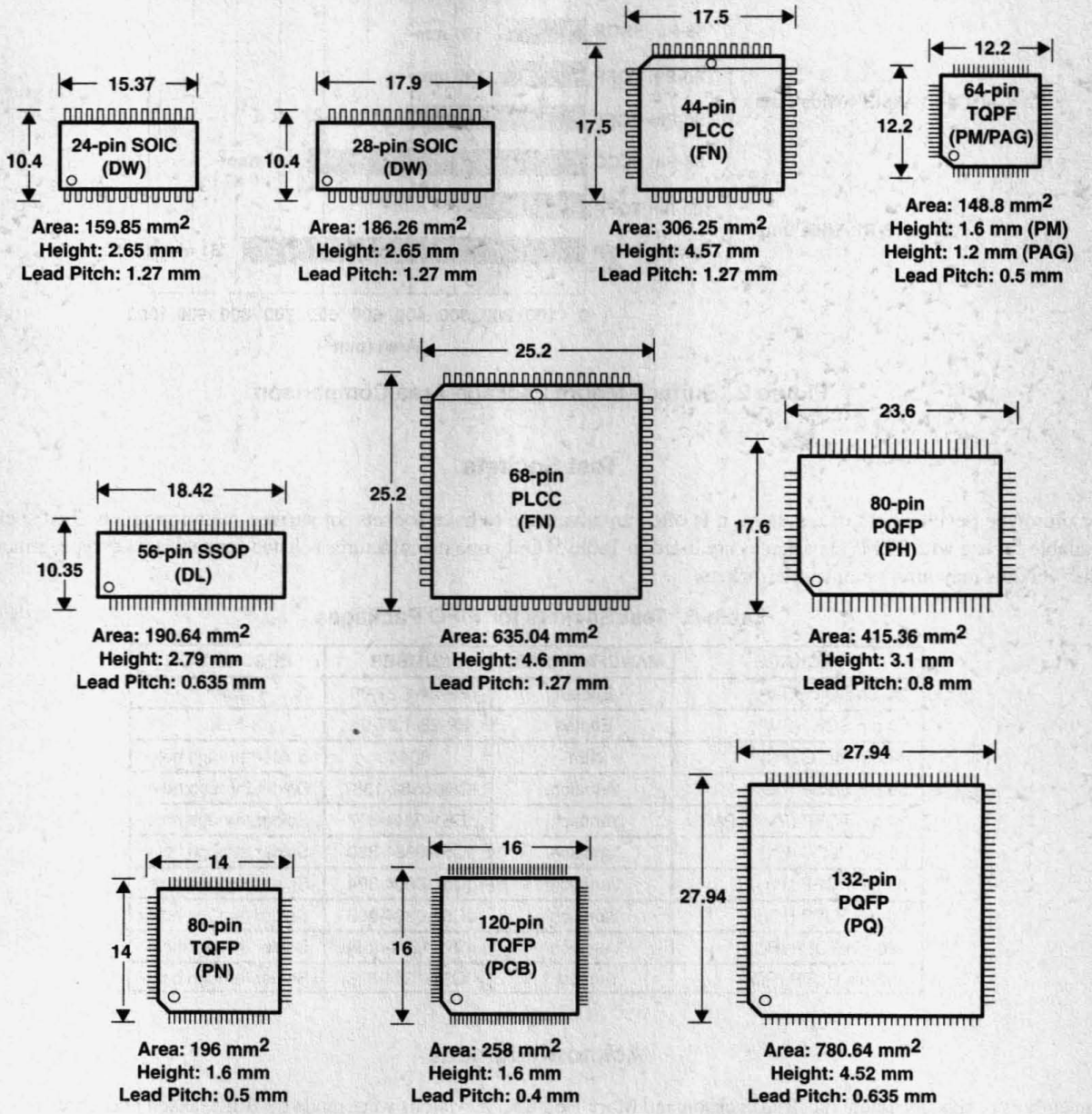
PACKAGE†	PACKING METHOD			MOISTURE SENSITIVITY LEVEL	DRY PACK
	TUBE‡	TAPE/REEL‡	TRAYS‡		
24-pin SOIC (DW)	25	1000	N/A	1	No
28-pin SOIC (DW)	20	1000	N/A	1	No
44-pin PLCC (FN)	26	500	N/A	1	No
56-pin SSOP (DL)	20	1000	N/A	1	No
64-pin TQFP (PM)	N/A	N/A	160	4	Yes
64-pin TQFP (PAG)	N/A	N/A	160	2	Yes
68-pin PLCC (FN)	18	250	N/A	2	Yes
80-pin TQFP (PN)	N/A	N/A	96	2	Yes
80-pin PQFP (PH)	N/A	N/A	66	3	Yes
120-pin TQFP (PCB)	N/A	N/A	24	2	Yes
132-pin PQFP (PQ)	N/A	N/A	36	3	Yes

† (xx) = TI package nomenclature
‡ TI reserves the right to change any of the shipping quantities at any time without notice.
N/A = not applicable

Package Dimensions and Area Comparison

Figure 1 contains two-dimensional drawings of the ten available surface-mount FIFO packages. The dimensions given are averages. For detailed mechanical drawings of these packages, please refer to the mechanical drawing section of the 1996 *High-Performance FIFO Memories Data Book*, literature number SCAD003C.

Figure 2 shows the area comparison of surface-mount packages for FIFOs from TI and other FIFO vendors.



NOTE: Package linear dimensions are in millimeters.

Figure 1. Package Dimensions

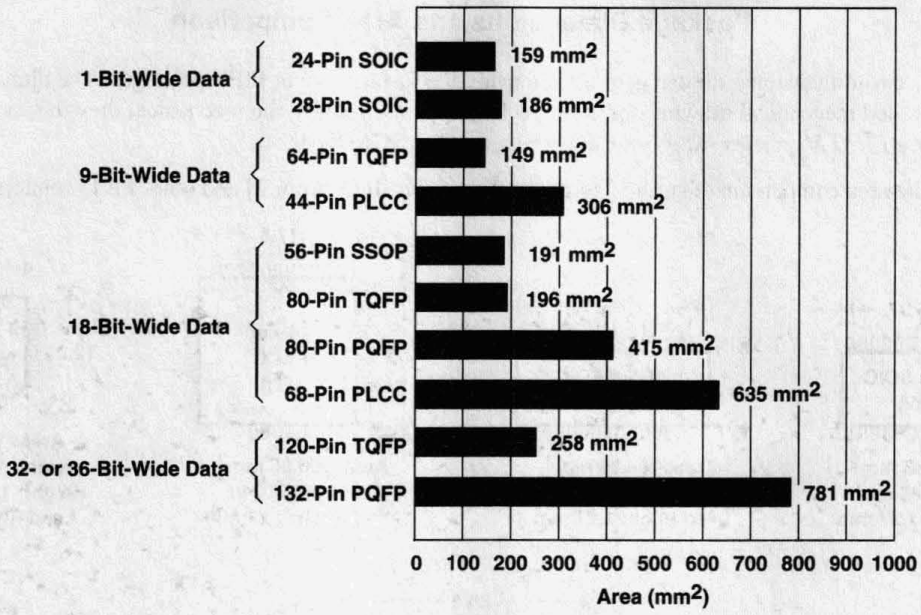


Figure 2. Surface-Mount Package Area Comparison

Test Sockets

For prototype development of a system, it is often an advantage to have sockets for surface-mount products. Test sockets available for use with TI FIFO packages are listed in Table 5. Only one manufacturer is listed for each socket type, although other vendors may offer comparable sockets.

Table 5. Test Sockets for FIFO Packages

PACKAGE	MANUFACTURER	NUMBER	DESCRIPTION
24-pin SOIC (DW)	Enplas	FP-24-1.27-08	N/A
28-pin SOIC (DW)	Enplas	FP-28-1.27-06	N/A
44-pin PLCC (FN)	NEY	6044	Solder through hole
56-pin SSOP (DL)	Yamaichi	IC51-0562-1387	Solder through hole
64-pin TQFP (PM or PAG)	Yamaichi	IC51-0644-807	Solder through hole
68-pin PLCC (FN)	Yamaichi	IC51-0684-390	Solder through hole
80-pin PQFP (PH)	Yamaichi	IC51-0804-394	Solder through hole
80-pin TQFP (PN)	Yamaichi	IC51-0804-808	Solder through hole
120-pin TQFP (PCB)	Yamaichi	IC51-1204-1596	Solder through hole
132-pin PQFP (PQ)	Yamaichi	IC51-1324-828	Solder through hole

Acknowledgment

The authors of this document are Tom Jackson and Mary Helmick. Revisions were made by Bill Manson and Thomas Lewis (February 1997).

Comparison of the Packages DIP, SOIC, SSOP, TSSOP, and TQFP

SDYA003A
March 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	Page
Abstract	**8–17**
1 Introduction	**8–17**
2 Package Dimensions	**8–17**
3 Electrical Characteristics	**8–21**
3.1 Package Parameters	8–21
3.2 Simultaneous-Switching Behavior	8–25
3.3 Increase of Delay Time	8–28
4 Thermal Characteristics	**8–30**

List of Illustrations

Figure	Title	Page
1	20-Pin DIP Package (SN74...N)	8–17
2	20-Pin SOIC Package (SN74...DW)	8–18
3	20-Pin SSOP Package (SN74...DB)	8–18
4	20-Pin TSSOP Package (SN74...PW)	8–18
5	48-Pin SSOP Package (SN74...DL)	8–19
6	48-Pin TSSOP Package (SN74...DGG)	8–19
7	100-Pin TQFP Package (SN74...PZ)	8–20
8	Capacitances, Inductances, and Coupling Factors of a 20-Pin DIP	8–21
9	Capacitances, Inductances, and Coupling Factors of a 20-Pin SOIC	8–22
10	Capacitances, Inductances, and Coupling Factors of a 20-Pin SSOP	8–22
11	Capacitances, Inductances, and Coupling Factors of a 20-Pin TSSOP	8–23
12	Capacitances, Inductances, and Coupling Factors of a 48-Pin SSOP	8–23
13	Capacitances, Inductances, and Coupling Factors of a 48-Pin TSSOP	8–24
14	Capacitances, Inductances, and Coupling Factors of a 100-Pin TQFP	8–24
15	Simultaneous Switching of an SN74ABT245N (20-Pin DIP)	8–25
16	Simultaneous Switching of an SN74ABT245DW (20-Pin SOIC)	8–26
17	Simultaneous Switching of an SN74ABT245DB (20-Pin SSOP)	8–26
18	Simultaneous Switching of an SN74ABT245PW (20-Pin TSSOP)	8–27
19	Simultaneous Switching of an SN74ABT16245DL (48-Pin SSOP)	8–27

Widebus and Widebus+ are trademarks of Texas Instruments Incorporated.

List of Illustrations (continued)

Figure	*Title*	*Page*
20	Simultaneous Switching of an SN74ABT16245DGG (48-Pin TSSOP)	8–28
21	Simultaneous Switching of an SN74ABT32501PZ (100-Pin TQFP)	8–28
22	Delay Time of a Rising Edge as a Function of the Number of Simultaneously Switching Outputs (Measured With an SN74ABT245 in Seven Different Packages)	8–29
23	Delay Time of a Falling Edge as a Function of the Number of Simultaneously Switching Outputs (Measured With an SN74ABT245 in Seven Different Packages)	8–29
24	Thermal Characteristics of a 20-Pin DIP	8–30
25	Thermal Characteristics of a 20-Pin SOIC	8–31
26	Thermal Characteristics of a 20-Pin SSOP	8–32
27	Thermal Characteristics of a 20-Pin TSSOP	8–33
28	Thermal Characteristics of a 48-Pin SSOP	8–34
29	Thermal Characteristics of a 48-Pin TSSOP	8–35
30	Thermal Characteristics of a 100-Pin TQFP	8–36

List of Tables

Table	*Title*	*Page*
1	Thermal Characteristics of a 20-Pin DIP	8–30
2	Thermal Characteristics of a 20-Pin SOIC	8–31
3	Thermal Characteristics of a 20-Pin SSOP	8–32
4	Thermal Characteristics of a 20-Pin TSSOP	8–33
5	Thermal Characteristics of a 48-Pin SSOP	8–34
6	Thermal Characteristics of a 48-Pin TSSOP	8–35
7	Thermal Characteristics of a 100-Pin TQFP	8–36

Abstract

This application report compares mechanical data, electrical characteristics, and thermal parameters of seven packages: 20-pin DIP (dual in-line package), 20-pin SOIC (small-outline integrated circuit), 20-pin and 48-pin SSOP (shrink small-outline package) and TSSOP (thin shrink small-outline package), and 100-pin TQFP (thin quad flat package) for Widebus+™.

1 Introduction

The ever-increasing integration of electronic circuits has required corresponding miniaturization of component packages. Recent developments have also included space-saving packages for standard components such as bus drivers.

This report compares the dimensions, electrical characteristics, and thermal parameters of seven different package outlines:

- DIP (dual in-line package) . . . . . 20-pin N
- SOIC (small-outline integrated circuit) . . . . . 20-pin DW
- SSOP (shrink small-outline package) . . . . . 20-pin DB
- TSSOP (thin shrink small-outline package) . . . . . 20-pin PW
- SSOP (shrink small-outline package) for Widebus™ . . . . . 48-pin DL
- TSSOP (thin shrink small-outline package) for Widebus™ . . . . . 48-pin DGG
- TQFP (thin quad flat package) for Widebus+™ . . . . . 100-pin PZ

In addition to the package name and the number of pins, every package has a unique code (N, DW, DB, etc.) that helps define the required package, for example, when ordering a specific function.

The influence of various kinds of packages on electrical characteristics is examined and demonstrated in this application report by means of measurements on bidirectional bus drivers SN74ABT245, SN74ABT16245, and SN74ABT32501.

2 Package Dimensions

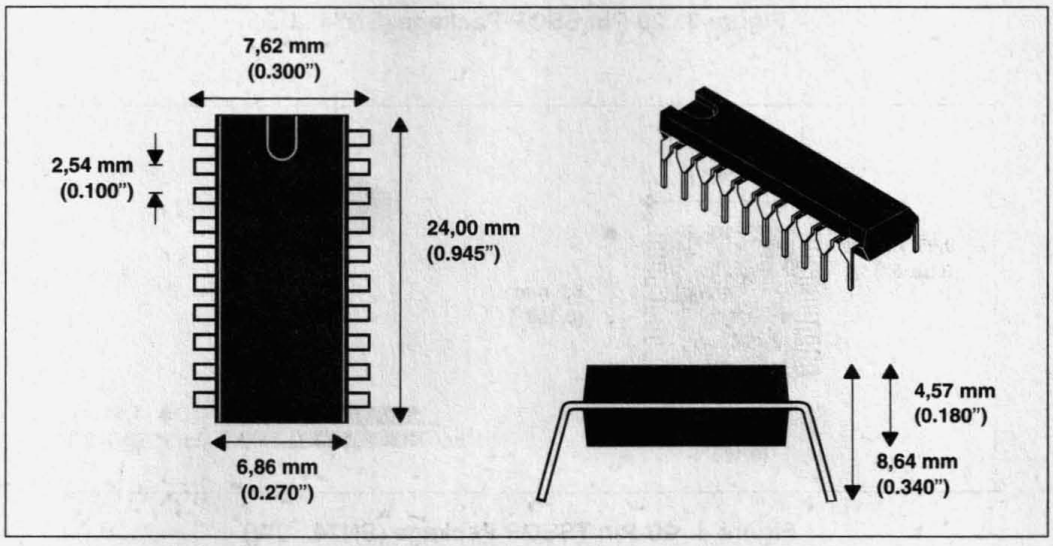


Figure 1. 20-Pin DIP Package (SN74...N)

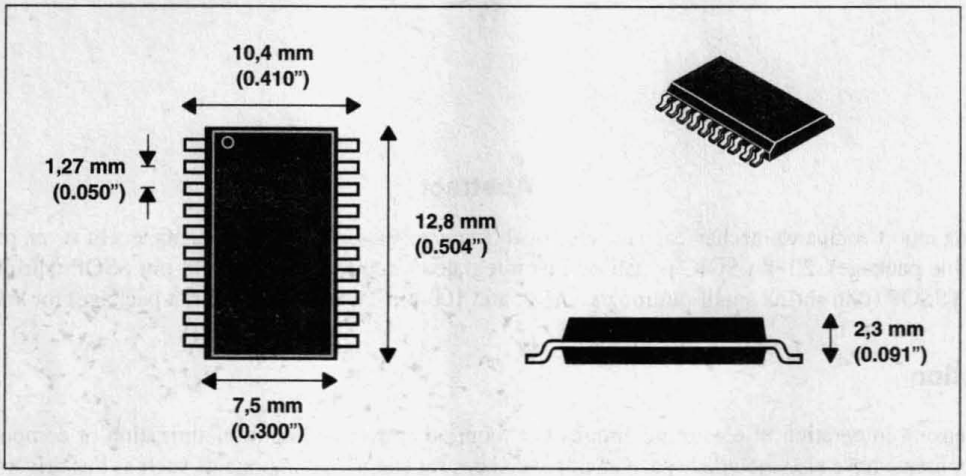


Figure 2. 20-Pin SOIC Package (SN74...DW)

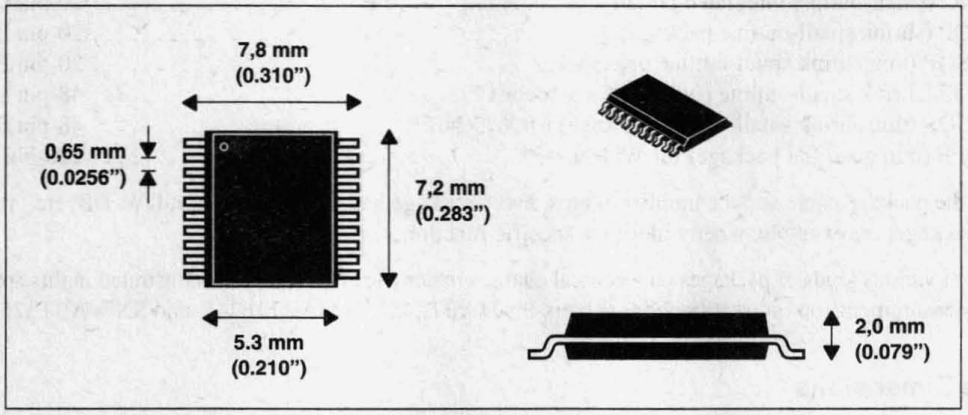


Figure 3. 20-Pin SSOP Package (SN74...DB)

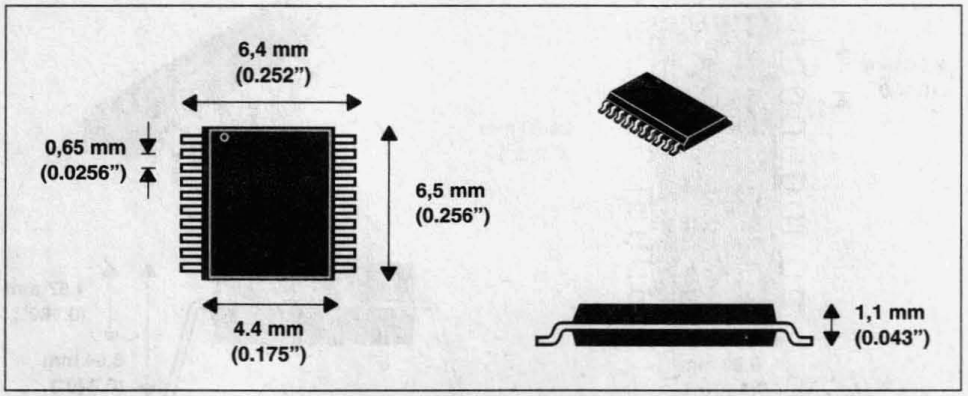


Figure 4. 20-Pin TSSOP Package (SN74...PW)

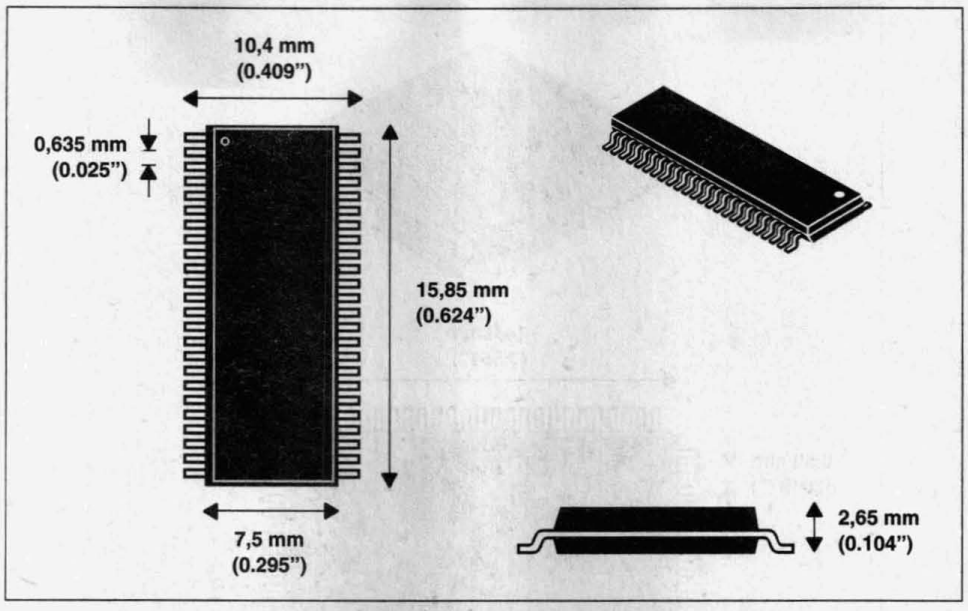


Figure 5. 48-Pin SSOP Package (SN74...DL)

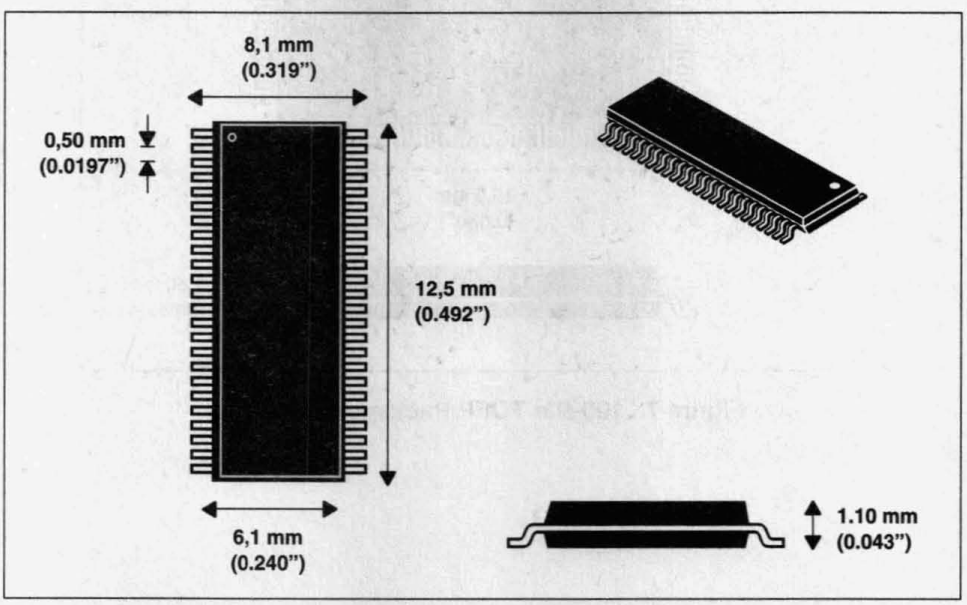


Figure 6. 48-Pin TSSOP Package (SN74...DGG)

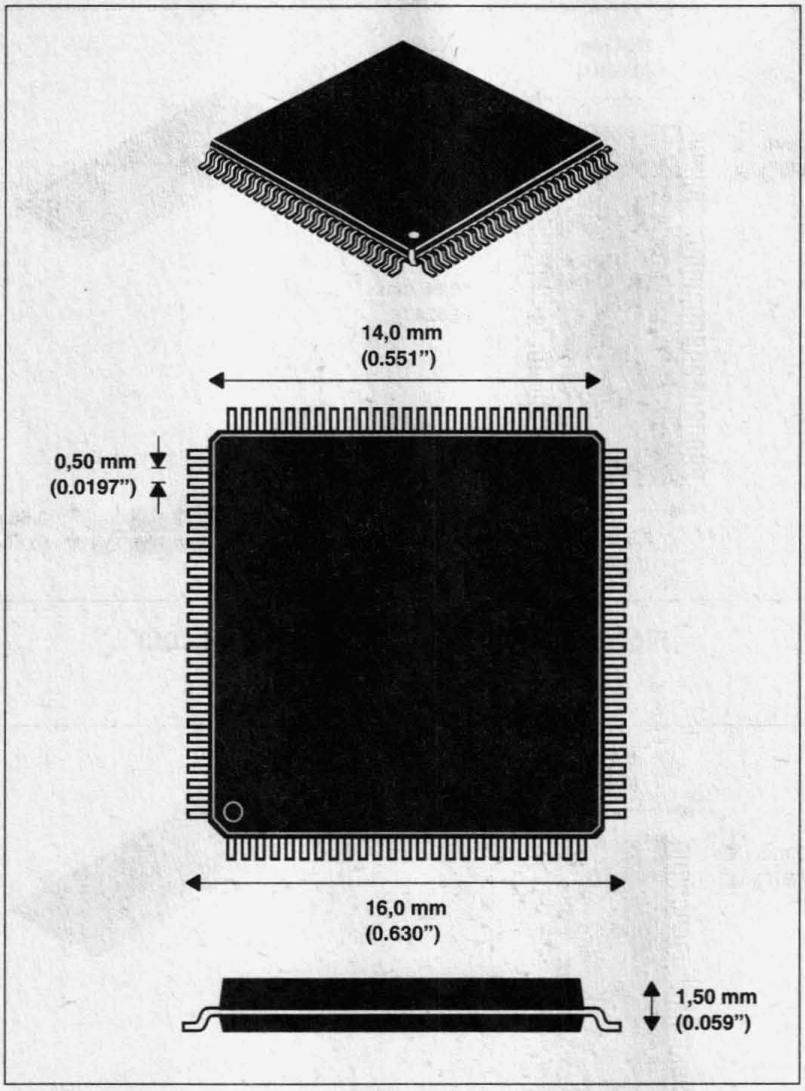


Figure 7. 100-Pin TQFP Package (SN74...PZ)

3 Electrical Characteristics

3.1 Package Parameters

The following factors determine the electrical characteristics of a package:

- Capacitance of a pin to ground
- Inductance of the pin
- Coupling factors of the pins with each other

The pins used for the supply voltage should have low inductance, and all three of the above parameters of all the signal lines should have values as low as possible. The three electrical parameters of the package are determined by the following:

- Length of the connections to the pins within the package
- Spacing between these connections
- Length of the wire bonds

A DIP package, for example, has significantly longer internal connections than an SOIC, an SSOP, or a TSSOP package. A long connection results in high inductance and high coupling factors. In addition, the increased area resulting from long connections gives rise to high capacitance. With small package outlines , such as the SSOP, the inductance and the capacitance of internal connections are significantly lower. However, the reduction in coupling factor achieved by the short connections will be partly offset by the smaller spacing between them. To a lesser extent, the size of the chip and its lead frame has an influence on electrical characteristics. Therefore, the measurement values given in this section should be understood as typical and refer only to the component actually measured. Nevertheless, they show the typical dependence of the measurement values on package type.

Figures 8 through 14 show the capacitances and inductances of the individual pins for the 20-pin DIP, SOIC, SSOP, and TSSOP packages; 48-pin SSOP and TSSOP packages; and the 100-pin TQFP package. In addition, the coupling factors between neighboring pins can be seen. Variations are possible as a result of differences between lead frames.

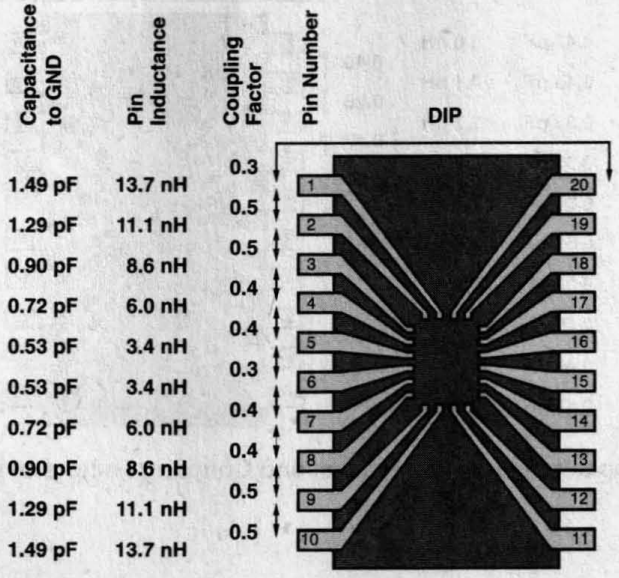


Figure 8. Capacitances, Inductances, and Coupling Factors of a 20-Pin DIP

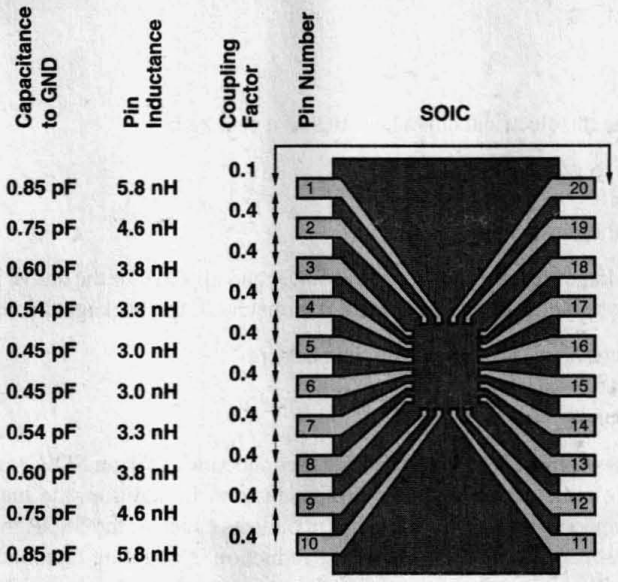


Figure 9. Capacitances, Inductances, and Coupling Factors of a 20-Pin SOIC

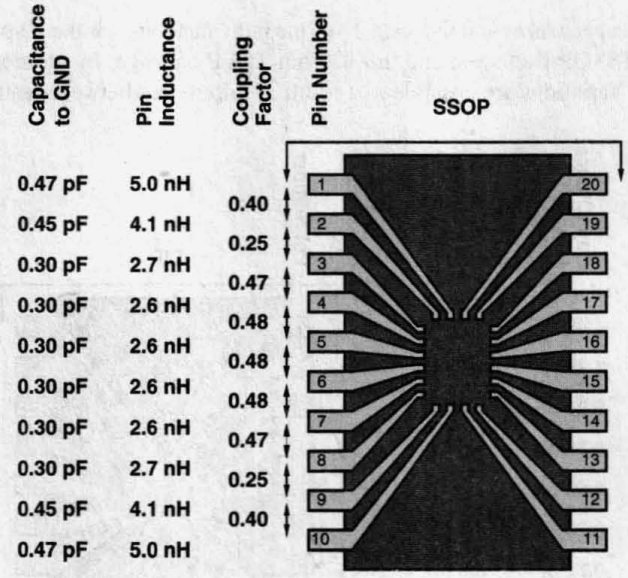


Figure 10. Capacitances, Inductances, and Coupling Factors of a 20-Pin SSOP

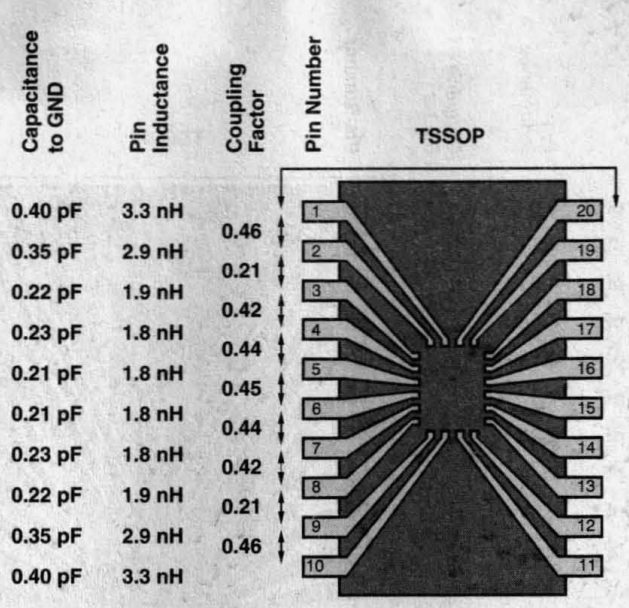


Figure 11. Capacitances, Inductances, and Coupling Factors of a 20-Pin TSSOP

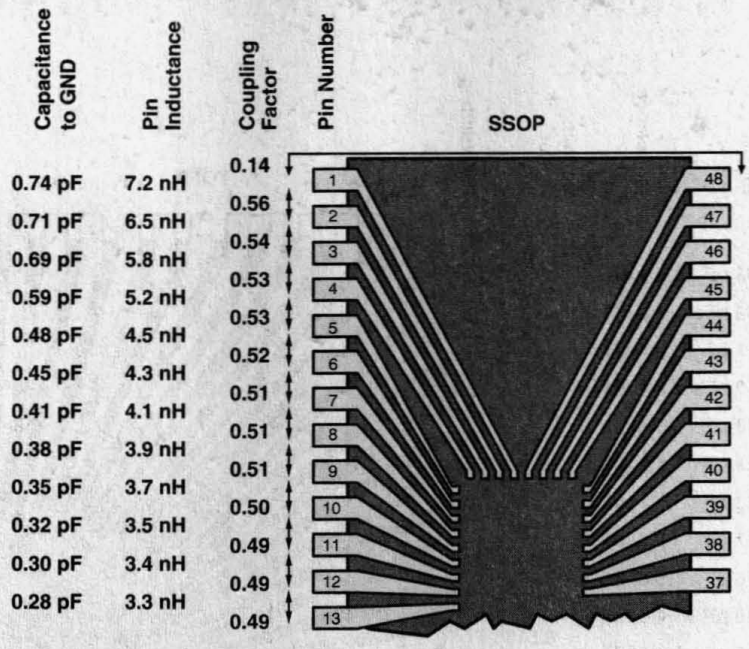


Figure 12. Capacitances, Inductances, and Coupling Factors of a 48-Pin SSOP

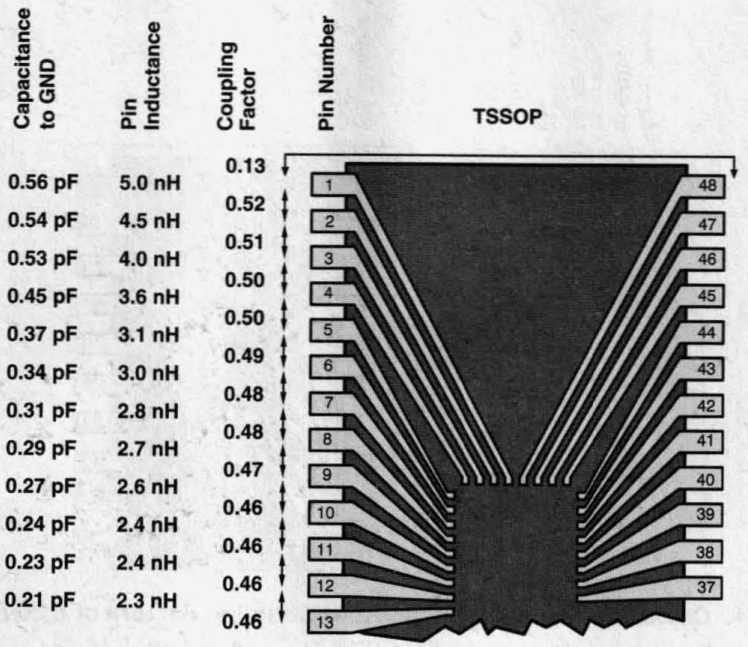


Figure 13. Capacitances, Inductances, and Coupling Factors of a 48-Pin TSSOP

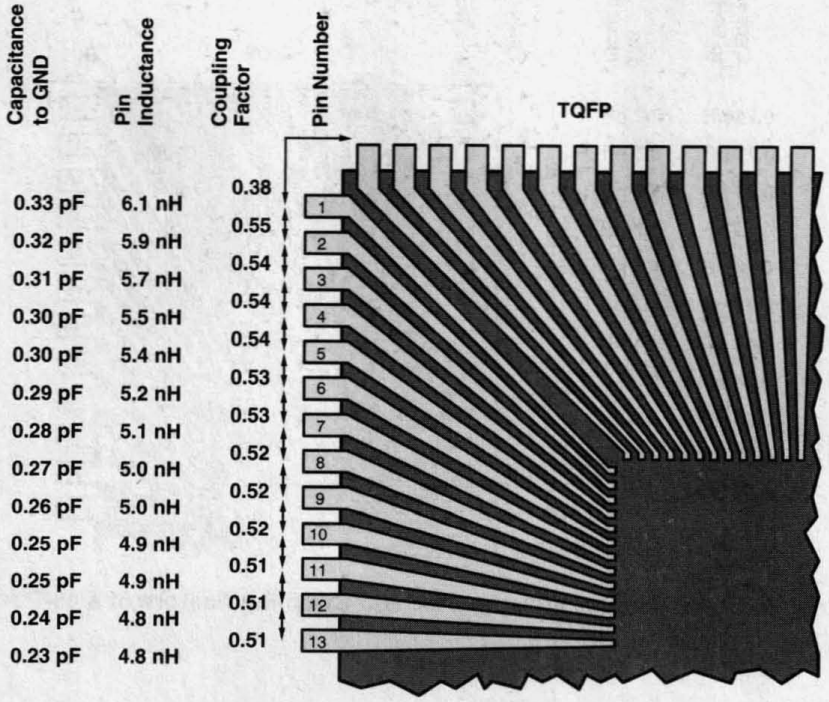


Figure 14. Capacitances, Inductances, and Coupling Factors of a 100-Pin TQFP

3.2 Simultaneous-Switching Behavior

The results of measurements of simultaneous-switching behavior are shown in Figures 15 through 21 for the seven package types under consideration. For this measurement, only one input is kept at low logic level, while all other inputs are switched simultaneously. The outputs of the drivers that are switching react with a certain delay to the changes at their inputs, while the unswitched input should remain undisturbed at low logic level. Crosstalk from the neighboring pins, together with a brief dip in the supply voltage (which cannot be measured externally) and a brief rise of the ground level at the chip (resulting from the inductance of the V_{CC} and GND connections), inevitably cause a reaction at the corresponding output. In such a case, the noise voltage that is generated must not exceed the threshold voltage level (about 1.4 V to 1.5 V) of the subsequent input. All seven package outlines have values from 0.16 V to 1.40 V and, therefore, lie below the threshold voltage level.

By far, the best results were obtained with the two 48-pin packages. This is primarily the result of the eight distributed GND pins for the 16 integrated drivers. Packages with the traditional corner-pin arrangement, such as the 20-pin package evaluated here, are provided with only one GND pin for eight driver circuits and, therefore, show inferior behavior. The large, 100-pin TQFP package has 12 GND pins for 36 drivers and, therefore, simultaneous-switching performance that is correspondingly worse than that of the 48-pin types. Some of the differences that have been measured can also be attributed to distributions between packages of the same type and are not necessarily the exclusive result of differences between package types.

The measured values of a given noise level are dependent on process technology, whereas, with BiCMOS and bipolar components, the threshold level normally will not be exceeded. With fast CMOS logic circuits, values of more than 2 V are the result of their steeper pulse slopes and, consequently, the greater effect of inductance with CMOS signals.

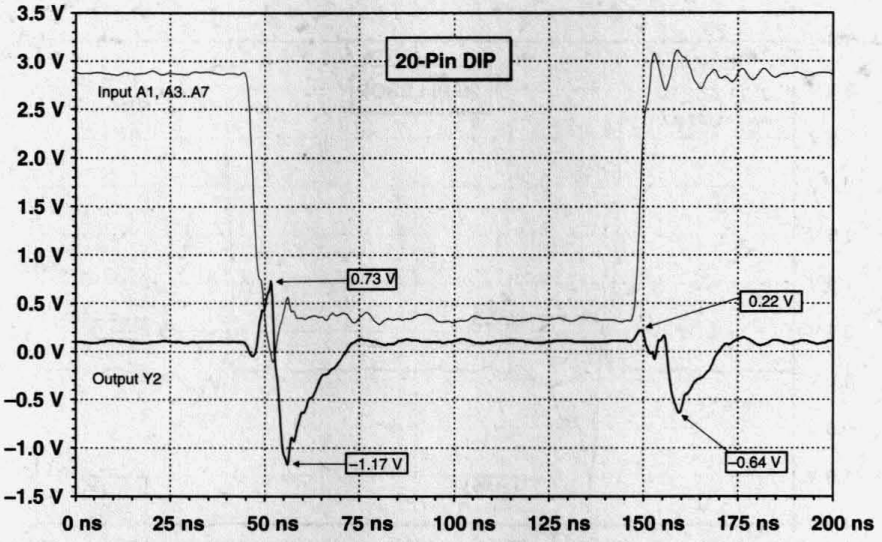


Figure 15. Simultaneous Switching of an SN74ABT245N (20-Pin DIP)

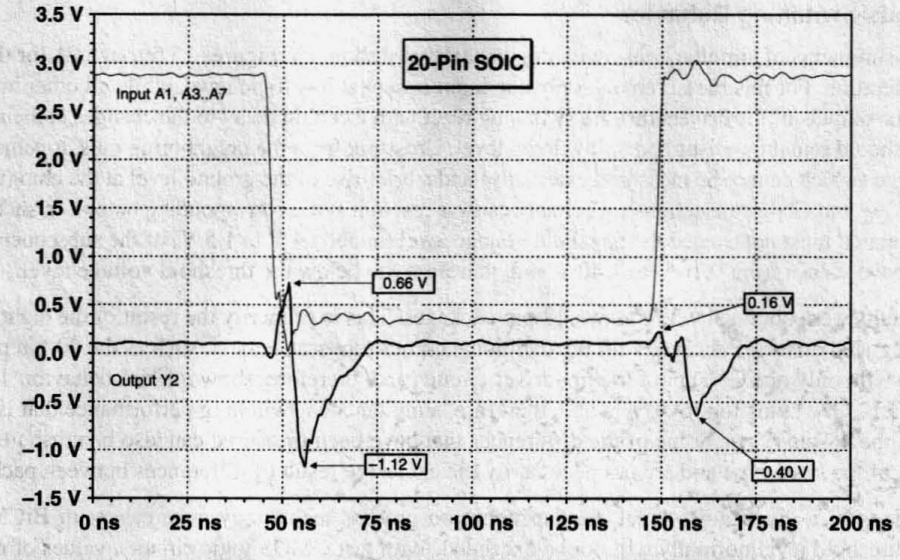


Figure 16. Simultaneous Switching of an SN74ABT245DW (20-Pin SOIC)

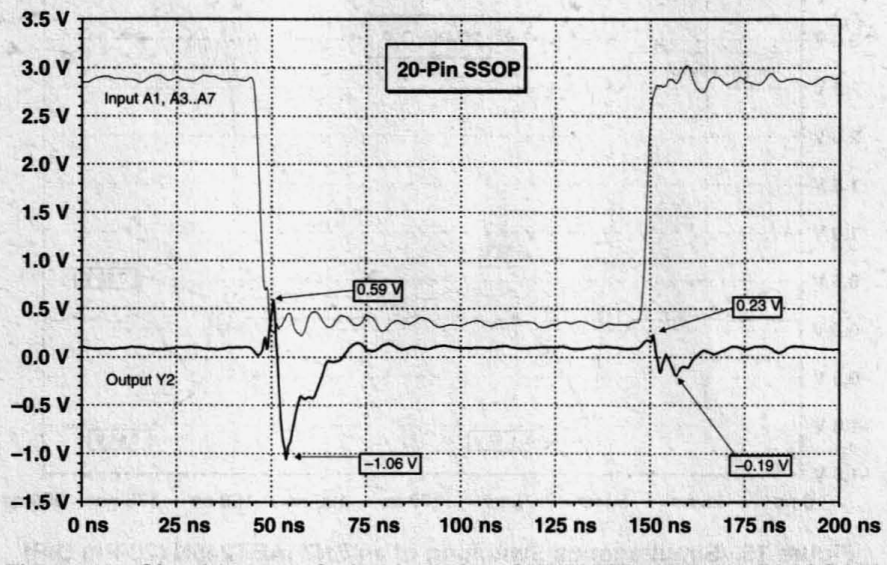


Figure 17. Simultaneous Switching of an SN74ABT245DB (20-Pin SSOP)

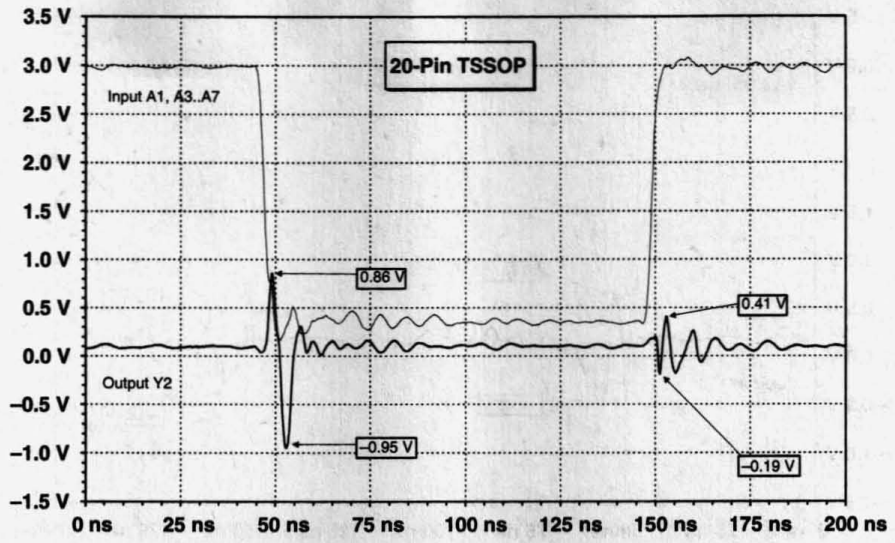


Figure 18. Simultaneous Switching of an SN74ABT245PW (20-Pin TSSOP)

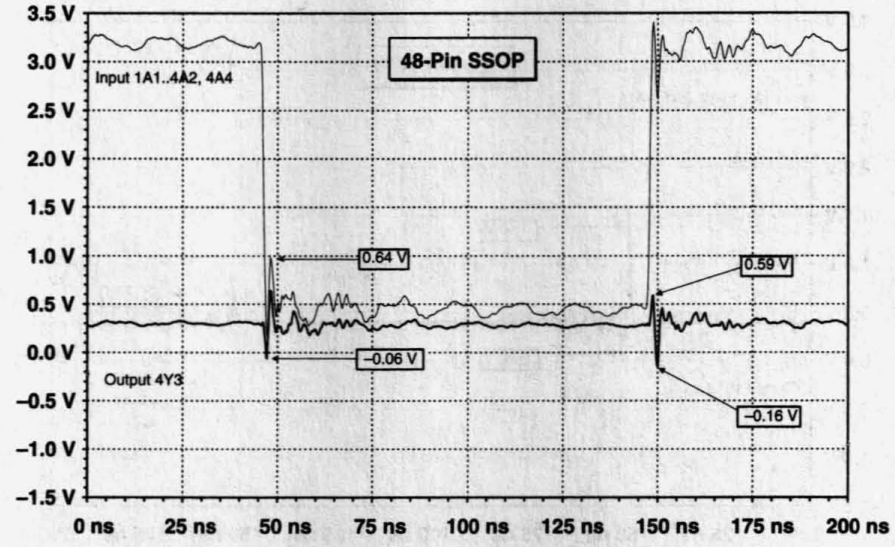


Figure 19. Simultaneous Switching of an SN74ABT16245DL (48-Pin SSOP)

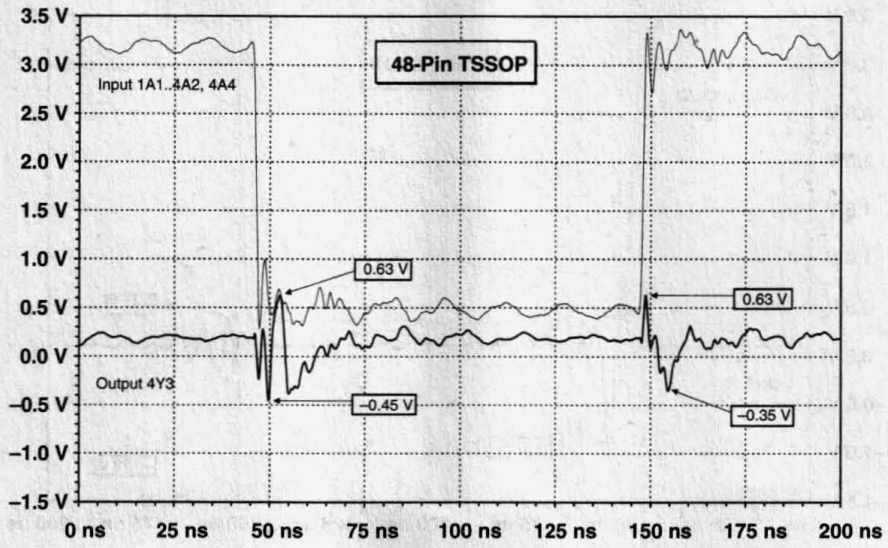


Figure 20. Simultaneous Switching of an SN74ABT16245DGG (48-Pin TSSOP)

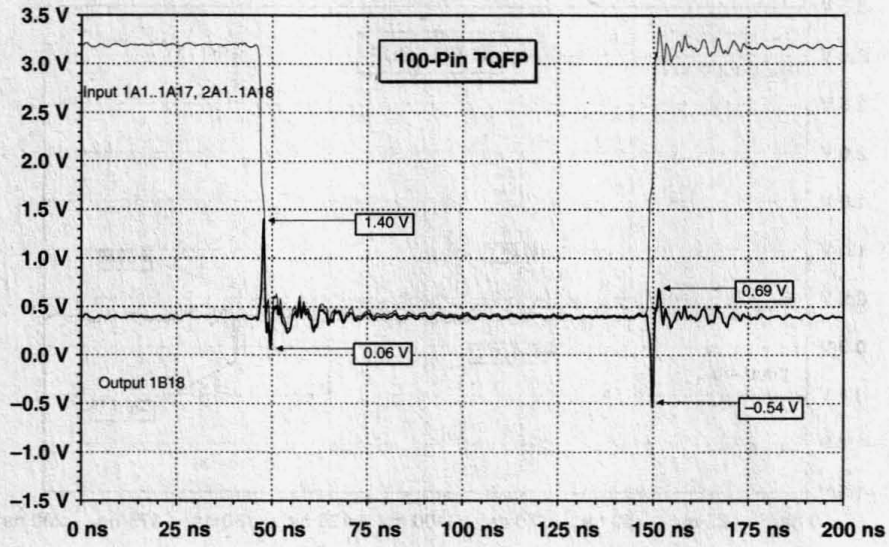


Figure 21. Simultaneous Switching of an SN74ABT32501PZ (100-Pin TQFP)

3.3 Increase of Delay Time

When several outputs are switched simultaneously, the form of the package can increase delay time. In this case, the inductances of the V_{CC} and GND connections are also factors. To evaluate the dependence of delay time increase on the various package outlines with electrical measurements, the delay time was measured as a function of the number of outputs being switched (Figures 22 and 23). The devices under test, in each case, were from the ABT family, namely SN74ABT245, SN74ABT16245, and SN74ABT32501. Their outputs were connected to a load of 50 pF and 500 Ω to GND. In both figures, the Y-axis direction represents the increase of delay time and the X-axis direction represents the number of switching outputs. The increase of delay time was chosen to eliminate the effect of component distributions at the absolute switching speed.

The absolute increase of the delay time with a rising edge is in the range of 0.5 ns to 0.9 ns. With a falling edge in the range of 0.8 ns to 1.5 ns, the measurements are at the limits of the accuracy that can be obtained with the setup and the instruments used. This explains the nonlinearities, as shown by the SSOP curve for falling edges.

The DIP package had the poorest performance with all measurements; the 20-pin SMD packages (surface-mount device) SOIC, SSOP, and TSSOP gave better results. The 48-pin and 100-pin packages, again, showed the best behavior of all.

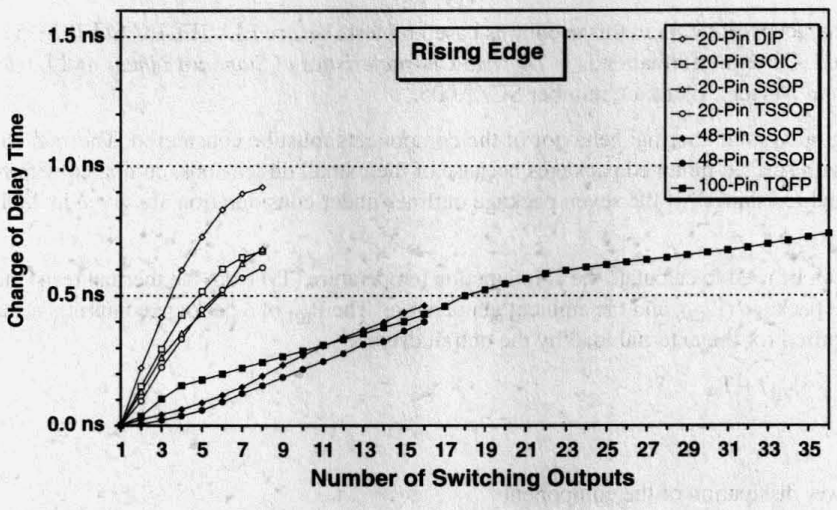


Figure 22. Delay Time of a Rising Edge as a Function of the Number of Simultaneously Switching Outputs (Measured With an SN74ABT245 in Seven Different Packages)

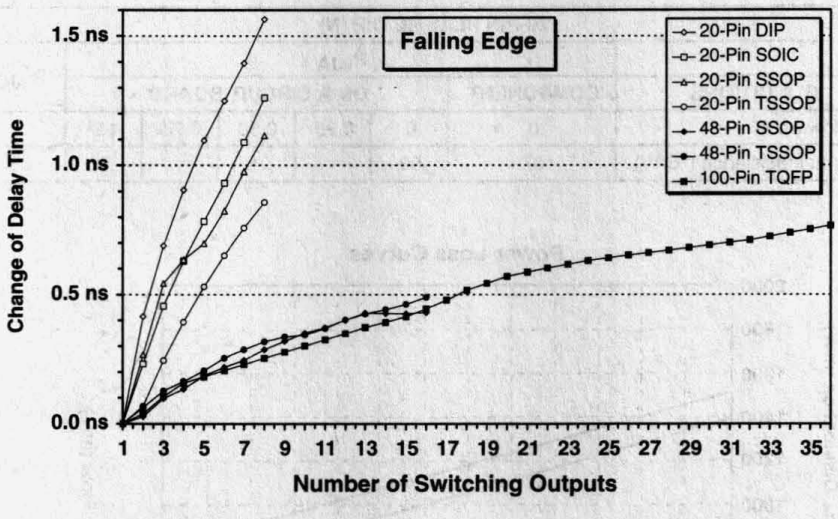


Figure 23. Delay Time of a Falling Edge as a Function of the Number of Simultaneously Switching Outputs (Measured With an SN74ABT245 in Seven Different Packages)

4 Thermal Characteristics

NOTE:

Thermal-characteristics data in this section is based on tests before EIA/JEDEC Std JESD51-3 was implemented. Current information is in *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices*, literature number SCZA005.

When developing a digital system, thermal behavior of the components must be considered. Thermal characteristics are of particular importance with surface-mounted packages because of their small dimensions, compared with relatively large DIP components. The thermal resistances of the seven package outlines under consideration are given in Tables 1 through 7 and Figures 24 through 30.

The expression below can be used to calculate the chip junction temperature (T_J) from the thermal resistance ($R_{\theta JA}$), the total power dissipation of the package (P_{tot}), and the ambient temperature. The P_{tot} of a package comprises a static part, a dynamic part, and the power required for the external load by the output drivers.

$$T_J = (R_{\theta JA} \times P_{tot}) + T_A \quad (1)$$

Where:

P_{tot} = total power dissipation of the component
$R_{\theta JA}$ = thermal resistance from the junction of the chip to the ambient air temperature
T_A = ambient air temperature
T_J = chip junction temperature

Table 1. Thermal Characteristics of a 20-Pin DIP

20-PIN PLASTIC DIP (N)							
	$R_{\theta JA}$						$R_{\theta JC}$
CONDITIONS	COMPONENT	ON A CIRCUIT BOARD					
Air flow (m/s)	0	0	0.25	0.50	0.75	1.0	
Thermal resistance (°C/W)	67	90		75			33

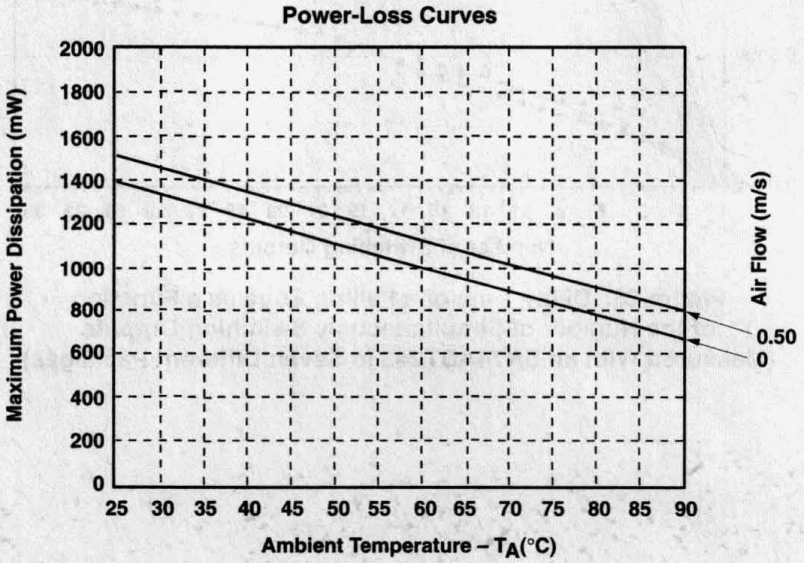


Figure 24. Thermal Characteristics of a 20-Pin DIP

Table 2. Thermal Characteristics of a 20-Pin SOIC

20-PIN SOIC (DW)							
	$R_{\theta JA}$						$R_{\theta JC}$
CONDITIONS	COMPONENT	ON A CIRCUIT BOARD					
Air flow (m/s)		0	0.25	0.50	0.75	1.0	
Thermal resistance (°C/W)	151	109	94	89	86	82	32

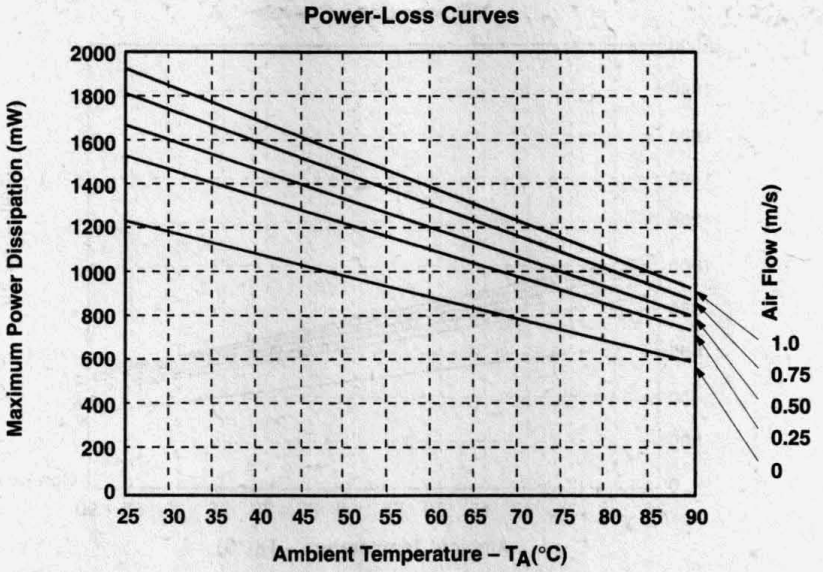


Figure 25. Thermal Characteristics of a 20-Pin SOIC

Table 3. Thermal Characteristics of a 20-Pin SSOP

20-PIN SSOP (DB)							
	$R_{\theta JA}$						$R_{\theta JC}$
CONDITIONS	COMPONENT	ON A CIRCUIT BOARD					
Air flow (m/s)	0	0	0.25	0.50	0.75	1.0	
Thermal resistance (°C/W)	203	143	135	128	123	119	45

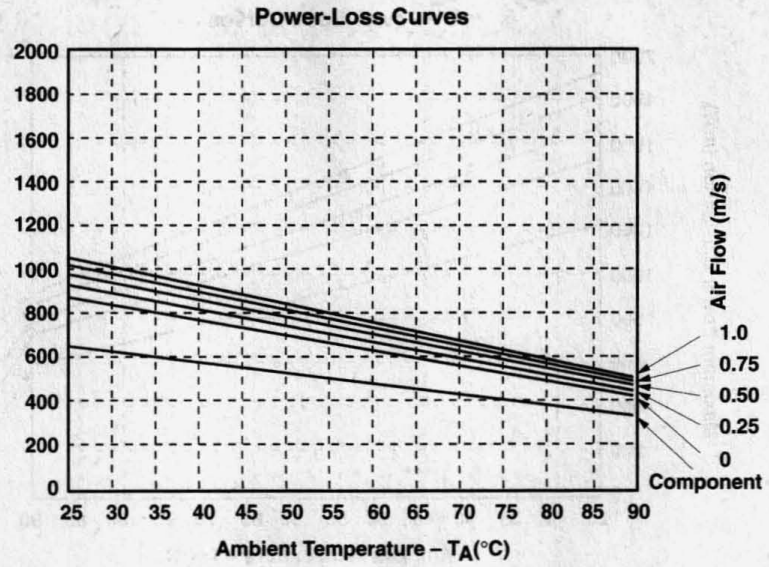


Figure 26. Thermal Characteristics of a 20-Pin SSOP

Table 4. Thermal Characteristics of a 20-Pin TSSOP

20-PIN TSSOP (PW)							
	$R_{\theta JA}$						$R_{\theta JC}$
CONDITIONS	COMPONENT	ON A CIRCUIT BOARD					
Air flow (m/s)	0	0	0.25	0.50	0.75	1.0	
Thermal resistance (°C/W)	239	155	138	133	130	128	34

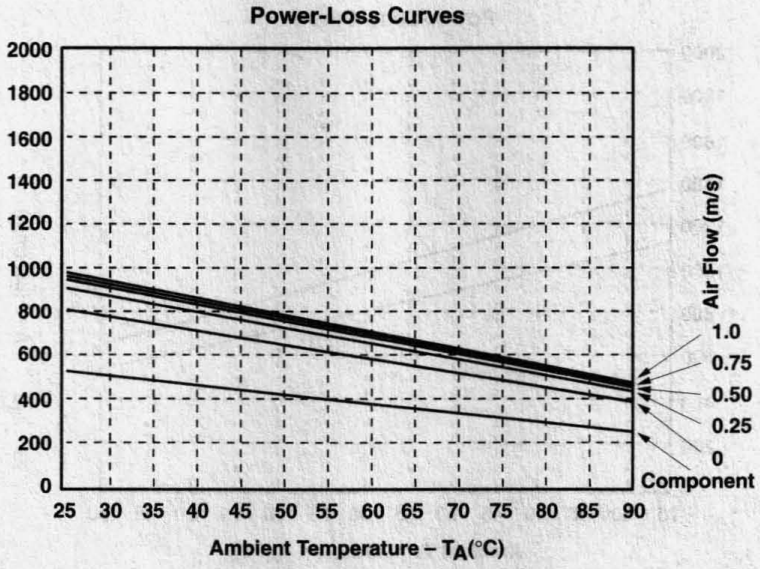


Figure 27. Thermal Characteristics of a 20-Pin TSSOP

Table 5. Thermal Characteristics of a 48-Pin SSOP

48-PIN SSOP (DL)							
	$R_{\theta JA}$						$R_{\theta JC}$
CONDITIONS	COMPONENT	ON A CIRCUIT BOARD					
Air flow (m/s)	0	0	0.25	0.50	0.75	1.0	
Thermal resistance (°C/W)		112		92			26

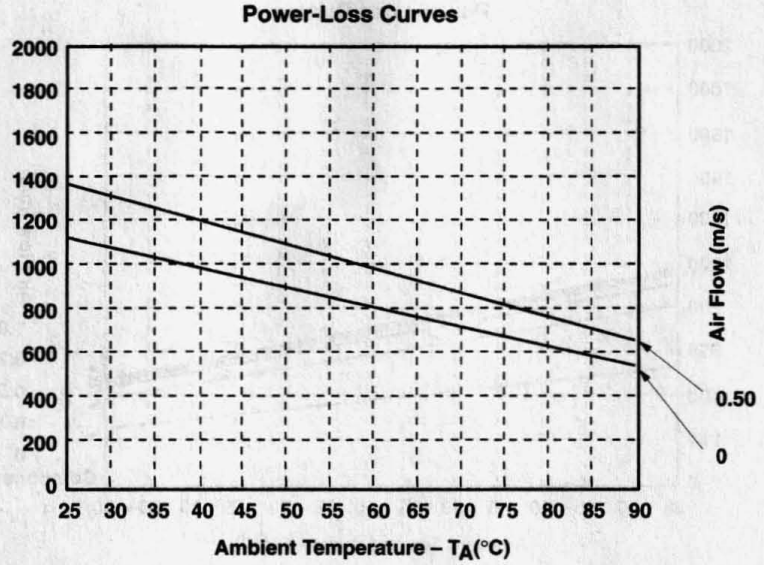


Figure 28. Thermal Characteristics of a 48-Pin SSOP

Table 6. Thermal Characteristics of a 48-Pin TSSOP

48-PIN TSSOP (DGG)							
	$R_{\theta JA}$						$R_{\theta JC}$
CONDITIONS	COMPONENT	ON A CIRCUIT BOARD					
Air flow (m/s)	0	0	0.25	0.50	0.75	1.0	
Thermal resistance (°C/W)	192	115	103	95	92	89	26

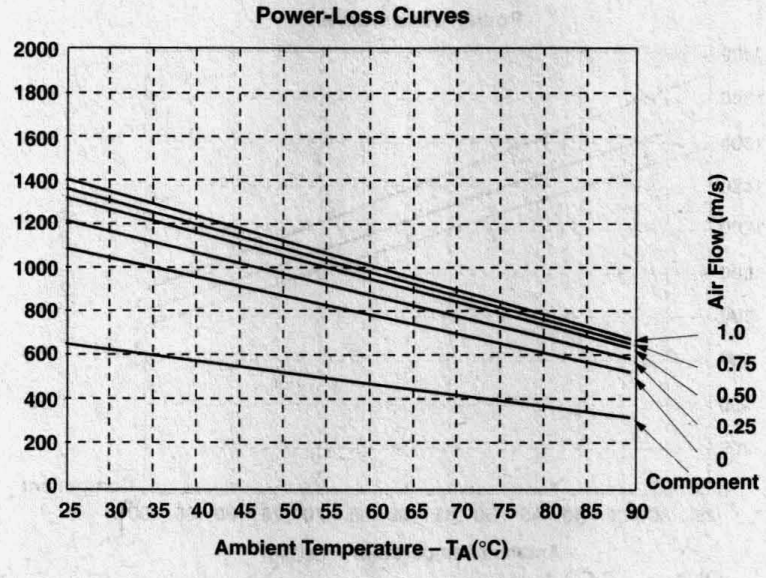


Figure 29. Thermal Characteristics of a 48-Pin TSSOP

Table 7. Thermal Characteristics of a 100-Pin TQFP

100-PIN TQFP (PZ)							
	$R_{\theta JA}$						$R_{\theta JC}$
CONDITIONS	COMPONENT	ON A CIRCUIT BOARD					
Air flow (m/s)	0	0	0.25	0.50	0.75	1.0	
Thermal resistance (°C/W)	79	72.7		65			11.6

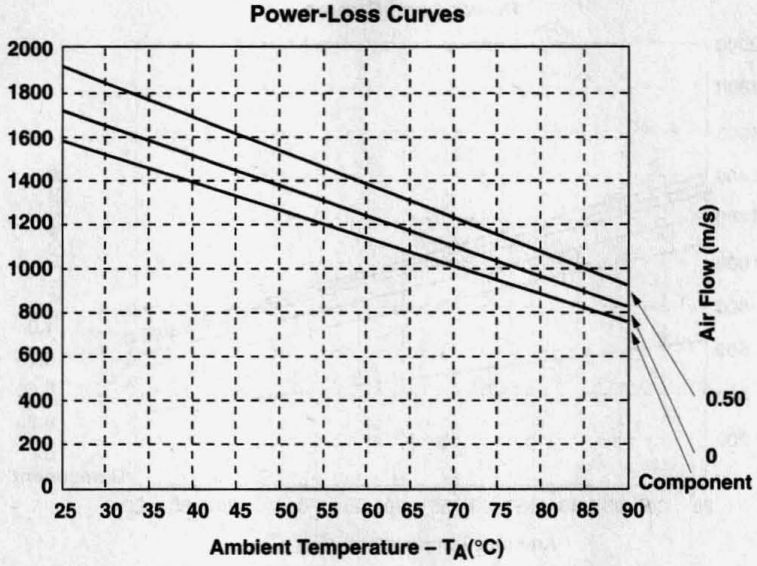


Figure 30. Thermal Characteristics of a 100-Pin TQFP

Recent Advancements in Bus-Interface Packaging and Processing

SCZA001A
February 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Introduction	**8–41**
Evolutions in Device Packaging	**8–41**
Thermal Impedances of Bus-Interface Packages	**8–43**
Evolutions in Device Processing	**8–43**
3.3-V Operation	8–44
Advanced Bus-Interface Solutions	**8–44**
Memory-Driver Usages for the SSOP	8–44
Bus-Interface Usages for the SSOP	8–46
Summary	**8–46**
References	**8–47**

List of Illustrations

Figure	*Title*	*Page*
1	Packaging/Processing Evolution	8–41
2	24-Pin Surface-Mount Comparison	8–42
3	High Pin-Count Comparison	8–42
4	Loaded Z_O Versus Distributed Capacitance	8–44
5	Typical t_{pd} Versus Capacitive Load	8–45
6	Typical t_{pd} Versus Capacitive Load	8–45
7	Typical t_{pd} Versus Capacitive Load	8–45
8	Typical Δt_{pd} Versus Outputs Switching	8–46

Introduction

Over the past several years, advancements in semiconductor processing have been combined with advanced surface-mount packages to offer solutions to board area concerns, as well as providing for increased system performance. Figure 1 compares the reduction of the package lead pitch to that of both CMOS and BiCMOS transistor geometries. This paper examines the different types of fine-pitch logic packages and the bus-interface solutions provided when they are combined with submicron semiconductor processes.

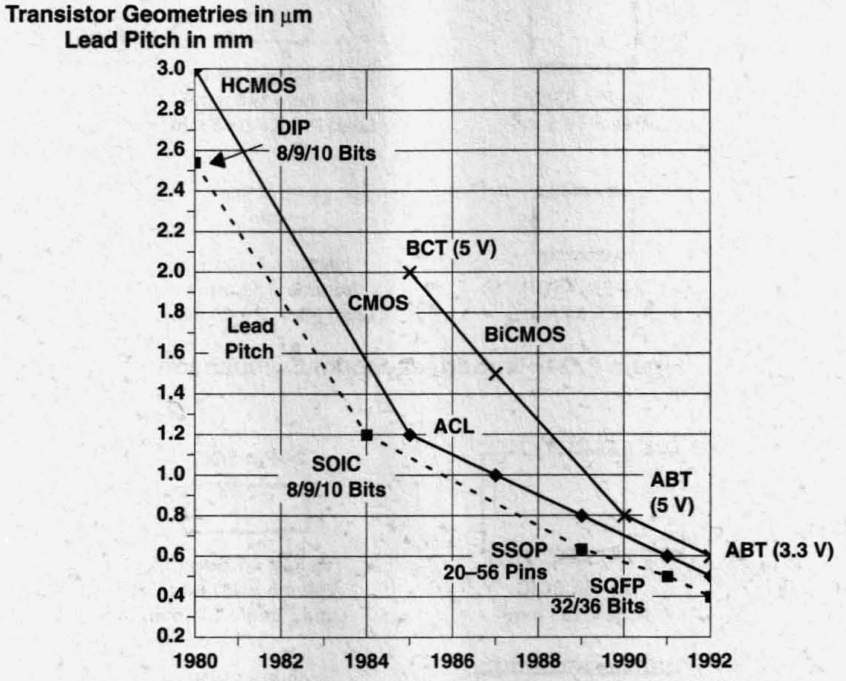


Figure 1. Packaging/Processing Evolution

Evolutions in Device Packaging

With the need for increased functionality in less board area has come the consolidation of much of the board's logic into more complex devices. In many cases, the discrete logic parts that remain, primarily interface/bus drivers, must occupy the board area left over after the higher level chips, i.e., microprocessor, ASICs, memory, etc., have been laid out. To meet this task, the standard small-outline integrated circuit (SOIC) has evolved in two distinct paths. One path reduces the package's area and volume (see Figure 2), and the other increases the bit density of the device (see Figure 3).

One method to increase bit density is to keep the number of pins constant while reducing both the lead pitch and package area. The 20-/24-pin SSOPs utilize a 0.65-mm lead pitch to achieve over a 50% reduction in area, compared to their standard SOIC counterparts. The package height is also reduced from 2.65 mm for the SOIC to 2 mm for the 20-/24-pin SSOPs. This reduction in volume translates into tighter board-to-board spacing, allowing for denser memory arrays.

The advent of the Personal Computer Memory Card International Association (PCMCIA) standard has required that the package height be reduced even further, thus spawning the thin small-outline package (TSOP). This package utilizes a 0.65-mm lead pitch and has a maximum device height of 1.1 mm. With an area of 59 mm^2, this package occupies 86% less volume than the standard 24-pin SOIC, facilitating the use of logic functions on these cards.

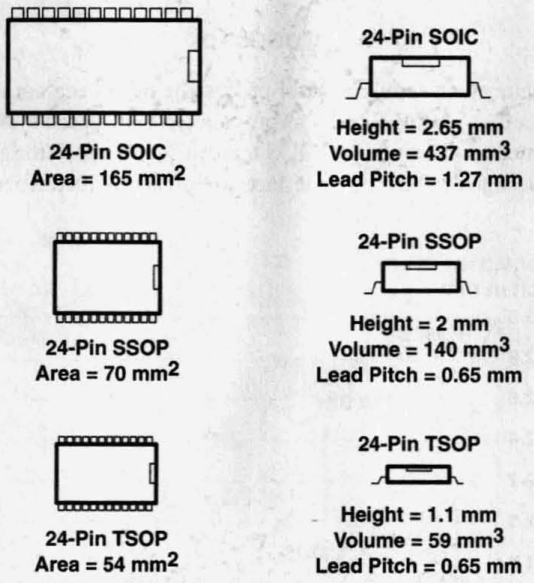


Figure 2. 24-Pin Surface-Mount Comparison

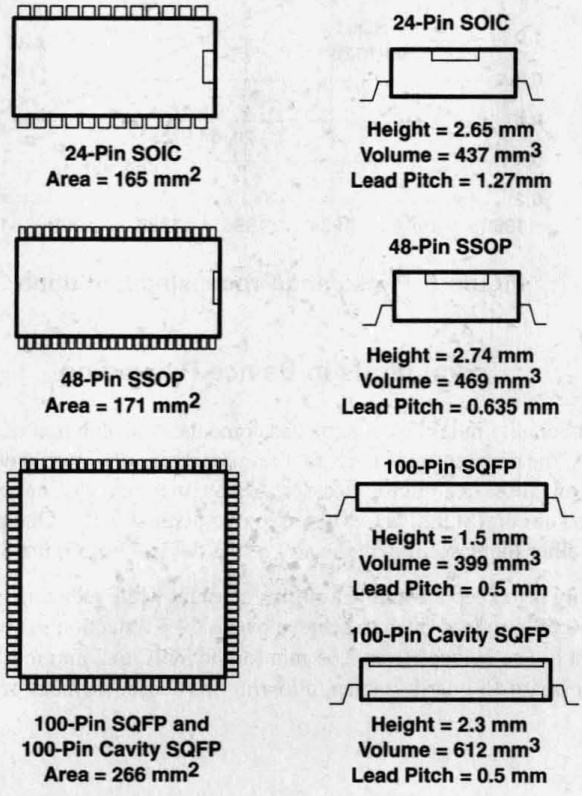


Figure 3. High Pin-Count Comparison

Another way to increase bit density is to reduce the lead pitch of the package. The 48-/56-pin shrink small-outline package (SSOP) halves the lead pitch of the SOIC package from 1.27 mm to 0.635 mm, allowing for twice the number of I/O pins in the same board area. The 8-, 9-, and 10-bit functions now become 16-, 18-, and 20-bit devices. The 100-pin shrink quad flat package (SQFP), along with the high-power cavity SQFP, further reduces the lead pitch to 0.5 mm. These packages double the bit density over the 48-pin SSOP with only a 50% increase in area. Both of these high pin-count packages allow for 32- and 36-bit logic functions, providing for efficient buffering of today's 32- and 64-bit bus widths.

Thermal Impedances of Bus-Interface Packages

By far the most common measure of package thermal performance is θ_{JA}, the thermal impedance measured (or modeled) from junction to ambient. θ_{JA} values are also the most subject to interpretation. Factors that can greatly influence the measurement and calculation of θ_{JA} are:

- Board mounted: yes/no?
- Traces: size, composition, thickness, and geometry
- Orientation: horizontal or vertical?
- Ambient: volume
- Proximity: any other surfaces near the device being measured?

In August 1996, the Electronics Industries Association released Standard EIA/JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. This standard provides guidelines for design of the test board used in taking thermal-impedance measurements of integrated-circuit packages. Prior to release of this standard, thermal-impedance data for similar packages varied greatly across the industry because of the use of different test-board designs. In particular, the characteristics of the test board have a dramatic impact on the measured θ_{JA}. As the industry begins using this standard test-board design, the variation in thermal-resistance data caused by the board should be minimized.

Key features of the standard test-board design are:

- Board thickness: 0.062 in.
- Board dimension: 3.0 in. × 4.5 in. for packages < 27.0 mm in length
- Board dimension: 4.0 in. × 4.5 in. for packages > 27.0 mm in length
- Trace thickness: 0.0028 in.
- Trace length: 0.984 in. (25.0 mm)

The ASL product group is now using the EIA/JESD51-3 standard to design the test boards used for thermal-impedance measurements. Also, the parameters outlined in this standard are used to set up thermal models. Thermal-impedance (θ_{JA}) data is now available for all ASL leaded surface-mount packages using the new JEDEC standard. Actual data has been generated on several ASL packages, and thermal models have been run on the remaining packages. Please refer to *Thermal Characteristics of SLL Packages and Devices*, literature number SCZA005, for additional information.

Evolutions in Device Processing

With the improvements to microprocessor clock rates and memory access times, bus-interface devices have become a larger percentage of the total bus cycle time. To keep pace with the need for faster logic, many semiconductor manufacturers are using submicron BiCMOS processes with shorter gate lengths and thinner gate oxide for device speed improvements. The reductions in transistor area result in less intrinsic capacitance, allowing faster internal gate delays, as well as lowering the output capacitance (C_{io}). With a lower C_{io}, ABT devices minimize their impact on system loading.

In a transmission-line environment, when the driver's edge rate is less than twice the line's propagation delay, distributed output loading has the effect of reducing the characteristic impedance (Z_O) of the transmission line. The higher the distributed capacitive load, the lower the apparent impedance, making it harder for the driver to switch the line on the incident wave. This well-known transmission-line loading equation is:

$$Z'_O = \frac{Z_O}{\sqrt{1 + \frac{C_d}{C_o}}} \quad (1)$$

Where:

Z_O = line's unloaded characteristic impedance, C_o
C_o = line's intrinsic capacitance per unit length
C_d = distributed capacitive load per unit length

Figure 4 shows how device output capacitance can lower line impedance, as in the case of a backplane. If the effects of the other board capacitance contributors — connectors, vias, and trace stubs — are assumed to be constant regardless of the device used, and thus ignored, a comparison of transmission-line loading between different technologies can be made.

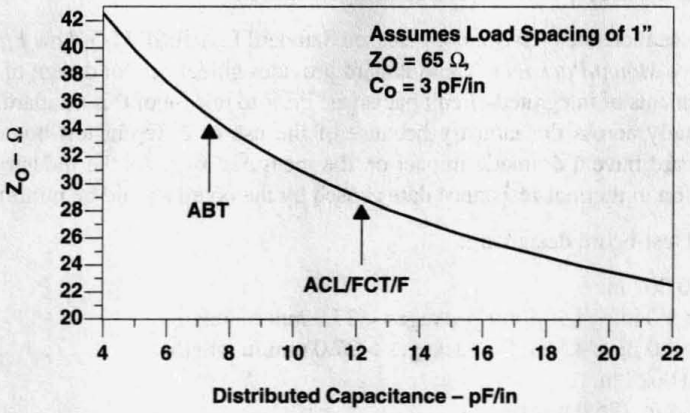


Figure 4. Loaded Z_O Versus Distributed Capacitance

3.3-V Operation

As process geometries move toward gate lengths of 0.5 µm and below, coupled with the desire for lower power consumption, 3.3-V operation becomes necessary. Because the migration to 3.3 V will be gradual, gated by the availability of semiconductor functions, the need for mixed signal-level operation will be critical for bus-interface devices. That is, the input and I/O pins will have input voltage levels up to 5.5 V without any conduction paths to V_{CC}. The outputs should also be capable of driving a standard 5-V backplane, which translates into drive currents of at least –15 mA of I_{OH} and 64 mA of I_{OL}.

Advanced Bus-Interface Solutions

Memory-Driver Usages for the SSOP

As noted previously, any of the SSOPs can be used as buffers in high-density memory arrays. In many instances, series damping termination is chosen due for its ease of implementation and power savings. Numerous logic devices are available that incorporate the series damping resistor on chip, as in the BCT2XXX series of products, simplifying this type of termination. When these parts are packaged in the 20-pin SSOP, as in the 'BCT2240DB, a tremendous board real-estate savings is realized over a discrete approach using external resistors and SOIC devices. For PCMCIA cards, the driver also must offer low-power consumption necessary for battery operation. The 'AC11244PW (TSOP package) can be used in these applications due to its low static-power CMOS characteristics.

Many times, when an output switches a large memory array, the capacitive load is localized in close proximity to the driver and can be treated as a simple lumped load. In these instances, it is useful to know how the propagation delay (t_{pd}) of the driver changes with the additional capacitive load. The change in the driver's t_{pd} is due to the interaction of its source impedance (R_{on}) with the capacitive load (C_L). Figures 5, 6, and 7 show these phenomena for the 'AC11244, 'BCT2240, 'ABT16244, and 'ABT32245 for both single- and multiple-outputs switching.

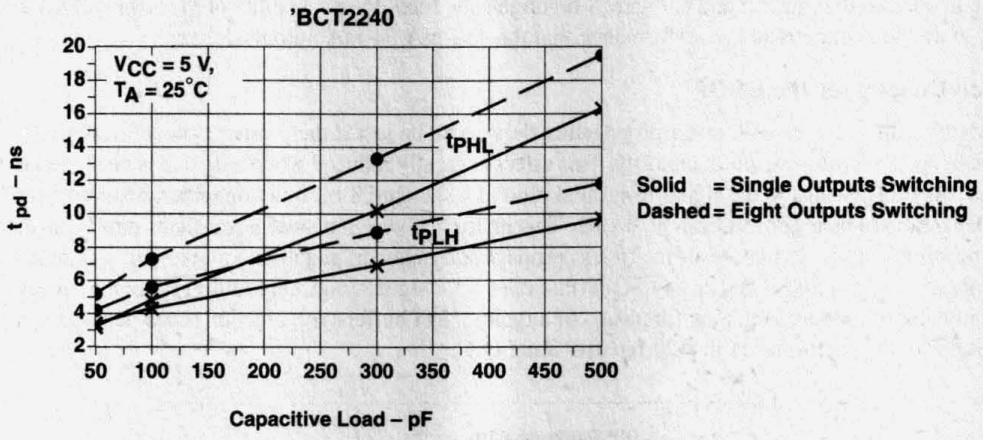


Figure 5. Typical t_{pd} Versus Capacitive Load

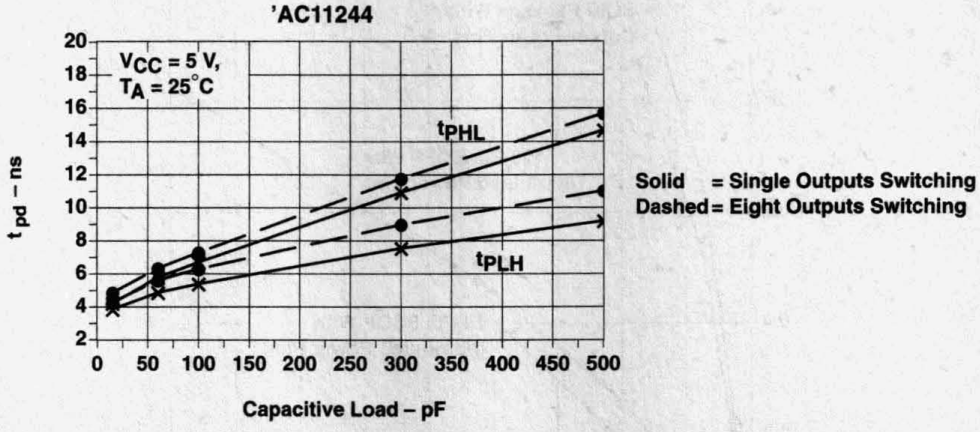


Figure 6. Typical t_{pd} Versus Capacitive Load

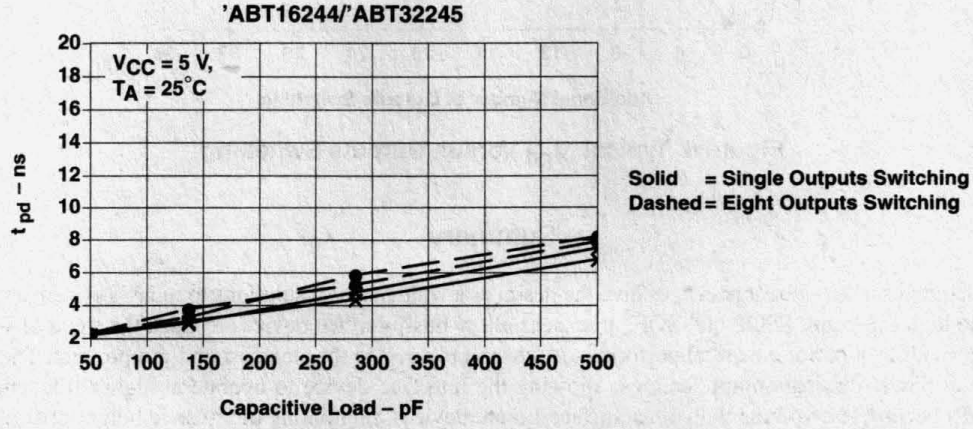


Figure 7. Typical t_{pd} Versus Capacitive Load

Figures 5 through 7 illustrate the effect that the output impedance of the driver has over t_{pd} degradation. Figure 5 shows that, even though the 'AC11244 has symmetrical high and low output-drive current ratings of 24 mA, t_{PHL} shows more degradation versus capacitive loading due to the graded turn on of the output to minimize simultaneous switching noise (ground bounce). Many advanced CMOS logic devices use this graded turn on, but not without the penalty of slower propagation delays at higher capacitive loads. Figure 6 shows a similar asymmetrical t_{PHL} performance, but now it is due to the inclusion of a 33-Ω series output resistor. In contrast to Figures 5 and 6, Figure 7 highlights the high-drive capability of the ABT16XXX and ABT32XXX devices, along with the symmetrical t_{pd} performance that the –32-mA/64-mA outputs deliver.

Bus-Interface Usages for the SSOP

The gains made by using devices with faster propagation delays can be lost if the propagation delay degrades when multiple outputs on a package are switched simultaneously. This effect is greatly reduced when a device is packaged in the 48-/56-pin SSOP, because this package allows the signal-to-ground ratio of a standard 8-bit function to be improved from 8:1 to 2:1, and the signal-to-V_{CC} ratio to be improved from 8:1 to 4:1. This multiple power-pin system translates into a quieter on-chip power system when multiple outputs switch, resulting in less propagation-delay degradation compared to a standard 8-bit function. The same is true for 100-pin SQFP and cavity SQFP that uses a 3:1 signal-to-ground ratio. Figure 8 compares the change in t_{pd} versus the number of outputs switching (in phase) of a typical '244 buffer-type function when packaged in a 48-pin SSOP and 100-pin SQFP to the performance in a 20-pin DIP and SOIC.

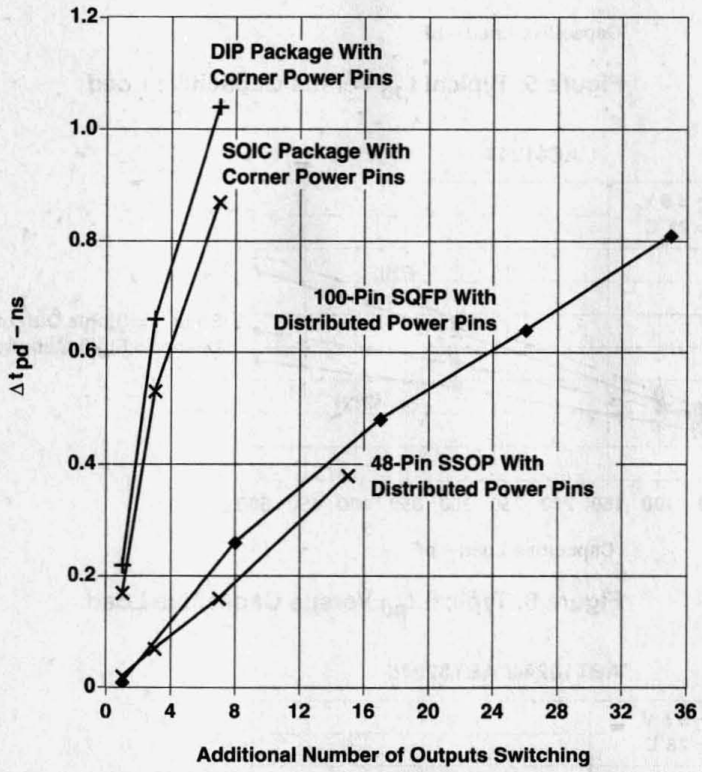


Figure 8. Typical Δt_{pd} Versus Outputs Switching

Summary

The various fine-pitch surface-mount packages give the designer a wide range of solutions to today's system area and volume constraints. The high pin-count SSOP and SQFP packages allow bus-interface devices to track the trend of wider data bus widths, while providing superior electrical performance when compared to the standard end-pin product. The cavity SQFP allows for higher power-dissipation applications, allowing the interface device to operate at higher frequencies. The low pin-count SSOPs occupy less volume than other surface-mount devices, facilitating their use in height-critical applications.

References

Transmission Lines

Advanced Schottky Family Applications, Texas Instruments Incorporated Advanced Schottky Data Book, 1986
Advanced CMOS Logic Designer's Handbook, Texas Instruments Incorporated, 1988

Power Dissipation

SSOP Designer's Handbook, Texas Instruments Incorporated, 1991

Thin Very Small-Outline Package (TVSOP)

SCBA009C
March 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title *Page*

Introduction **8–55**

TVSOP Dimensions **8–55**

Advanced System Logic (ASL) Packaging Trends **8–56**
ASL Line-Up of Similar Packages 8–56

The TVSOP Package and Its Development **8–58**
Description 8–58
JEDEC Registration 8–60
Symbolization 8–60

Printed-Circuit-Board Manufacture With the TVSOP **8–61**
Overview of Test Site Results 8–61
TVSOP Results From TI Custom Manufacturing Services 8–61
Pad Geometry Requirements 8–61
Stencil Geometry Requirements 8–62
Component Placement 8–62
Placement of TVSOP Devices (0.40-mm-Pitch Devices With Leads on Two Sides of the Body) 8–63
Quad Flat Pack (QFP) Devices 8–63
Raw-PCB and Stencil-Image Attributes 8–64
PCB Image Misregistration 8–64
The Stencil Process 8–65
Component-Placement Process 8–65
Infrared-Reflow Characteristics 8–65

TVSOP Results From AVEX Electronics **8–67**
Pad- and Stencil-Geometry Requirements 8–67
Assembly Process 8–68
Process Reflow Profile 8–69
Conclusion 8–69

Solder-Joint Reliability Study **8–69**
Temperature-Cycle Test 8–70
Test Implementation 8–70
Equipment List 8–70
Chamber Profile 8–71
Test Data 8–71
Definitions 8–71
References 8–71

Contents (continued)

Title	*Page*
TI Reference Information	**8–71**
Thermal Characteristics	8–71
Thermal Parameters	8–72
Thermal Measurements	8–72
TVSOP Power Dissipation and Thermal Impedance Characteristics	8–73
Power Calculation	8–77
CMOS	8–79
CMOS-Level Inputs	8–79
Transient Power Consumption	8–79
Capacitive-Load Power Consumption	8–79
TTL-Level Inputs	8–79
BiCMOS	8–80
Static Power	8–80
Dynamic Power	8–80
Electrical Characteristics	8–82
Electrical Parameters	8–82
Resistance	8–82
Capacitance	8–82
Inductance	8–82
TVSOP Electrical Data	8–83
Delivery of the TVSOP to TI Customers	**8–89**
Moisture Sensitivity of the TVSOP	8–89
Moisture-Sensitivity Qualification Data	8–90
Tape and Reel	8–90
Test Sockets	8–92
Acknowledgment	**8–93**

List of Illustrations

Figure	*Title*	*Page*
1	TVSOP Dimensions	8–55
2	Package Area Comparison	8–56
3	SSOP, TSSOP, and TVSOP Packages	8–57
4	14-Pin to 56-Pin TVSOP Package Dimensions	8–58
5	80-Pin and 100-Pin TVSOP Package Dimensions	8–59
6	Product Symbolization Format	8–60
7	Pad and Stencil Geometry	8–62
8	TVSOP Placement on PCBs	8–63
9	QFP Placement on PCBs	8–64
10	Defect Rate With 5-mil Stencil Thickness	8–66
11	Defect Rate With 6-mil Stencil Thickness	8–66
12	IR-Reflow Thermal Profile	8–67
13	TVSOP Pad and Stencil Geometry for IR Solder-Reflow Process	8–68
14	AVEX Process Flow for Mounting TVSOP Devices	8–68
15	Cross Section of a TVSOP Lead-to-Pad Solder Joint (Side View)	8–69
16	Cross Section of a TVSOP Lead-to-Pad Solder Joint (End View)	8–70
17	14-Pin TVSOP Derating Curves	8–73
18	16-Pin TVSOP Derating Curves	8–74
19	20-Pin TVSOP Derating Curves	8–74
20	24-Pin TVSOP Derating Curves	8–75
21	48-Pin TVSOP Derating Curves	8–75
22	56-Pin TVSOP Derating Curves	8–76
23	80-Pin TVSOP Derating Curves	8–76
24	100-Pin TVSOP Derating Curves	8–77
25	Input Waveform	8–78
26	TVSOP Package Inductance (14, 16, 20, 24, 48, and 56 Pins)	8–83
27	TVSOP Package Inductance (80 and 100 Pins)	8–84
28	TVSOP Package Capacitance (14, 16, 20, 24, 48, and 56 Pins)	8–84
29	TVSOP Package Capacitance (80 and 100 Pins)	8–85
30	TVSOP and SSOP Self-Inductance Comparison	8–85
31	Carrier and Cover-Tape Information for Reeled TVSOP Packages	8–91
32	Reel Dimensions	8–92

List of Tables

Table	*Title*	*Page*
1	TVSOP Dimensions By Pin Count	8–55
2	JEDEC Registration for TVSOP Packages	8–60
3	Product Symbolization	8–60
4	Characteristics of the ESS5-7RWC Test Chamber	8–71
5	Junction Temperature Versus Long-Term Reliability Comparison	8–72
6	JEDEC Thermal Test Board Specifications	8–72
7	C_{pd} Test Conditions With One- or Multiple-Bit Switching	8–78
8	Summary of TVSOP Electrical Data	8–86
9	14-Pin TVSOP Package Reliability Results	8–86
10	20-Pin TVSOP Package Reliability Results	8–87
11	48-Pin TVSOP Package Reliability Results	8–88
12	80-Pin TVSOP Package Reliability Results	8–89
13	TVSOP Floor Life	8–90
14	TVSOP Moisture-Sensitivity Levels	8–90
15	Available TVSOP Test Sockets	8–92

Introduction

Development of portable, lightweight, high-performance electronics products is driving the semiconductor industry toward smaller, thinner, and higher-density packages. Pricing pressures are encouraging strong efforts toward cost reduction.

Texas Instruments (TI) always has been a leader in IC packaging and is now introducing a new family of thin very small-outline packages (TVSOP) to support the component miniaturization requirements of the industry. The new TVSOP package family, in 14-, 16-, 20-, 24-, 48-, 56-, 80-, and 100-pin types, features a lead pitch of 0.40 mm (16 mil) and a device height meeting the 1.2-mm Personal Computer Memory Card International Association (PCMCIA) requirement. The TVSOP packages have received Joint Electronics Device Engineering Council (JEDEC) registration under semiconductor package standard MO-194.

This application report presents an overview of the TVSOP package family characteristics, including thermal, electrical, reliability, and moisture-sensitivity performance. Assembly and mounting guidelines for devices with 0.40-mm lead pitch are included.

TVSOP Dimensions

Figure 1 and Table 1 show TVSOP package dimensions.

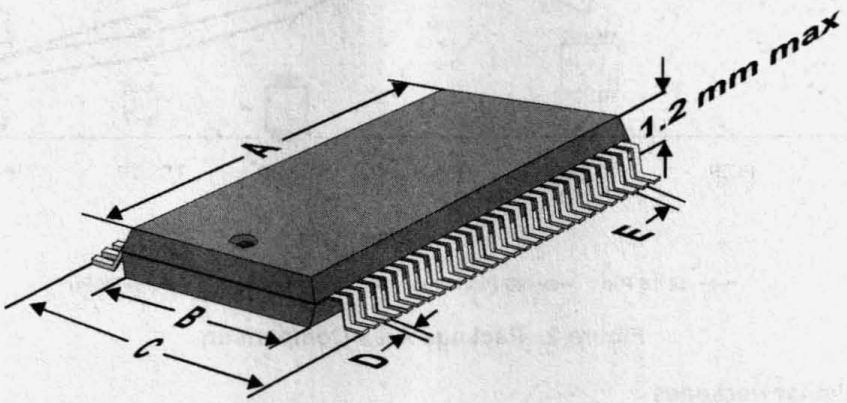


Figure 1. TVSOP Dimensions

Table 1. TVSOP Dimensions By Pin Count

TVSOP PACKAGE	TYPICAL DIMENSIONS (mm)					AREA (mm^2)	PERCENTAGE SMALLER THAN SSOP	PERCENTAGE SMALLER THAN TSSOP	PERCENTAGE SMALLER THAN TQFP
	A	B	C	D	E				
14-pin	3.60	4.40	6.40	0.18	0.40	23.00	52.4	29.3	
16-pin	3.60	4.40	6.40	0.18	0.40	23.00	52.4	29.3	
20-pin	5.00	4.40	6.40	0.18	0.40	32.00	43.0	24.0	
24-pin	5.00	4.40	6.40	0.18	0.40	32.00	50.0	34.0	
48-pin	9.80	4.40	6.40	0.18	0.40	63.00	61.9	38.0	
56-pin	11.3	4.40	6.40	0.18	0.40	72.30	62.2	36.0	
80-pin	17.0	6.10	8.10	0.18	0.40	137.8			30.0
100-pin	20.8	6.10	8.10	0.18	0.40	168.5			35.0

Advanced System Logic (ASL) Packaging Trends

Figure 2 shows how the TVSOP package follows the trend toward smaller and smaller surface-mount packages.

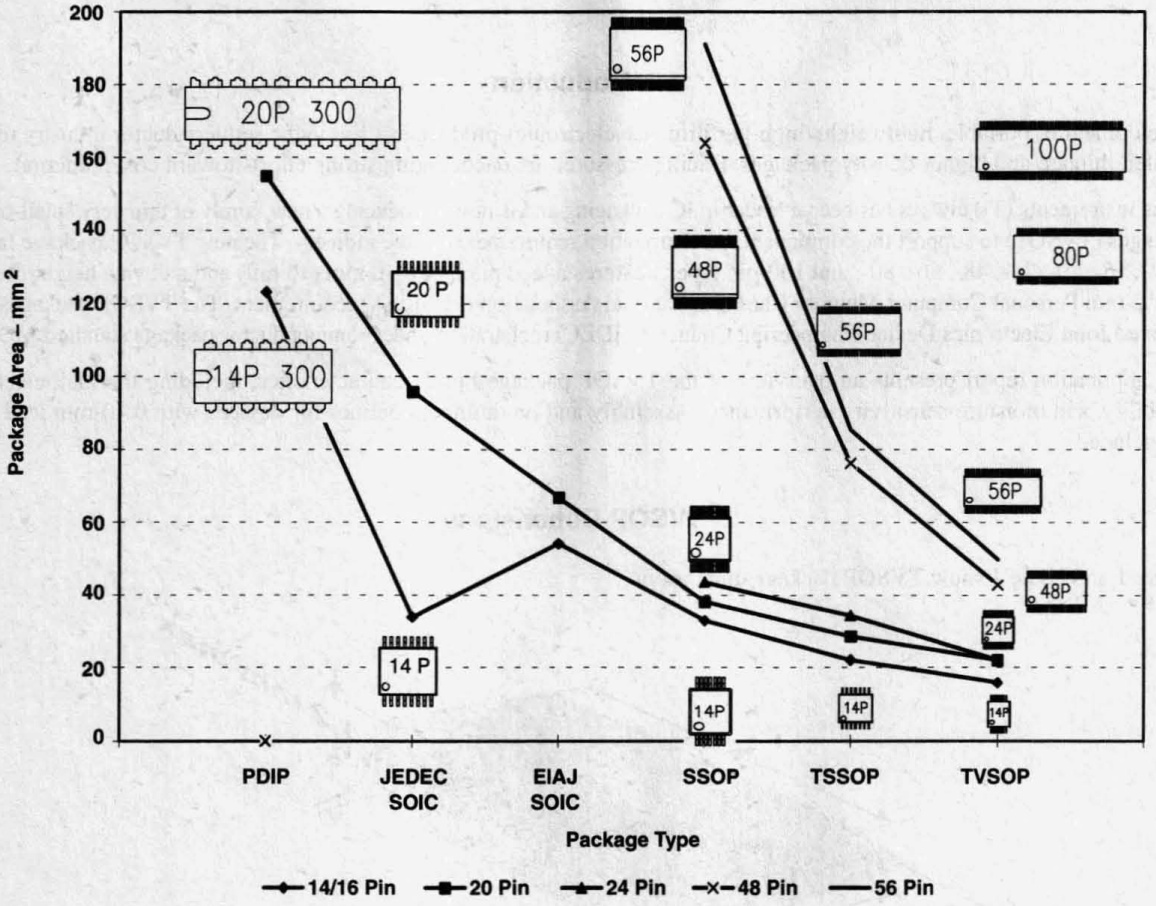
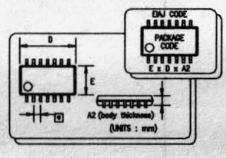


Figure 2. Package Area Comparison

ASL Line-Up of Similar Packages

Figure 3 shows TI's SSOP, TSSOP, and TVSOP surface-mount packages with pin pitches of 0.65 mm to 0.40 mm.

PACKAGE TYPE	EIAJ TYPE (mil)	PITCH ⓔ	14	16	20	24	48	56	100	80	JEDEC
SSOP	II 300	0.65	DB 5.3 x 6.2 x 1.8	DB 5.3 x 6.2 x 1.8	DB 5.3 x 7.2 x 1.8	DB 5.3 x 8.2 x 1.8					
	III 375	0.635					DL 7.5 x 15.9 x 2.3	DL 7.5x 18.4 x 2.3			
TSSOP	I 225	0.65	PW 4.4 x 5.0 x 1.0	PW 4.4 x 5.0 x 1.0	PW 4.4 x 6.5 x 1.0	PW 4.4 x 7.8 x 1.0					MO–153
	II 300	0.50					DGG 6.1 x 12.5 x 1.0	DGG 6.1 x 14.0 x 1.0			MO–153
TVSOP	I 225	0.40	DGV 4.4 x 3.6 x 1.0	DGV 4.4 x 3.6 x 1.0	DGV 4.4 x 5.0 x 1.0	DGV 4.4 x 5.0 x 1.0	DGV 4.4 x 9.7 x 1.0	DGV 4.4 x 11.3 x 1.0			MO–194
	II 300	0.40							DBB 6.1 x 17.0 x 1.0	DBB 6.1 x 20.8 x 1.0	MO–194



NOTE: The package outlines are not to scale.

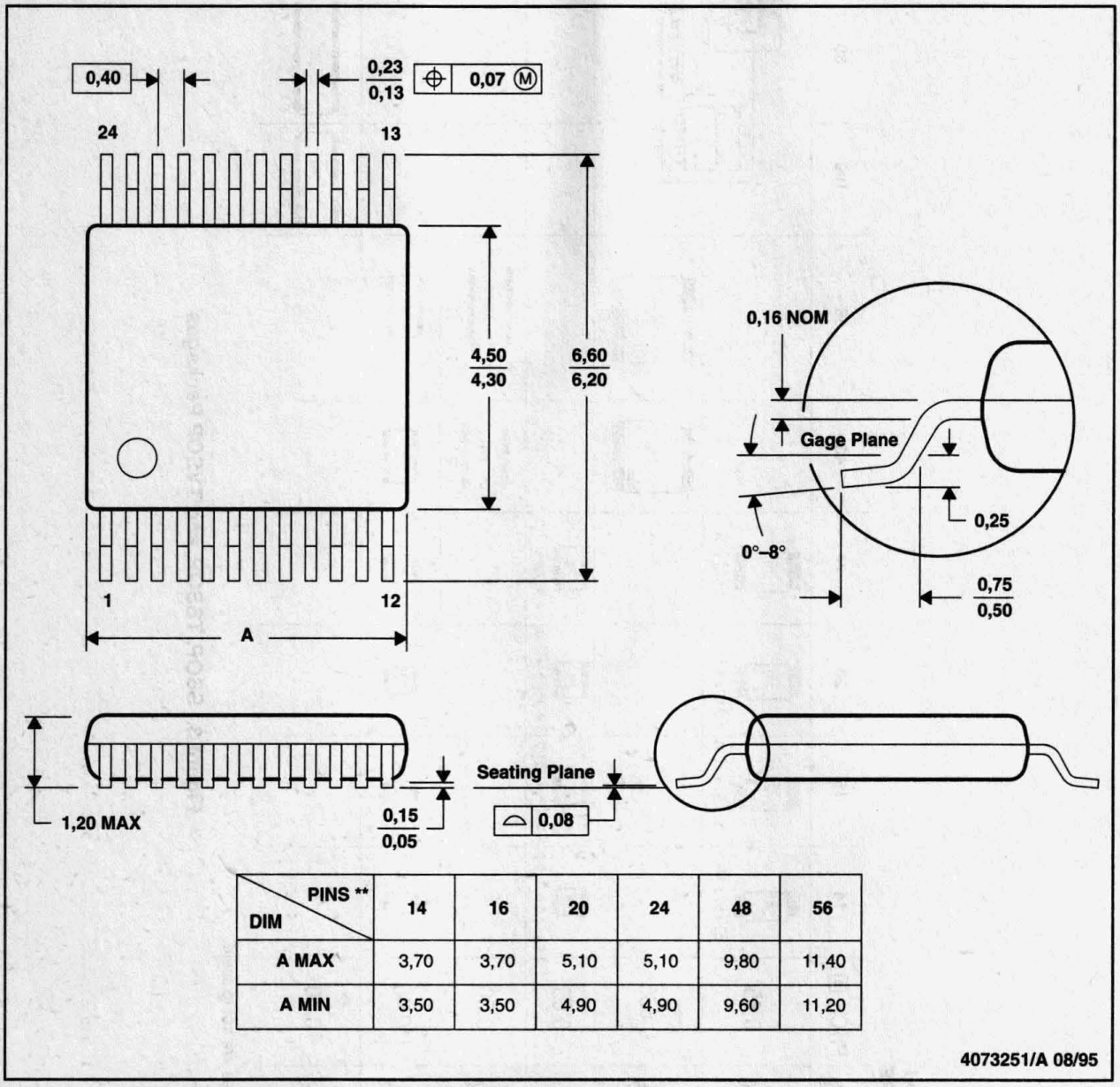
Figure 3. SSOP, TSSOP, and TVSOP Packages

The TVSOP Package and Its Development

Description

Figures 4 and 5 show the basic dimensions of the TVSOP package.

24 PIN SHOWN

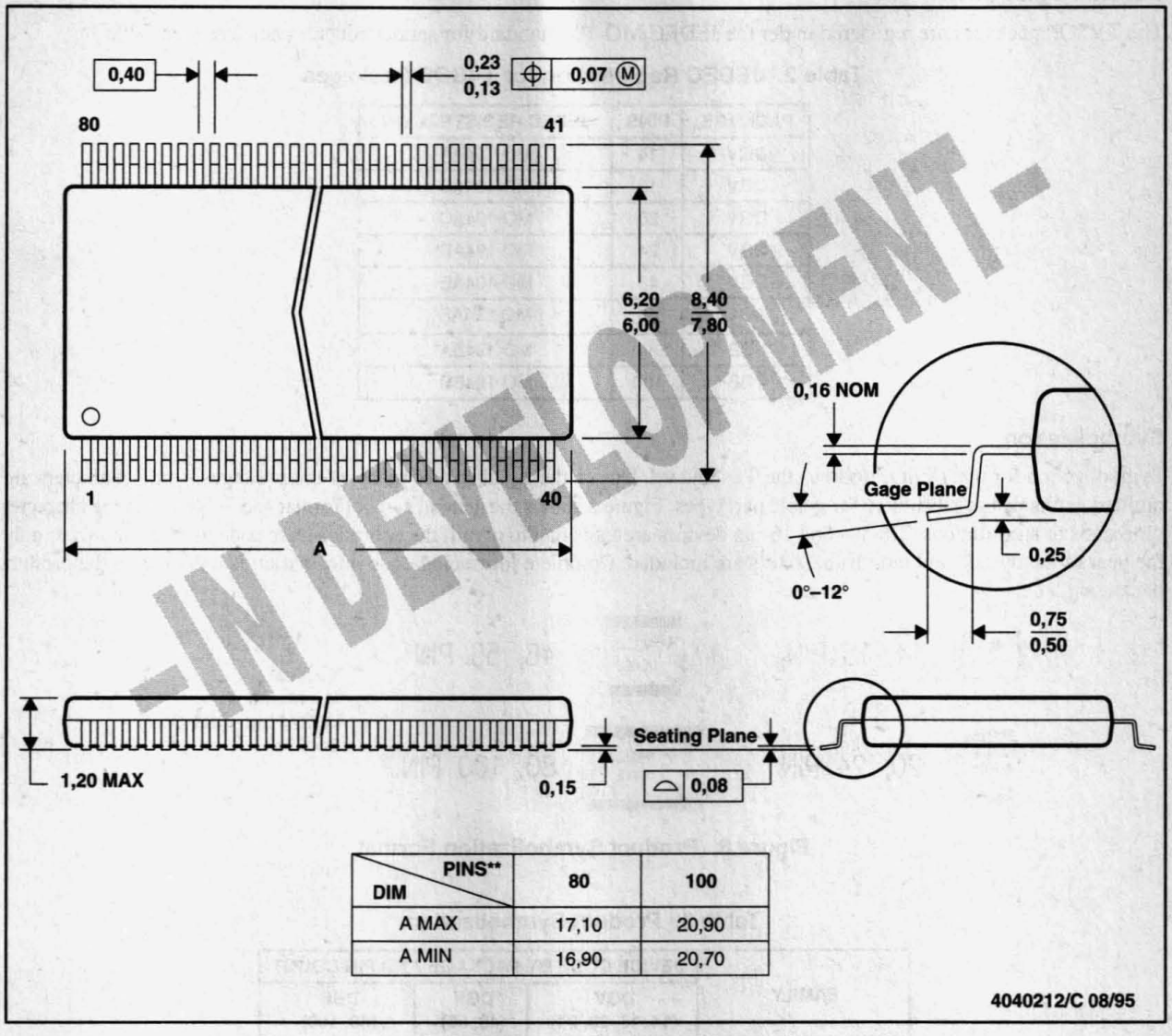


DIM \ PINS **	14	16	20	24	48	56
A MAX	3,70	3,70	5,10	5,10	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	9,60	11,20

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

Figure 4. 14-Pin to 56-Pin TVSOP Package Dimensions

80 PIN SHOWN



DIM \ PINS**	80	100
A MAX	17,10	20,90
A MIN	16,90	20,70

-IN DEVELOPMENT-

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.

Figure 5. 80-Pin and 100-Pin TVSOP Package Dimensions

JEDEC Registration

The TVSOP packages are registered under the JEDEC MO-194 standard for semiconductor packages (see Table 2).

Table 2. JEDEC Registration for TVSOP Packages

PACKAGE	PINS	JEDEC REGISTRATION
DGV	14	MO-194AA
DGV	16	MO-194AB
DGV	20	MO-194AC
DGV	24	MO-194AD
DGV	48	MO-194AE
DGV	56	MO-194AF
DBB	80	MO-194BA
DBB	100	MO-194BB

Symbolization

Symbolization for the TVSOP follows the TI standard. Due to the small size of many of the packages, some characters are omitted or characters substituted for whole part types. Figure 6 shows the general symbol format and Table 3 lists the character omissions or substitutions. The 14- and 16-pin devices are too small to permit the entire lot-trace code to be symbolized; only the year of the decade and month characters are included. Complete lot-tracing code information is included on the product packaging labels.

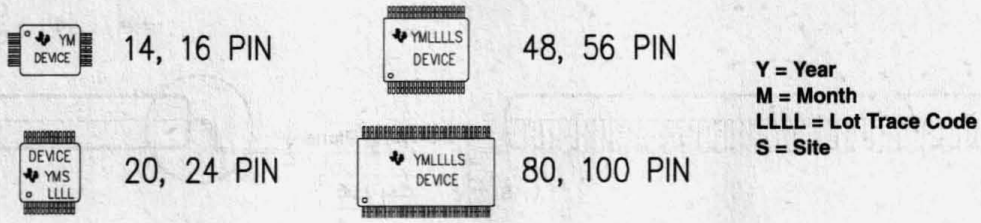


Figure 6. Product Symbolization Format

Table 3. Product Symbolization

FAMILY	DEVICE CODE BY PACKAGE AND PIN COUNT		
	DGV (14, 16, 20, 24)	DGV (48, 56)	DBB (80, 100)
SN74ALVCH16xxx	N/A	VHxxx	ALVCH16xxx
SN74ALVCHG16xxx	N/A	VGxxx	ALVCHG16xxx
SN74ABTxxx	ABxxx	N/A	N/A
SN74ABTHxxx	AKxxx	N/A	N/A
SN74ABT16xxx	N/A	AHxxx	N/A
SN74ABTH16xxx	N/A	AMxxx	N/A
SN74AHCxxx	HAxxx	N/A	N/A
SN74AHCTxxx	HBxxx	N/A	N/A
SN74CBTD3xxx	CCxxx	N/A	N/A
SN74CBT16xxx	N/A	CYxxx	CBT16xxx
SN74LVCxxx	LCxxx	N/A	N/A
SN74LVCHxxx	LCHxxx	N/A	N/A
SN74LVC16xxx	N/A	LDxxx	N/A
SN74LVCH16xxx	N/A	LDHxxx	N/A

NOTE: Please contact your nearest TI Sales Office or authorized distributor for specific device and type availability.

Printed-Circuit-Board Manufacture With the TVSOP

Overview of Test Site Results

ASL Packaging Engineering has been working in cooperation with Solectron, Texas (formerly TI Custom Manufacturing Services, Austin) and AVEX Electronics Inc. to develop printed-circuit-board (PCB) assembly-process guidelines for ultra-fine-pitch packages in high-volume manufacturing.

The majority of defects encountered in board assembly with fine-pitch packages are caused by solder bridging, open circuits, or improper device placement. Proper lead planarity and the absence of bent leads are essential to minimize assembly-mounting defects. Components with poor co-planarity require more solder paste to obtain a good solder joint. The increased volume of solder paste can cause bridging. All board-mounted components must be selected carefully based on the lead foot specifications provided by component suppliers. Lead co-planarity data are constantly monitored on TI TVSOP packages to ensure that all units fall within the JEDEC co-planarity specifications of less than 0.08 mm. Inaccurate device placement, the last of the defect issues, is a function of pick-and-place equipment capability.

Two major potential applications for TVSOP 0.40-mm packages were addressed during the assembly process development project: standard PCB boards (8 in. × 16 in.) and standard PCMCIA cards. Many factors can affect board performance (equipment, environment, component and board quality, etc.), therefore, the guidelines presented herein are primarily intended to give manufacturers and designers useful information that resulted from our package-development work.

TVSOP Results From TI Custom Manufacturing Services

TI conducted evaluations to establish the design and processing requirements, along with the limitation in applying the TVSOP series of 0.40-mm- (16 mil) pitch devices. Footprint-geometry, stencil, placement, and surface-mount technology (SMT) processing guidelines are needed to minimize the solder-defect rate of indiscriminate use of 0.40-mm-pitch devices in designs.

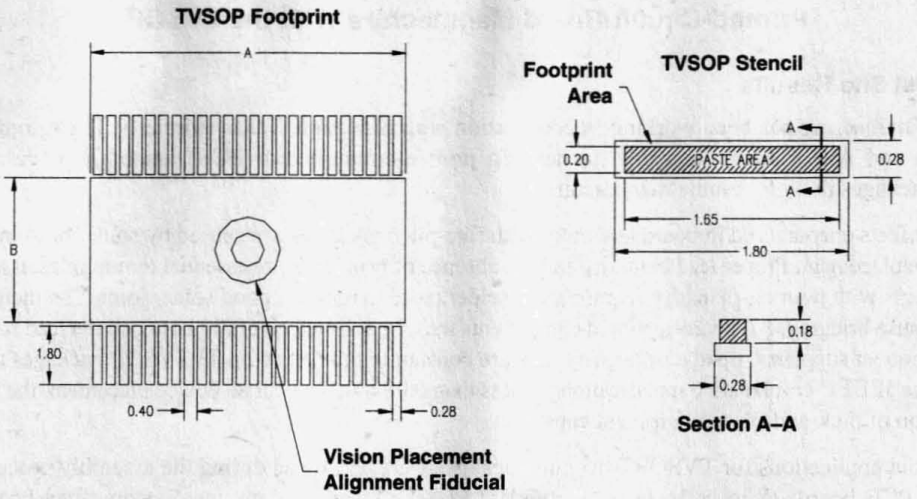
Each SMT assembly-process defect rate is unique to the demands of 0.40-mm-pitch devices on the assembly process. Equipment accuracy, repeatability, and process capability all play large roles in the resultant defect rate. Therefore, differences in the magnitudes of the rates achievable through implementation of the recommended guidelines have been quantified.

Pad Geometry Requirements

The following dimensional requirements for the 0.40-mm-pitch terminal pad are recommended (see Figure 7):

Terminal pad length	1.8 mm, 0.070 in.
Terminal pad width	0.28 mm, 0.011 in.
Terminal pad pitch	0.4 mm, 0.0157 in.
Gerber Tru Position	2–4 format minimum
Pad finish	Entek™

Conclusion: The pad geometry and finish are very important to the assembly-defect rate for widely spaced 0.40-mm-pitch devices.



See table below for dimension A and B

All dimensions in mm

	PIN COUNT					
	14/16	**20/24**	**48**	**56**	**80**	**100**
Dimension A	3.6	5.0	9.8	11.3	17.0	20.8
Dimension B	4.4	4.4	4.4	4.4	6.1	6.1

Figure 7. Pad and Stencil Geometry

Stencil Geometry Requirements

We recommend a single-level, laser-cut, electro-polished stainless steel, 0.006-inch-thick stencil for any product that has both PLCC and 0.40-mm-pitch devices. PCBs without PLCC devices could use a 0.005-in. stencil. However, other 50-mil-pitch devices will trend toward insufficient solder volume.

	PLCC AND TVSOP	TVSOP ONLY
Stencil opening length	0.065 in.	0.065 in.
Stencil opening width	0.008 in.	0.008 in.
Stencil thickness	0.006 in.	0.005 in.
Gerber 7 position	2–4 format minimum	

Conclusion: Stencil thickness has the greatest influence on defect rates. Our experience shows that a small increase in the solder-short defect rate of 0.40-mm-pitch devices is preferable to using a thinner stencil that produces difficult-to-detect opens or solder insufficiencies.

Component Placement

All 0.40-mm-pitch device defect rates (shorts) are very sensitive to the lead orientation with respect to the radial distance the devices are from the stencil alignment point (usually the center of the PCB). Defect rates of widely-spaced TVSOP devices can be reduced by orders of magnitude by placing the device with its leads parallel to the raw PCB image-stretch axis. Each PCB and stencil has an image positional accuracy that usually exhibits an inch-per-inches misregistration. Also, stencils have an image-registration accuracy and tend to change dimensionally with the number of print cycles.

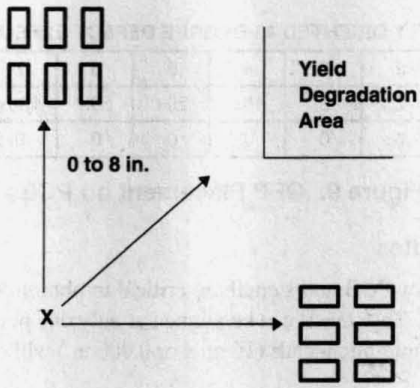
Placement of TVSOP Devices (0.40-mm-Pitch Devices With Leads on Two Sides of the Body)

The previously stated dimensional considerations yield the following optimum placement practices. This information applies to any pin count of a 0.40-mm-pitch small-outline package.

Maximum assembly yields for components placed more than 8 in. from the center of the PCB (stencil alignment point) can be achieved by orienting the leads parallel to the PCB expansion axes, with the longest distance from the center point. In areas where the distance from the alignment point is excessive (yield degradation area), the defect rate will climb rapidly without special placement guidelines.

Devices outside the 8-in. area must have their leads positioned as shown in Figure 8 or assembly yields will degrade significantly.

Devices in the yield degradation area of Figure 8 should be avoided. If unavoidable, the leads should be oriented at 45 degrees to the PCB expansion axes to avoid excessive defects.



CORRECTLY ORIENTED DEFECT EXPECTATIONS

Inches from center	1	2	3	4	5	6	7	8	9	10	11
Yield degradation	0	0	0	0	0	0	1x	2x	4x	10x	30x

NOTE: Magnitude of 4x denotes 4 times the defect rate.

Figure 8. TVSOP Placement on PCBs

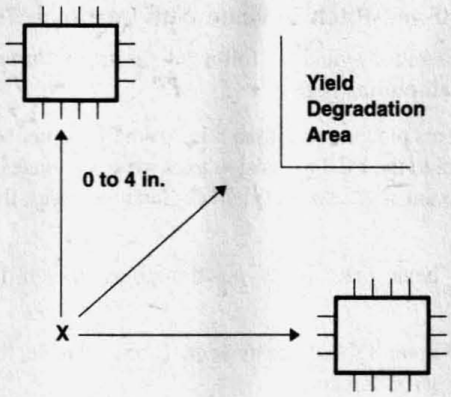
Quad Flat Pack (QFP) Devices

This information applies to any pin count 0.40-mm-pitch quad flat pack (leads out all sides) devices.

QFP devices cannot avoid defects by changing their lead orientation from 0 to 90 degrees. There is the added complication of stenciling inconsistency with leads in both directions.

Optimum assembly yields of a QFP device are realized when the component is rotated 45 degrees from the PCB expansion axis. Significant defects occurred at all distances more than 4 in. from the stencil alignment point with normally oriented QFPs (see Figure 9).

In summary, placement of any 0.40-mm-pitch device has the second greatest influence over the defect rate.



CORRECTLY ORIENTED 45-DEGREE DEFECT EXPECTATIONS

Inches from center	1	2	3	4	5	6	7	8	9	10	11
0–90° orientation	0	0	0	10x	20x	50x	100x	250x	500x		
45° orientation	0	0	0	0	0	0	0	0	10x	20x	100x

Figure 9. QFP Placement on PCBs

Raw-PCB and Stencil-Image Attributes

The image reproduction accuracy of the raw PCB and stencil are critical in obtaining and sustaining a satisfactory defect rate with widely spaced 0.40-mm-pitch devices. The stencil can be aligned at only one point on the PCB image. Any misregistration approaching a full space between the 0.40-mm-pitch leads (16 mils or 0.006 in.) will cause shorts beginning at tens of thousands of parts per million.

Typical commercial PCB fabrication processes have not comprehended the need for very accurate and repeatable images on the active side of the PCBs. Research indicates that the specifications and requirements for image registration are not well defined. The old *hole true-position registration* plays very little part in the sub-0.50-mm-pitch assembly process. Some points of reference were obtained. One supplier suggests an image registration accuracy of ±0.002 in. (0.00011 in. per inch) over a 24-in. by 18-in. fabrication panel. This experiment substantiated that level of registration misalignment.

PCB Image Misregistration

The following data summarizes the estimated maximum misregistration allowed:

TEST BOARD DIMENSIONS	MEAN X	3 SIGMA X	MEAN Y	3 SIGMA Y	INCH PER INCHES
15 in.	0.0018	0.0024			0.00012
6 in.			0.00136	0.00138	0.00025

Conclusion: Use of widely-spaced 0.40-mm-pitch devices requires an image-registration-tolerance specification and lot testing at the supplier to ensure compliance. Exceeding 0.00015 in. per inch in registration accuracy will begin to degrade the defect rate.

The stencil image registration is just as important as the PCB. It has been our experience that stencil images are as difficult to control as the PCB image. Also, the image moves with the number of print cycles. The movement is of limited predictability.

Conclusion: As with the PCB, every stencil-image registration must be specified and verified when first purchased. Maximum misregistration should be ±0.002 in. over 13 inches (0.00015 in. per inch). If the dimensional registration of the board and stencil are at alignment extremes, it is prudent to rebuild the stencil to more closely match the board-registration trends. The maximum mismatch allowable, including the stencil visual-alignment accuracy, is 0.005 in. before significant defects occur. Compensating a stencil to match board lots is considered to be counterproductive.

The Stencil Process

Equipment capability is critical to the defect rate (see Figures 10 and 11). Characteristics of the stencil equipment and process are:

Stencil printer	MPM UP 3030
Stencil alignment accuracy	±0.0003 in.
Solder paste type	Alpha 609
Solder paste particle size	325 to 500
Stencil thickness	0.006 in. laser-cut 301 stainless steel
Squeegee type	Metal
Paste actual thickness	Mean = 0.0069 in.
Average 9 boards, 3 devices, 10 leads per device	3 Sigma = 0.00073
Paste volume	Mean = 3110 mils^3
3 sigma paste volume	3 Sigma = 281 mils^3

Component-Placement Process

Characteristics of the placement process are:

Placement equipment	Fuji IPIII Placer
Placement accuracy	±0.0015 in.

The parts were placed on the pads using two local fiducials per device.

Conclusion: The placement was aligned with local fiducials and the devices were placed in the center of the pads. Placement was not considered a significant contributor to the defect rate.

Infrared-Reflow Characteristics

Our standard reflow profile for this type of board was used. Characteristics of the solder-paste-reflow process are:

Infrared reflow oven	Full convection BTU MN: TRS21
Atmosphere	Shop air (no nitrogen)
Chain speed	40 in. per minute
Maximum temperature	215°C
Time over 183°C	90 seconds

Conclusion: The infrared-reflow profile has the least effect on the 0.40-mm-pitch defect rate. A profile is shown in Figure 12.

Overall Conclusion: Special attention to design and the assembly process is critical to assembly of widely spaced 0.40-mm-pitch devices. Closely spaced 0.40-mm-pitch devices offer lower defect rates. With proper design, the most important is placement and lead rotation, widely spaced 0.40-mm-pitch devices can be assembled with defect rates approaching those of 0.50-mm-pitch devices. Not paying attention to a few basic requirements can make a product unmanufacturable and cost the manufacturer $20s of dollars per board in touch-up costs, a truly non-value-added and avoidable expense.

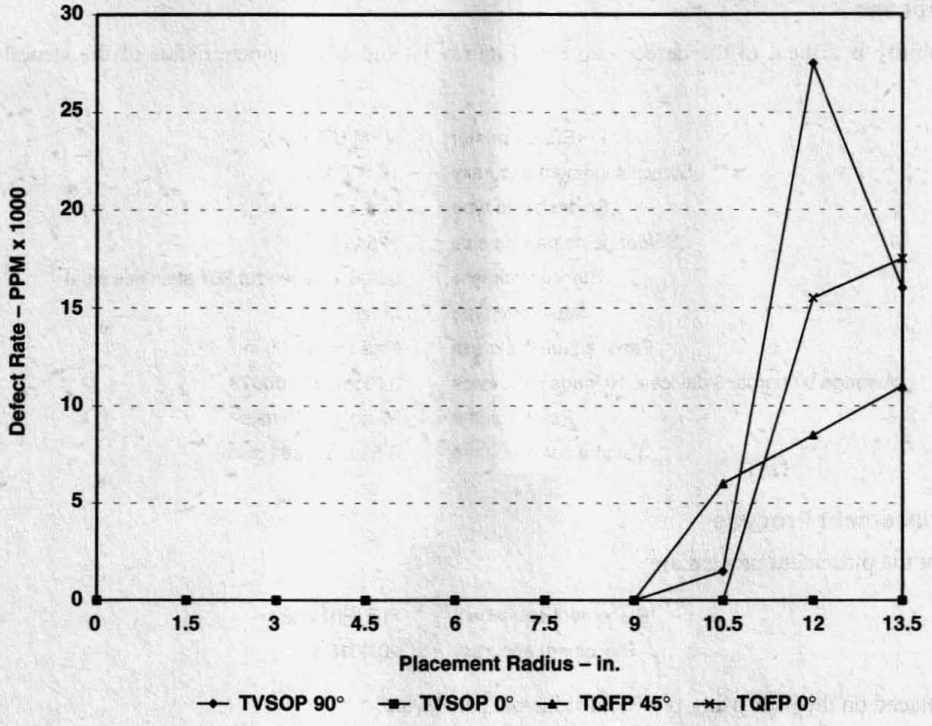


Figure 10. Defect Rate With 5-mil Stencil Thickness

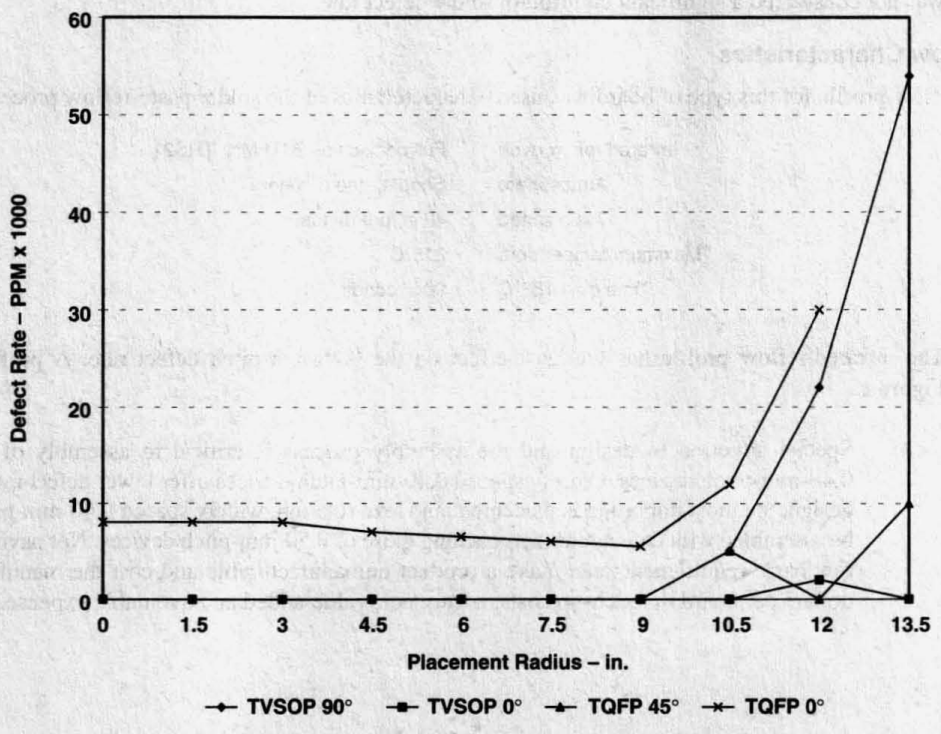
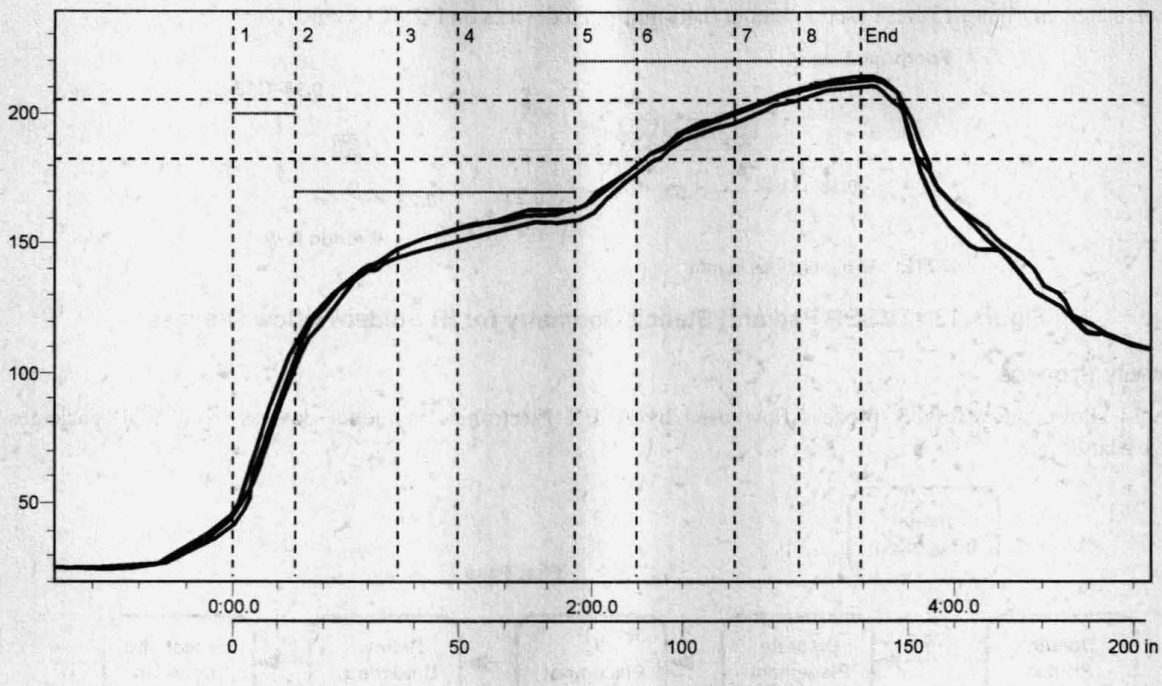


Figure 11. Defect Rate With 6-mil Stencil Thickness



	ZONE	1	2	3	4	5	6	7	8
Speed	Upper	200°	170°	170°	170°	220°	220°	220°	220°
40 (in./min.)	Lower	200°	170°	170°	170°	220°	220°	220°	220°

Figure 12. IR-Reflow Thermal Profile

TVSOP Results From AVEX Electronics

Fifty-six individual double-sided PCMCIA assemblies, eight to a manufacturing panel, for each of two types of plating (gold and Entek™) were manufactured by AVEX Electronics Inc. Experiments were performed on each of the assemblies to investigate the effect of pad geometry, stencil geometry, and assembly process flow on 0.40-mm (16-mil) lead-pitch devices using high-volume manufacturing equipment.

Pad- and Stencil-Geometry Requirements

The dimensions of the interconnect pad and the stencil aperture have a major effect on the quality of the solder joint. These dimensions must be adhered to during design. The raw card and stencil must maintain these dimensions; otherwise, yields and reliability will be reduced significantly.

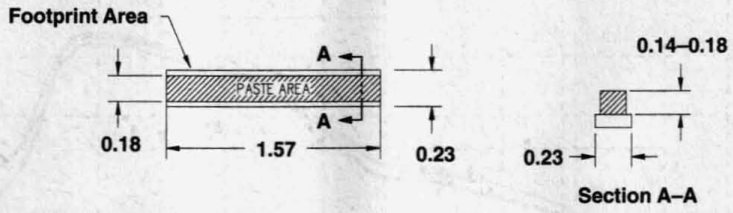
PAD GEOMETRY

Terminal pad length	1.57 mm (0.062 in.)
Terminal pad width	0.23 mm (0.009 in.)
Terminal pad pitch	0.40 mm (0.016 in.)
Pad finish	Entek™, gold plating

STENCIL GEOMETRY

Stencil opening length	1.57 mm (0.062 in)
Stencil opening width	0.18 mm (0.007 in)
Stencil thickness	0.13 mm (0.005 in)

The dimensions in Figure 13 were used to mount 0.40-mm-pitch devices on PCMCIA cards.



NOTE: All dimensions in mm

Figure 13. TVSOP Pad and Stencil Geometry for IR Solder-Reflow Process

Assembly Process

Figure 14 shows the assembly process flow used by AVEX Electronics to mount devices in TVSOP packages on PCMCIA cards.

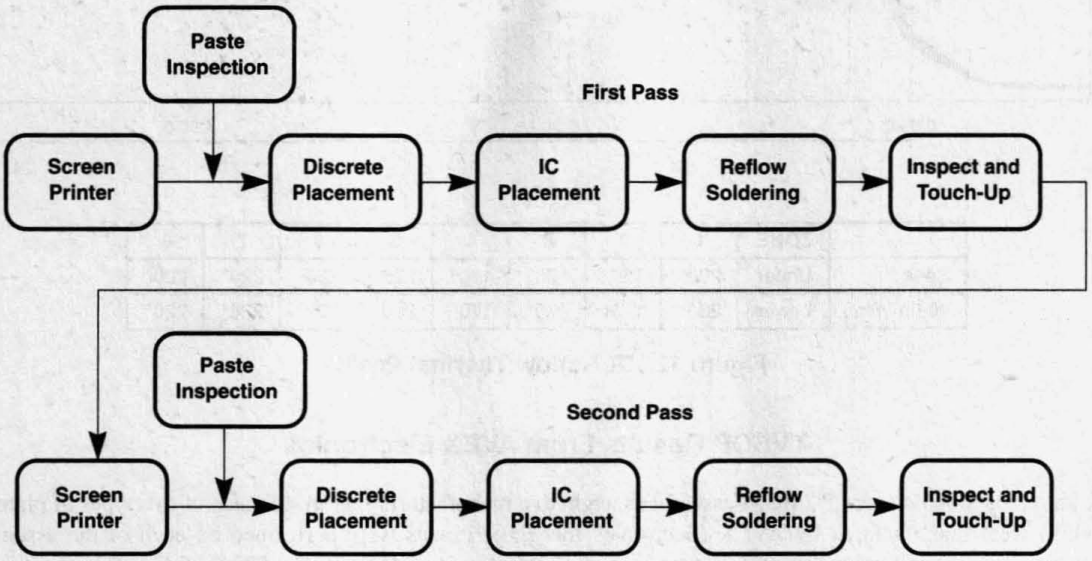


Figure 14. AVEX Process Flow for Mounting TVSOP Devices

The equipment used for the 0.40-mm-lead-pitch mounting evaluation is:

Screen printer	DEK 265GS
Stencil alignment accuracy	±0.0006 in.
Solder paste	Alpha WS609
Solder paste particle size	325–500 (25–45 μm)
Stencil thickness	0.005 in.
Squeegee type	Metal
Paste actual thickness	0.0055 in. to 0.007 inch
Paste inspection	Cyberoptics LSI
Visual placement	KME CM82 (for discrete parts) KME CM92 (for ICs)
Visual accuracy	±0.001 in.
Reflow oven	Heller 1700D

Process Reflow Profile

The recommended, and used, IR-reflow profile, which is standard for PCMCIA cards, is:

- Preheat: Solder-joint temperature must be gradually increased from ambient to approximately 170°C at a rate not to exceed 2.5°C per second.
- Soak: Solder-joint temperature should be held at approximately 170°C for no more than 50 seconds.
- Reflow: Solder-joint temperature must be increased from 170°C to 210°C at a rate not to exceed 2.5°C per second. Temperature dwell time above 183°C may range from 45 seconds to 65 seconds. Total heating dwell time may be 4 min. to 6 min., depending on thermal inertia and component sensitivity.

Conclusion

Based on the experiments during the qualification run, AVEX concludes:

- There was no appreciable difference between the gold- and Entek™-plated PCBs. Choice of PCB plating materials should be based on the solder-paste chemistry.
- Results comparing 7-mil and 8-mil stencil apertures showed that the smaller aperture resulted in a better yield.
- Special consideration must be given to the screen-print process: stencil thickness, aperture size, and PCB support during the second-pass screen-print process.
- Dedicated tooling may be required for machine placement on PCBs less than 0.031 in. thick.
- Component inspection is critical and may require laser-inspection capability on placement equipment.

Solder-Joint Reliability Study

The following photomicrographs are cross sections of leads on TVSOP packages attached to simulated PCMCIA circuit cards.

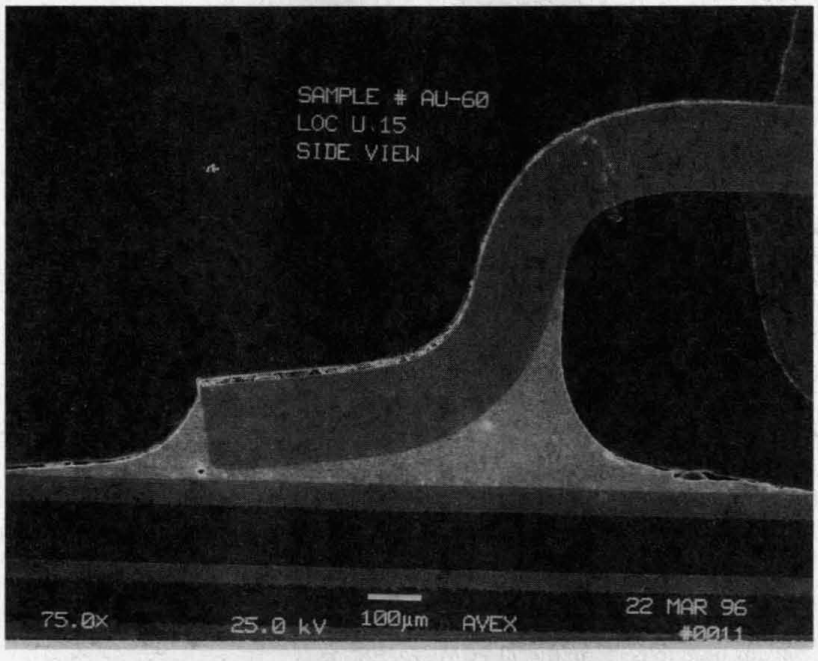


Figure 15. Cross Section of a TVSOP Lead-to-Pad Solder Joint (Side View)

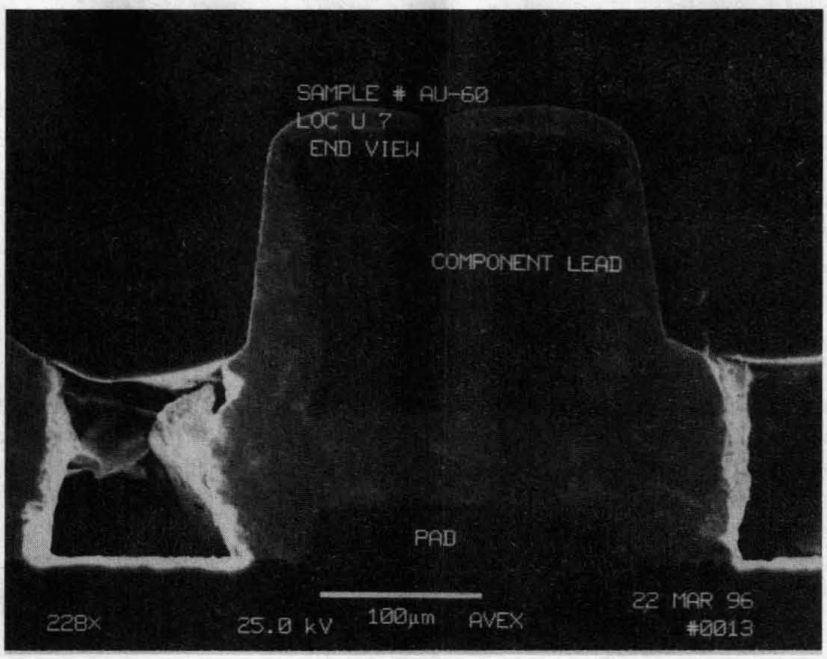


Figure 16. Cross Section of a TVSOP Lead-to-Pad Solder Joint (End View)

Temperature-Cycle Test

This experiment was designed to determine the reliability of TVSOP solder joints after thermal cycling.

No failures were obtained after 1200 thermal cycles between 0°C and 100°C. The following describes the AVEX thermal cycling test procedure and requirements for the TI PCMCIA Environmental Stress Screening (ESS):

- Support testing of 48 PCBs (12 panels) per run
- 300 cycles (0°C–100°C temperature profile, 15-min. dwell time, 15-min. ramp)
- 900 cycles (0°C–100°C temperature profile, 7.5-min. dwell time, 7.5-min. ramp)
- No power source is required for the unit under test (UUT)
- UUT continuity test requires monitoring of two circuits per UUT
- No current load required on UUT traces
- Continuous monitoring of UUT status, sample rate of at least one sample per second
- Failures to be removed after return to 25°C

Test Implementation

The PCMCIA panel assemblies were loaded onto an AVEX standard ESS tray. The tray was modified to hold five panels per tray on metal screws with nylon standoffs. The standard ESS frame wiring was used to provide the I/O interface from the ESS chamber to a monitoring PC system. The PC system monitored the continuity of the UUT traces through a standard digital I/O interface card.

Equipment List

The following equipment was used to perform the TI PCMCIA ESS test:

- ESS Chamber Model ESS5-7RWC
- AVEX ESS Frame
- Five AVEX tray assemblies
- Dell 486/33 PC system
- Metrabyte: PIO96 digital I/O card
- Application-specific chamber-to-PC controller-interface card assembly
- Application-specific test software written in Borland C

Chamber Profile

Table 4 lists the essential characteristics of the ESS5-7RWC test chamber.

Table 4. Characteristics of the ESS5-7RWC Test Chamber

ACTIVITY	TEMPERATURE RANGE	
	0°C–100°C	0°C–100°C
Negative ramp time	15 min.	7.5 min.
Lower dwell time	15 min.	7.5 min.
Positive ramp time	15 min.	7.5 min.
Upper dwell time	15 min.	7.5 min.
Total cycle length	60 min.	30 min.
Number of cycles	300 cycles	900 cycles
Total continuous cycles		1200 cycles

Test Data

The ESS profile was run from February 27, 1996 to April 8, 1996. No test failures were observed. The PC test-data log contained no entries for state changes of the PIO96 digital I/O inputs.

Definitions

UUT Unit under test. A single board assembly that is subjected to testing.

I/O Input/output. Signal lines for stimulus and monitoring of a system or board assembly.

PC system IBM-compatible personal computer system. Used as test controllers and monitoring units.

References

AVEX Electronics, In-Line ESS Lab Setup Wiring Diagram, Document No. 4000-14-0159.

AVEX Electronics, ESS Drawer Block Diagram, Document No. 4978-08-2034.

TI Reference Information

Thermal Characteristics

Heat is transferred from packages in three ways: conduction, convection, and radiation.

Conduction, the simplest heat-transfer mechanism, is the transfer of kinetic energy from a more excited electron to a nearby electron by vibrations and collisions. It is the primary mode of heat transfer within or between solids. Metals are good conductors because they have a large number of free electrons to encourage collisions. This ability to conduct heat is quantified by a proportionality constant (k) also known as thermal conductivity. The higher the thermal conductivity, the better the material conducts heat. Mold compounds play a role in conduction but do not contribute as much as copper leadframes.

The second method of heat transfer is convection. This transfer involves the movement of the heated substance. Convection is the primary mode of transfer between solids, liquids, or gases. The rate of convection is dependent on the surface area of the package and on the velocity and physical properties of air. Natural convection is heat transfer caused by induced differences in density that result from the expansion and contraction of air subjected to temperature changes. Forced convection is heat transfer caused by moving a cooling medium across a heat source. Forced airflow increases the rate of heat transfer.

The third mode of heat transfer is radiation. Radiated heat transfers occur due to thermal emission, primarily in the infrared spectrum. Though radiation always exists, it is the only mode of heat transfer between objects separated in a vacuum. Most of the heat transfer will take the form of conduction or convection.

Thermal Parameters

The thermal impedance (k-factor) of a package is defined as the increase in junction temperature above the ambient temperature due to the power dissipated by the device and is measured in degrees Celsius per watt. Two indices are commonly used to describe the thermal characteristics of an integrated-circuit package, θ_{JA} (junction to ambient) and θ_{JC} (junction to case).

Junction temperature Temperature of the die inside the package. Maintaining the junction temperature within a given range is necessary for proper device functionality and for long-term reliability. A lower junction temperature results in increased component reliability due to the reduced possibility of electro-migration or ball-bond intermetallic failure. Table 5 shows this relationship.

Table 5. Junction Temperature Versus Long-Term Reliability Comparison

JUNCTION TEMPERATURE	FAILURE RATE† (%)
100°C	0.02
110°C	1
120°C	11
130°C	46
140°C	80
150°C	96

† Failure rate at 100,000 hours

Case temperature Temperature on the package surface measured at the center of the top of the package by an attached K-type thermocouple.

Ambient temperature Temperature of the surrounding air. It is usually used as a reference point to calculate the junction or case temperature. It is measured at some distance away from the device.

Thermal Measurements

In making comparisons among parameters, it is important to understand how the parameters are measured and under what test conditions. Thermal measurement standards that have been developed by JEDEC will lead to a more consistent correlation of thermal performance among IC vendors. The JC15 JEDEC committee was formed to develop standards for the thermal measurement and modeling of IC packages. Perhaps the most important factor regarding variability in thermal measurements is the design of the thermal test board. Table 6 provides the JEDEC dimensions of dual-in-line packages with body length less than 28 mm and external lead pitch equal or less than 0.40 mm.

Table 6. JEDEC Thermal Test Board Specifications

DIMENSION	SPECIFICATION
Board thickness	1.57 mm (0.062 in.)
Board dimension (package length < 28 mm)	76.2 mm × 114.3 mm (3.0 in. × 4.5 in.)
Board material	FR-4 epoxy glass
Fan-out trace length (minimum)	25 mm (0.98 in.)
Fan-out trace position	Centered in 76.2 mm × 76.2 mm
Trace thickness	0.071 mm (0.0028 in.) ±20%
Trace width for 0.40-mm lead pitch	0.40 mm (0.016 in.)

Thermal modeling at TI uses an internally developed software package, ThermCAL. The software divides the package into a large number of small elements (meshing) then calculates temperature for each element based on temperatures of the surrounding elements.

TVSOP Power Dissipation and Thermal Impedance Characteristics

Device junction temperature is determined mainly by the IC power consumption, the surrounding temperature, and the thermal impedance between the junction and the atmosphere. The relationship is expressed by equation 1,

$$T_J = T_A + (\theta_{JA})P \quad (1)$$

Where:

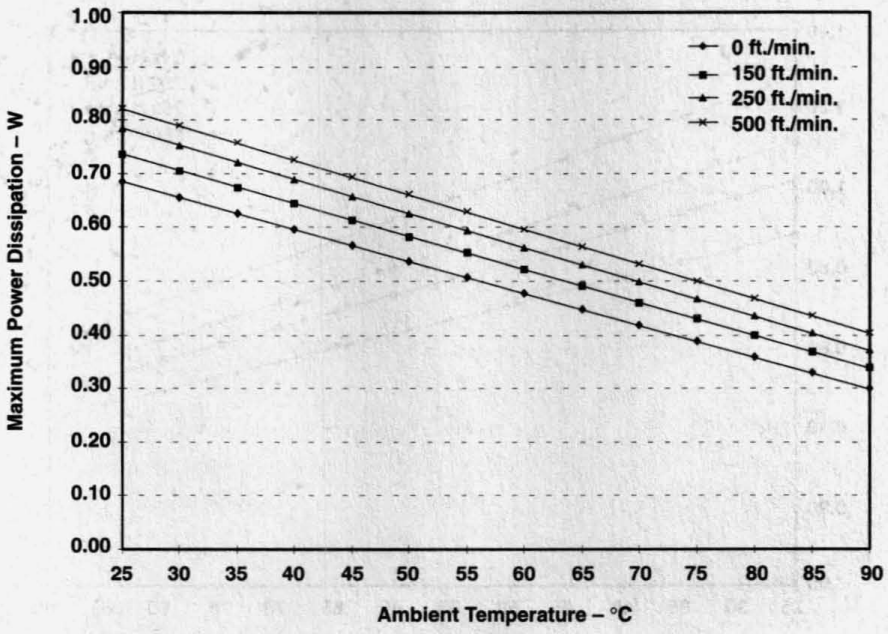
T_J = junction temperature
T_A = ambient temperature
P = power
θ_{JA} = thermal impedance

Thermal impedance is the package's resistance to heat dissipation and is inversely related to thermal conductivity (k). When a device reaches a state of equilibrium, the electrical power delivered is equal to the thermal heat dissipated. This thermal energy is in the form of heat and is given off to the surroundings. The maximum allowable power consumption at a given surrounding temperature is computed using the maximum junction temperature for the chip given in equation 2.

$$P = \frac{(T_J - T_A)}{\theta_{JA}} \quad (2)$$

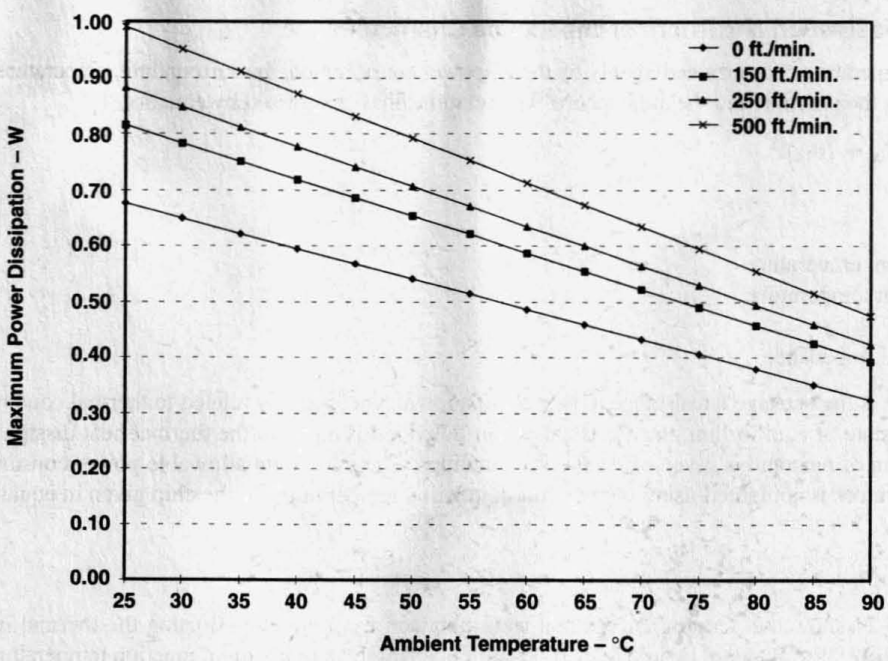
Figures 17 through 24 show the derating curves that were obtained from equation 2 using the thermal impedance values determined by using JEDEC-standard boards with 1000-mil trace length and maximum junction temperature 150°C. Factors affecting the thermal impedance are mainly material selection, package geometry, airflow, and length and width of the traces on the board.

Natural convection, in many cases, does not adequately dissipate heat. The solution is to induce airflow across a device. The data for a TVSOP 48-pin package shows that changing from natural convection to forced convection can decrease thermal impedance by as much as 25%.



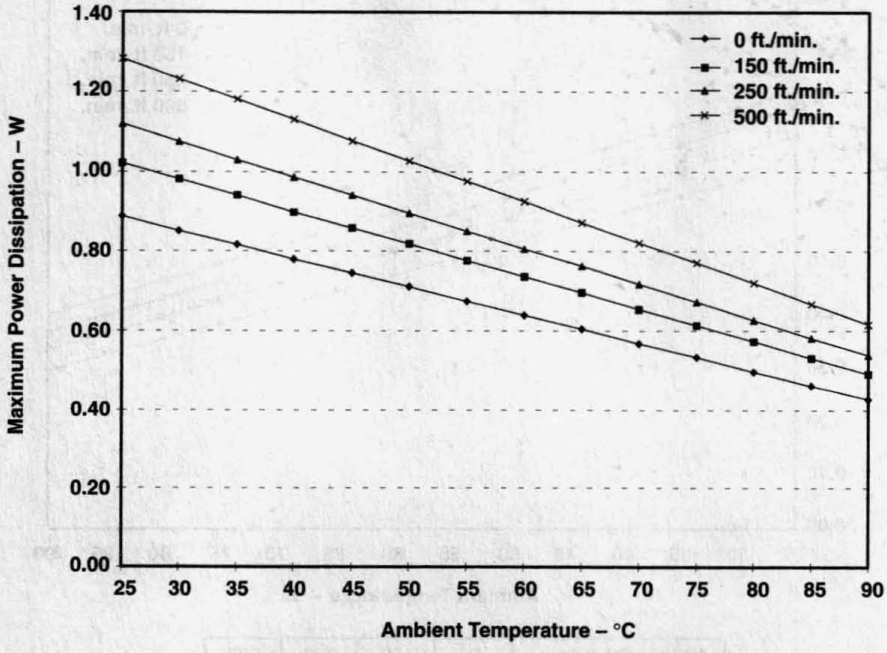
Air Velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	182	166	160	150

Figure 17. 14-Pin TVSOP Derating Curves



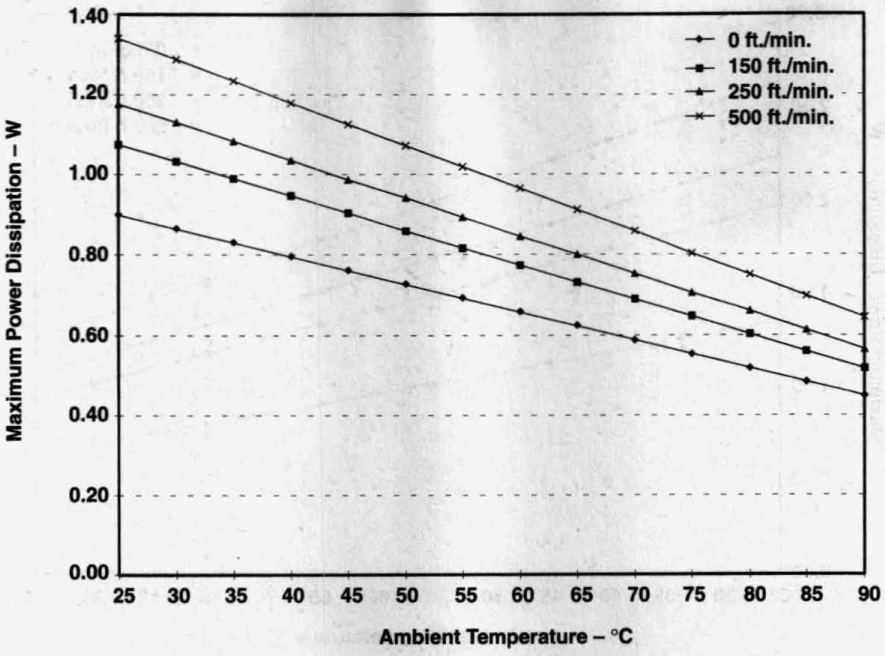
Air Velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	182	153	142	126

Figure 18. 16-Pin TVSOP Derating Curves



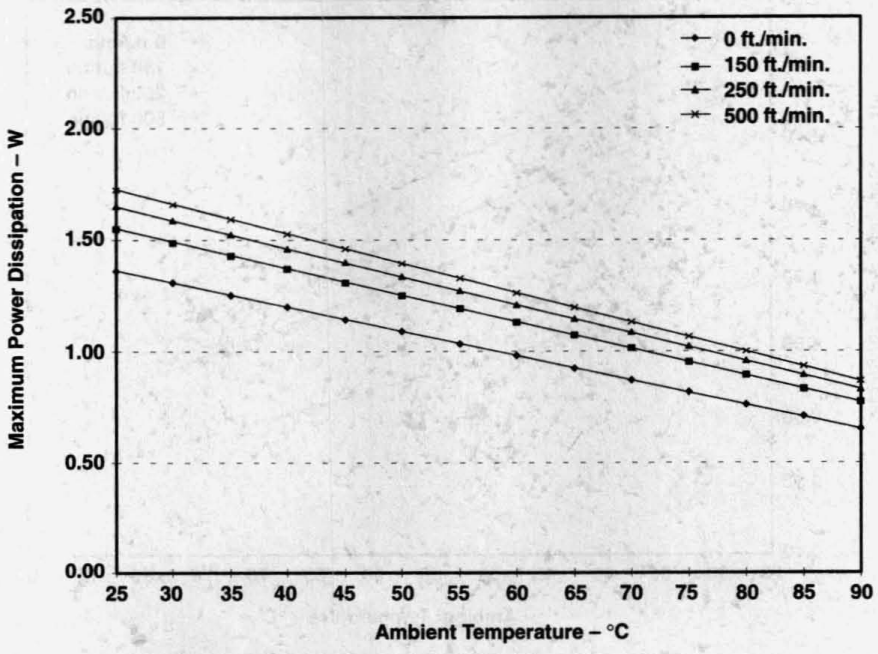
Air Velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	146	122	112	97

Figure 19. 20-Pin TVSOP Derating Curves



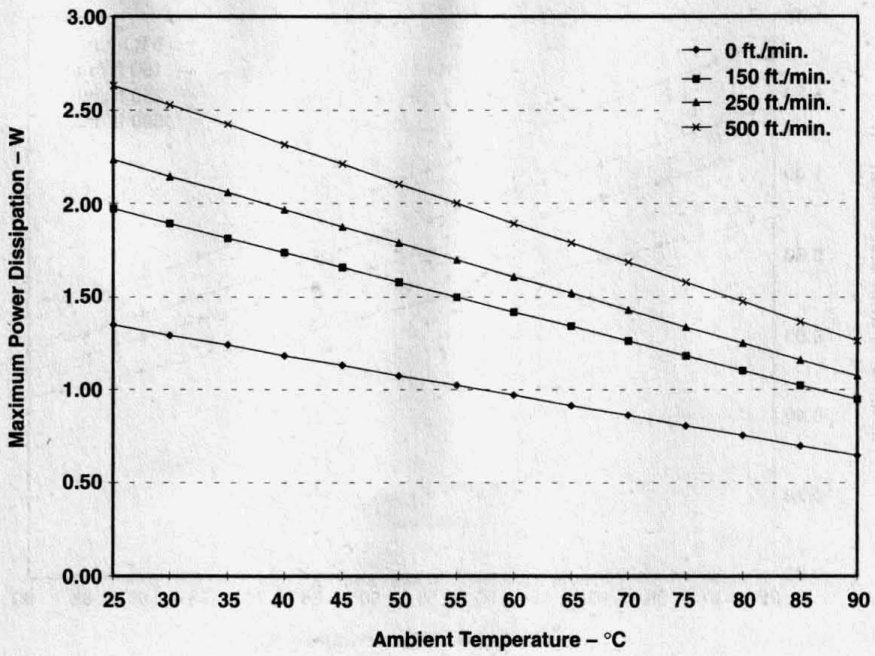
Air Velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	139	116	106	93

Figure 20. 24-Pin TVSOP Derating Curves



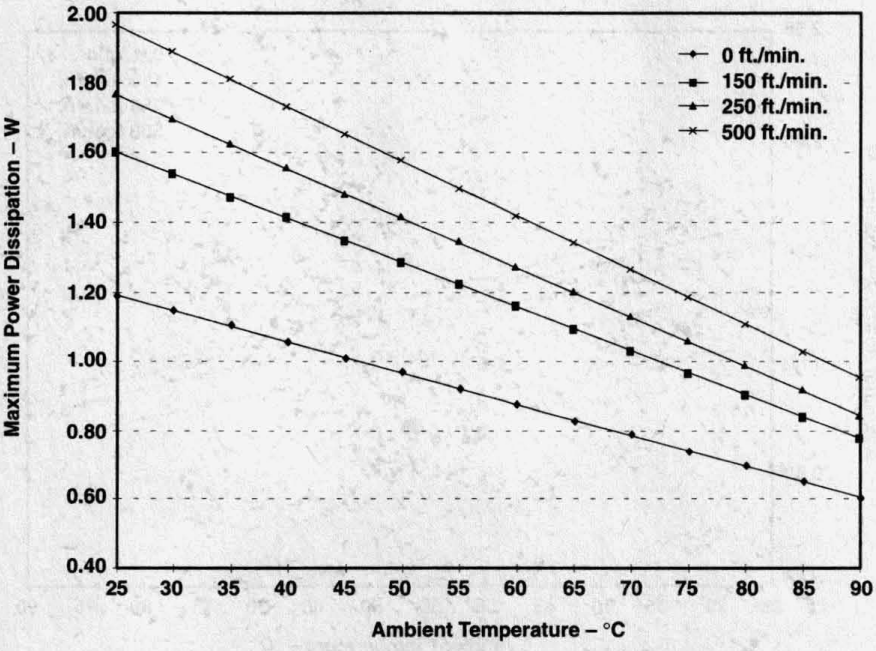
Air Velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	93	81	77	71

Figure 21. 48-Pin TVSOP Derating Curves



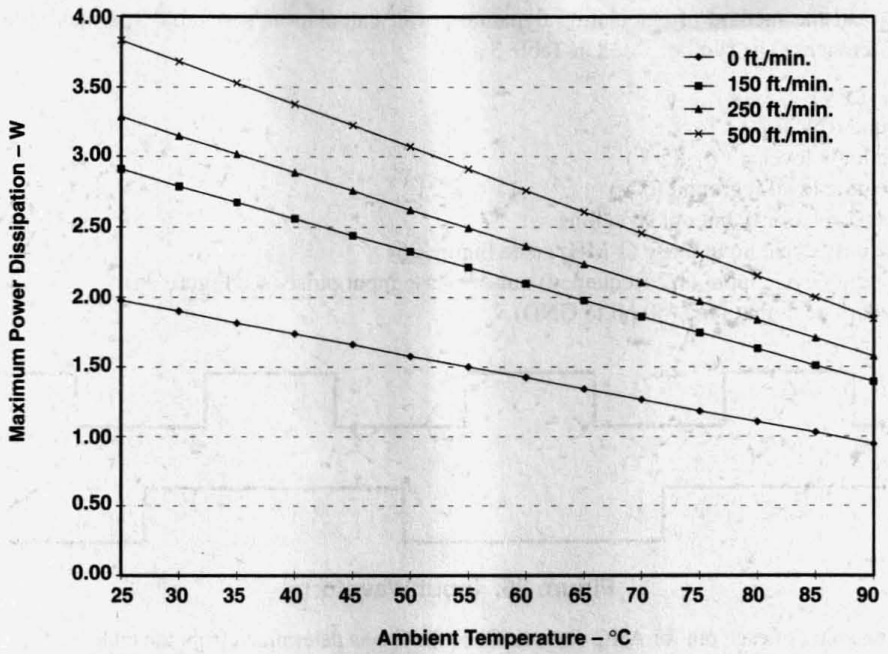
Air Velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	86	65	57	48

Figure 22. 56-Pin TVSOP Derating Curves



Air Velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	106	78	72	64
θ_{JC} (°C/W)	23			

Figure 23. 80-Pin TVSOP Derating Curves



Air Velocity (ft./min.)	0	150	250	500
θ_{JA} (°C/W)	63	43	38	33

Figure 24. 100-Pin TVSOP Derating Curves

Power Calculation[1]

When calculating the total power consumption of a circuit, both static and dynamic currents must be taken into account. Bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output (I_{CCL}, I_{CCH}, or I_{CCZ}), while a CMOS device has a single value for I_{CC}. These values can be found in the data sheets. TTL compatible CMOS and BiCMOS inputs, when driven at TTL levels, also consume additional current because they may not be driven all the way to V_{CC} or GND; therefore, the input transistors are not switched off completely. This value, known as ΔI_{CC}, also is provided in the data sheet.

Dynamic power consumption results from charging and discharging external load and internal parasitic capacitances. The parameter for CMOS device parasitic capacitance is C_{pd}, which is listed in the data sheet and is obtained using equations 3 and 4:

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_I} - C_{L(eff)} \quad (3)$$

$$C_{L(eff)} = C_L \times N_{SW} \times \frac{f_O}{f_I} \quad (4)$$

[1] The information presented in this section is a modified form of the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* Applications Report, literature number SCZA005.

To explain the C_{pd} and the method of calculating dynamic power calculation, see Table 7, which indicates the C_{pd} test conditions for AHC devices. The symbols used in Table 3 are:

V = V_{CC} (5 V)
G = ground (0 V)
1 = high logic level = V_{CC} (5 V)
0 = low logic level = ground (0 V)
X = don't care: 1 or 0, but not switching
C = 50% duty cycle input pulse (1 MHz) (see Figure 25)
D = 50% duty cycle input (1/2 frequency) out-of-phase input pulse (see Figure 25)
S = standard ac output load (50 pF to GND)

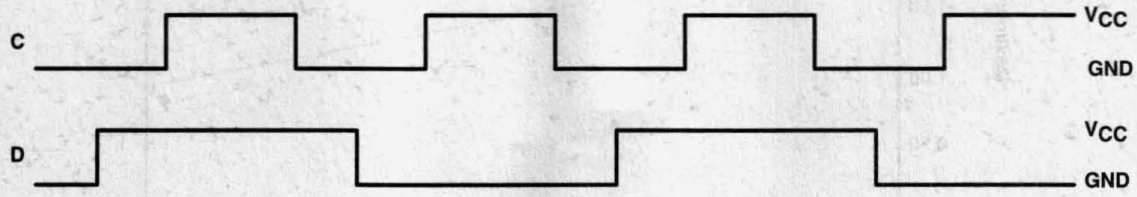


Figure 25. Input Waveform

Table 7 shows the switching of each pin for AHC devices. Once the C_{pd} is determined from the table, the P_D is easy to calculate using equations explained in the following sections.

Table 7. C_{pd} Test Conditions With One- or Multiple-Bit Switching

TYPE	PIN NO.																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AHC00	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC02	S	C	0	S	X	X	G	X	X	S	X	X	S	V						
AHC04	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC08	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC10	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC11	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC14	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC32	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC74	1	D	C	1	S	S	G	S	S	X	X	X	1	V						
AHC86	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC138	C	0	0	0	0	1	S	G	S	S	S	S	S	S	S	V				
AHC139	0	C	0	S	S	S	S	G	S	S	S	S	X	X	X	V				
AHC240	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC244	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC245	1	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC373†	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC374‡	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC540	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC541	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC573†	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V
AHC574‡	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V

† All bits switching, but with no active clock signal
‡ All bits switching

CMOS

CMOS-Level Inputs

Static-power consumption can be calculated using equation 5.

$$P_S = V_{CC} \times I_{CC} \quad (5)$$

The dynamic-power consumption of a CMOS device is calculated by adding the transient-power consumption and capacitive-load power consumption.

Transient Power Consumption

The transient power is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This power is a result of the current required to charge the internal nodes (*switching current*) plus the current that flows from V_{CC} to GND when the p-channel and n-channel transistors turn on briefly at the same time during the logic transition (*through current*). The frequency at which the device is switching, plus the rise and fall time of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible in comparison with the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the device and the charge and discharge current of the load capacitance.The transient power consumption can be calculated using equation 6.

$$P_T = C_{pd} \times V_{CC}^2 \times f_I \times N_{SW} \quad (6)$$

In case of single-bit switching, N_{SW} in equation 6 becomes 1.

Capacitive-Load Power Consumption

Additional power is consumed in charging of external load capacitance and is dependent on switching frequency. Equation 7 can be used to calculate this power while all outputs have same load and are switching at the same output frequency.

$$P_L = C_L \times V_{CC}^2 \times f_O \times N_{SW} \ (C_L \text{ is the load per output}) \quad (7)$$

In case of different loads and different output frequencies at all outputs, equation 8 is used to calculate capacitive load power consumption.

$$P_L = \Sigma(C_{Ln} \times f_{On}) \times V_{CC}^2 \quad (8)$$

Therefore, dynamic power consumption (P_D) is the sum of these two power consumptions, and is expressed in equation 9 (single-bit-switching case) and 10 (multiple-bit switching with variable load and variable output frequencies):

$$P_D = \left(C_{pd} \times f_I \times V_{CC}^2\right) + \left(C_L \times f_O \times V_{CC}^2\right) \quad (9)$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma\left(C_{Ln} \times f_{On}\right)\right] V_{CC}^2 \quad (10)$$

Total power consumption with a CMOS-level input is the sum of static and dynamic power consumption.

TTL-Level Inputs

Similarly, with TTL-level inputs, both static and dynamic power consumption can be calculated using equations 11, 12, and 13.

$$P_S = V_{CC}[I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)] \quad (11)$$

$$P_D = \left(C_{pd} \times f_I \times V_{CC}^2\right) + \left(C_L \times f_O \times V_{CC}^2\right) \text{ (single bit switching)} \quad (12)$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma\left(C_{Ln} \times f_{On}\right)\right] V_{CC}^2 \quad (13)$$

(multiple bit switching with variable load and frequency)

BiCMOS

Static Power

$$P_S = V_{CC}\left\{DC_{en}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] + (1 - DC_{en})I_{CCZ} + (N_{TTL} \times \Delta I_{CC} \times DC_d)\right\} \quad (14)$$

Where:

ΔI_{CC} = 0 for bipolar devices

NOTE:
For a continuous waveform at 50% duty cycle, DC_{en} = 1.

Equation 14 becomes:

$$P_S = V_{CC}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] \quad (15)$$

NOTE:
If half of the time the waveform is high and half of the time the waveform is low and the waveform is switching continuously, $\Rightarrow (N_H = N_L = 1/2\ N_T)$, P_S becomes:

$$P_S = \left(\frac{V_{CC}}{2}\right)(I_{CCH} + I_{CCL}) \quad (16)$$

Dynamic Power

$$P_D = (DC_{em} \times N_{SW} \times V_{CC} \times f \times I_{CCD}) \text{ Condition is } 50\ pF \parallel 500\ \Omega \quad (17)$$

I_{CCD} is calculated with 50 pF ‖ 500 Ω, and given number of outputs switching.

NOTE:
For a continuous waveform at 50% duty cycle, DC_{en} = 1.

Dynamic power with external capacitance:

$$P_D = DC_{en} \times N_{SW} \times V_{CC} \times f \times (V_{OH} - V_{OL}) \times (C_L - 50\ pF) + DC_{en} \times N_{SW} \times V_{CC} \times f \times I_{CCD} \quad (18)$$

I_{CCD} is calculated with 50 pF ‖ 500 Ω, and given number of output switching.

Power is also consumed by the upper output driver due to the output resistor (500 Ω in most load circuits for outputs in the data sheet). This power is very small but needs to be included in dynamic power consumption calculation. Equation 19 is used to calculate this power consumption.

$$P_{_Res} = (V_{CC} - V_{OH}) \times \frac{V_{OH}}{R} \quad (19)$$

NOTE:
Assume that the output waveform is always at logic high and is not frequency dependent.

Therefore, total dynamic power consumption is:

$$P_{D_TOT} = P_D + P_{_Res} \quad (20)$$

Finally, total power consumption can be calculated as:

$$P_{_Total} = P_{D_TOT} + P_S \quad (21)$$

Where:

V_{CC} = supply voltage (V)
I_{CC} = power-supply current (A) (from the data sheet)
I_{CCL} = power-supply current when outputs are in low state (A) (from the data sheet)
I_{CCH} = power-supply current when outputs are in high state (A) (from the data sheet)
I_{CCZ} = power-supply current when outputs are in high-impedance state (A) (from the data sheet)
ΔI_{CC} = power-supply current when one input is at a TTL level (A) (from the data sheet)
DC_{en} = % duty cycle enabled (50% = 0.5)

DC_d = % duty cycle of the data (50% = 0.5)
N_H = number of outputs in high state
N_L = number of outputs in low state
N_{sw} = total number of outputs switching
N_T = total number of outputs
N_{TTL} = number of inputs driven at TTL levels

fi = input frequency (Hz)
f_O = output frequency (Hz)
f = operating frequency (Hz)
V_{OH} = output voltage in high state (V)
V_{OL} = output voltage in low state (V)
C_L = external load capacitance (F)
I_{CCD} = slope of the I_{CC} versus frequency curve (A/Hz × bit)

$C_{L(eff)}$ = effective load capacitance (F)
f_O/f_I = ratio of output and input frequency (Hz)
P_T = transient power consumption
P_D = dynamic power consumption
P_S = static power consumption
$P_{_Res}$ = power consumption due to output resistance
P_{D_TOT} = total dynamic power consumption
$P_{_Total}$ = total power consumption

C_{PD} = dynamic power dissipation capacitance (F)
P_L = capacitive-load power consumption
Σ = sum of n different frequencies and loads at n different outputs
f_{On} = all different output frequencies at each output numbered 1 through n (Hz)
C_{Ln} = all different load capacitances at each output numbered 1 through n

For GTL and BTL/FB devices, the power consumption/calculation is similar to a BiCMOS device with the addition of the output power consumption through the pullup resistor, since GTL is open drain and BTL/FB is open collector.

The total power calculated using these equations should be less than the package power dissipation mentioned in the data sheets. Otherwise, the device may not function properly.

Electrical Characteristics

Electrical characteristics of the IC packages used at TI are normally determined by computer- modeling programs developed in-house (PACED)[2] or by using commercially available software. Electrical parameters are measured in our laboratories to verify the modeling data. The measurement methods follow the EIA/JEDEC Guideline EIA/JEP123 and include the use of impedance meters, time-domain reflectometers (TDRs) and network analyzers.

The electrical modeling program calculates the following parameters:

- Resistance (R) - dc or with high-frequency effects
- Capacitance (C) - including loading and coupling capacitance
- Inductance (L) - including mutual and self-inductance

The RLC parameters are available for each pin of the package being modeled or reported in tabular form as a range of values for the longest to the shortest leads. A SPICE input file for the package is also created by the modeling program. The SPICE file is produced in two formats: a lumped-parameter file, where each lead and bond wire is represented by one RLC element, or a distributed-parameter file, where the lead and bond wire is represented by many RLC elements. The distributed-parameter version represents varying sections of the lead more accurately and is used for higher-frequency simulations.

The characteristic impedance (Z_O) is calculated for each section of the lead and bond wire. This may be important if impedance matching is a consideration in the design for high-speed applications.

Electrical Parameters

Resistance

The resistance of an IC package conductor can be significant as a source of IR voltage drop in certain package families. In molded packages with copper lead frames (ρ = 1.7 μohm-cm)[3], most of the resistance is due to the bond wire because of the very small cross section (100 milliohms/0.1 in.). If Alloy 42 lead frames (ρ = 48.8 μohm-cm) are used, the resistance of the lead can be several-hundred milliohms and, therefore, much higher than the wire bonds. Co-fired ceramic packages tend to have higher conductor resistance because the material used is a tungsten/glass mixture (ρ = 25 μohm-cm). Other families that may have significant trace resistance include the thin-film processed interconnects, as in some multiple-chip modules, due to the low thickness of the conductors.

Capacitance

Capacitance is a function of the lead-surface proximity and the dielectric constant of the insulating material. These surfaces include the conductor leads, the power and ground planes (if any), and the presence of floating metal, such as heat spreaders. The electrical models for molded-lead-frame packages assume a ground plane exists in the PC board on which it is mounted. The capacitance to ground is usually very small for these style packages and most of the loading capacitance is due to interlead coupling. This coupling capacitance can be a source of crosstalk noise from lead to lead.

The relative dielectric constant can vary widely among package families. Mold compounds have relative dielectric constants of 4 to 5, alumina ceramic packages range from 9 to 10, and some lead-zinc-borate solder glass materials can be as high as 33.

Changing the proximity of one conductor to another can affect the coupling capacitance to a third conductor. This is exploited in some designs by moving the ground plane closer to the conductor leads to reduce the interlead coupling.

Inductance

Inductance is a function of the current distribution in the package and the relative permeability of the conductor material. Because of the dependence on current distribution, the effective inductance of a lead will depend on the ground return path in the system. Moving a ground plane closer to the conductor lead will decrease the magnetic field around the lead and reduce the mutual and self-inductance to the other leads. The lead width also significantly influences self-inductance. Minimum inductance is achieved when the lead width to height-of-lead-from-ground-plane ratio is maximized. Bond wires are a significant source of inductance because of their very narrow effective width.

---

2 PACED: Process Automation Center Electrical Design software

3 ρ (rho): Electrical resistivity

The proximity of floating, nonferrous metal (as in heat spreaders) will also decrease the effective inductance due to eddy currents flowing in these structures. The eddy currents flow in the opposite direction from the lead currents, reducing the total magnetic field.

As frequency increases, the self-inductance of the package lead will decrease. This is caused by the reduction of the magnetic field internal to the lead by the skin effect (current density greater near the surface of the conductor and less in the center). For copper lead frames, this effect is very small and can usually be ignored. For magnetic lead frame materials with higher relative permeability, such as Alloy 42, the frequency dependence is large. However, the fast rise times of modern devices dictate a high-frequency bandwidth for the package and the Alloy 42 self-inductance will approach that of copper.

Solutions for reducing the effective inductance, especially for ground and power leads, includes increasing the number of lead paths for that function and multiple-wire bonding to the same package pin. Doubling the conductors, however, does not reduce the inductance by half. The mutual inductance between the leads prevents this from happening and, if the leads are tightly coupled, the inductance may only decrease by 20 percent or so. To maximize the reduction of the effective inductance, the leads serving the same function, such as ground or power, should be as far apart as possible.

TVSOP Electrical Data

Figures 26 through 29 show the minimum and maximum range of capacitance (C) and inductance (L) for 14-pin to 56-pin narrow-body TVSOP packages and 80-pin and 100-pin wide-body TVSOP packages. Table 8 summarizes TVSOP electrical data.

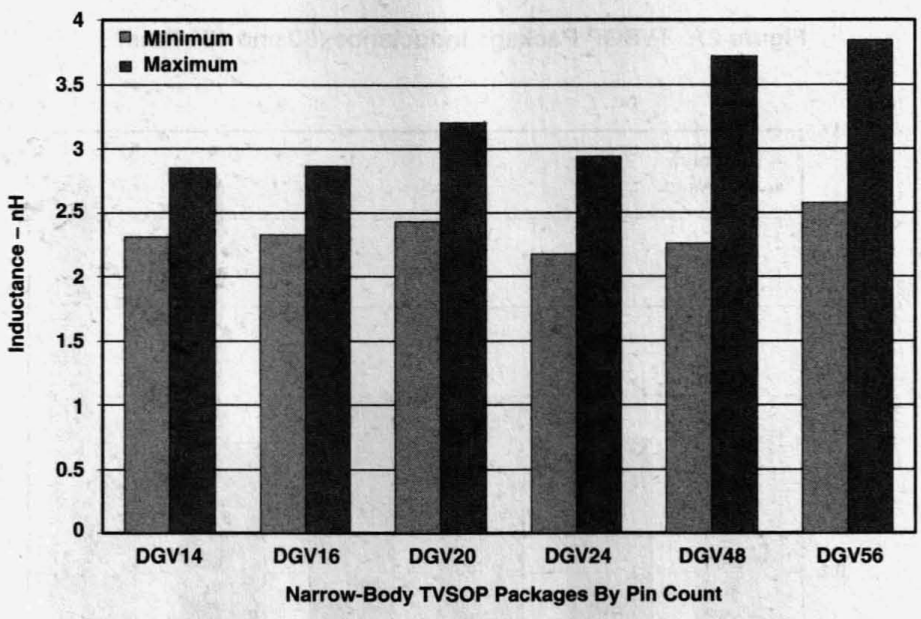


Figure 26. TVSOP Package Inductance (14, 16, 20, 24, 48, and 56 Pins)

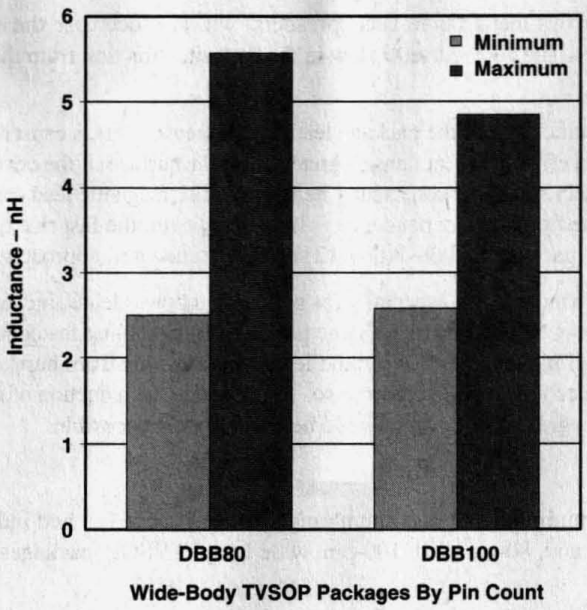


Figure 27. TVSOP Package Inductance (80 and 100 Pins)

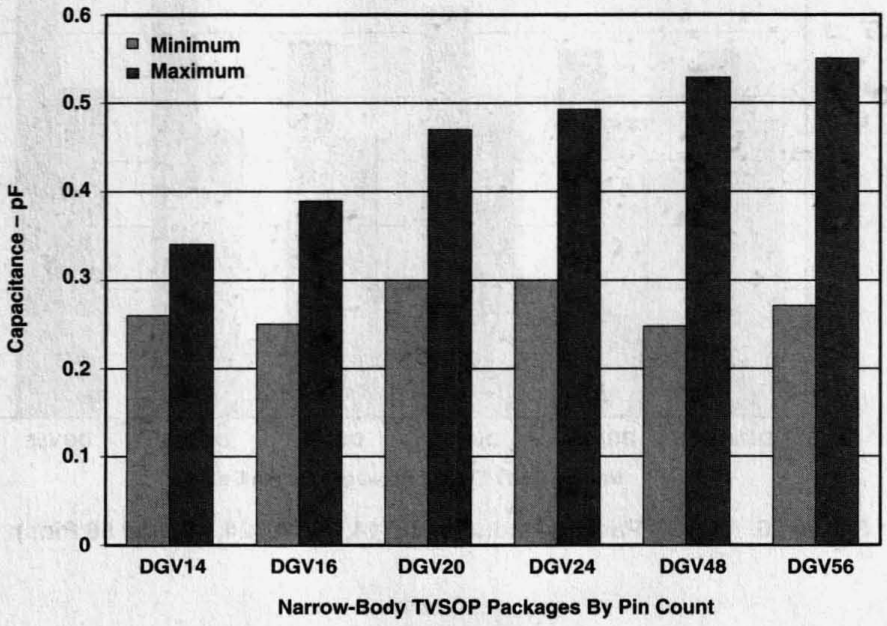


Figure 28. TVSOP Package Capacitance (14, 16, 20, 24, 48, and 56 Pins)

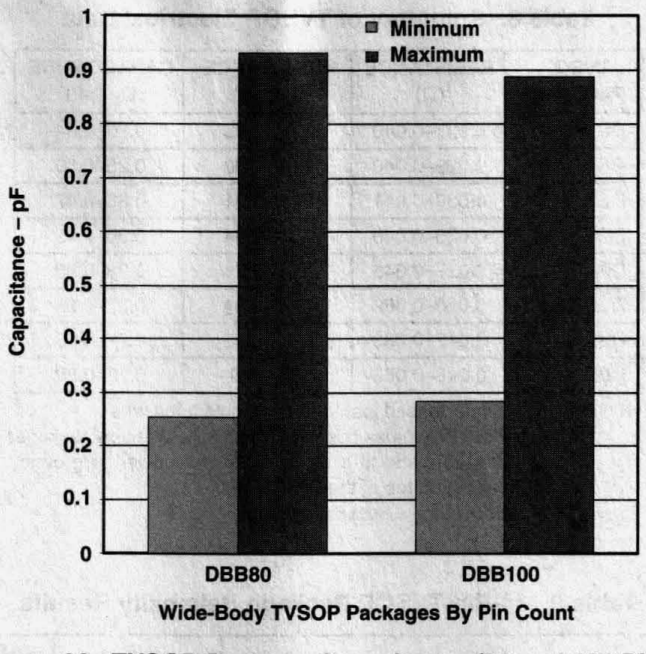


Figure 29. TVSOP Package Capacitance (80 and 100 Pins)

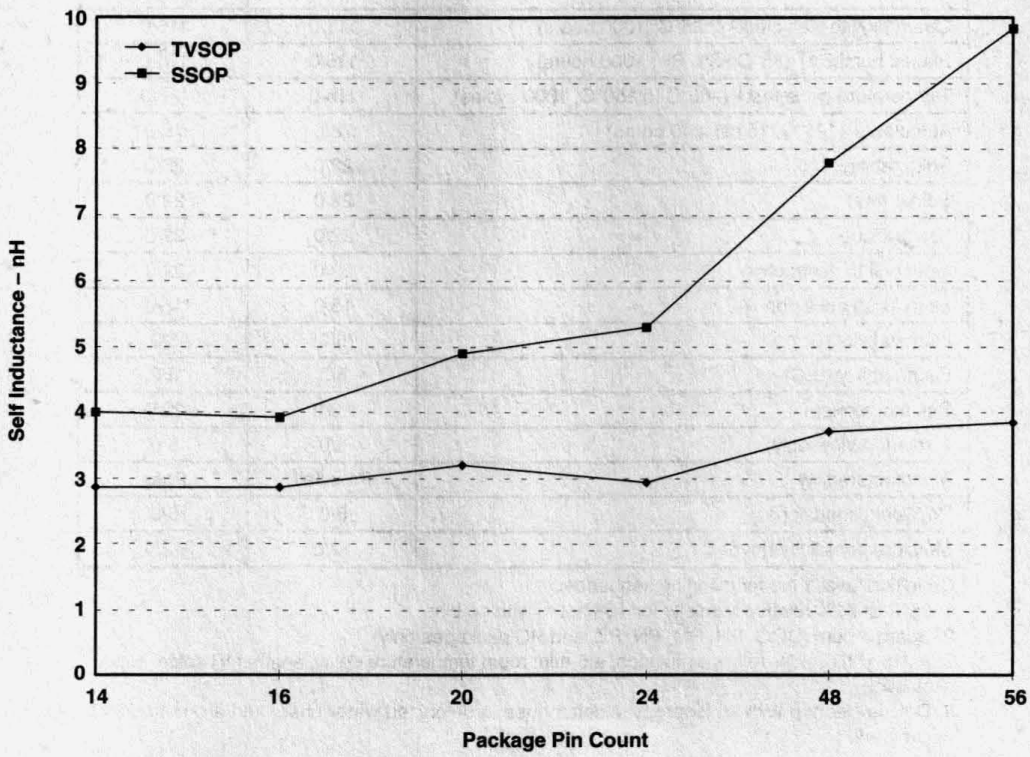


Figure 30. TVSOP and SSOP Self-Inductance Comparison

Table 8. Summary of TVSOP Electrical Data

TVSOP PACKAGE	RESISTANCE (Ω)	INDUCTANCE L_S (nH)	CAPACITANCE C_L (pF)
DGV 14	0.037–0.040	2.31–2.85	0.26–0.34
DGV 16	0.029–0.040	2.32–2.86	0.25–0.39
DGV 20	0.039–0.041	2.43–3.21	0.30–0.47
DGV 24	0.035–0.040	2.17–2.94	0.30–0.49
DGV 48	0.027–0.045	2.26–3.71	0.28–0.53
DGV 56	0.050–0.062	2.57–3.84	0.27–0.55
DBB 80	0.042–0.083	2.50–5.57	0.25–0.93
DBB 100	0.046–0.066	2.58–4.9	0.28–0.89

NOTES: 1. Copper-based leadframe and gold bond wire
2. Electrical values based on maximum die fit on packages
3. Ground plane is a single layer (no power or ground planes) on top of the PCB.

L_S = self-inductance, C_L = load capacitance

Table 9. 14-Pin TVSOP Package Reliability Results

	REQUIRED SS PER NUMBER OF FAILS	AABT126DGV ACTUAL SS PER NUMBER OF FAILS
Operating life static test† (125°C, 1000 hours)	116/0	116/0
Biased humidity† (85°C/85% RH, 1000 hours)	116/0	116/0
Temperature cycle test† (–65°C to 150°C, 1000 cycles)	116/0	116/0
Autoclave† (121°C, 15 psi, 240 hours)	76/0	76/0
Solderability	22/0	22/0
Solder heat	22/0	22/0
Lead fatigue	22/0	22/0
Lead pull to destruction	22/0	22/0
Lead finish adhesion	15/0	15/0
Flammability (UL)	5/0	5/0
Flammability (IEC)	5/0	5/0
Salt atmosphere	22/0	22/0
X-ray (top view only)	5/0	5/0
Manufacturability	Pass/fail	Pass
Physical dimensions	5/0	5/0
Moisture sensitivity (level 1)	12/0	12/0

† Condition level 1 preconditioning sequence:
1. 85°C at 85% relative humidity for 168 hours with no bias
2. Board mount (DGG, PH, PM, PN, PZ, and RC packages only)
3. A 215°C IR solder-reflow simulation, a 5-min. room temperature delay, another IR solder-reflow simulation
4. Device cleanup with an isopropyl alcohol rinse, a deionized water rinse, and a one-hr. 25°C drying period

Table 10. 20-Pin TVSOP Package Reliability Results

	REQUIRED SS PER NUMBER OF FAILS	AABT126DGV ACTUAL SS PER NUMBER OF FAILS
Operating life static test† (125°C, 1000 hours)	116/0	116/0
Biased humidity† (85°C/85% RH, 1000 hours)	116/0	116/0
Temperature cycle test† (–65°C to 150°C, 1000 cycles)	116/0	116/0
Autoclave† (121°C, 15 psi, 240 hours)	76/0	76/0
Solderability	22/0	22/0
Solder heat	22/0	22/0
Lead fatigue	22/0	22/0
Lead pull to destruction	22/0	22/0
Lead finish adhesion	15/0	15/0
Flammability (UL)	5/0	5/0
Flammability (IEC)	5/0	5/0
Salt atmosphere	22/0	22/0
X-ray (top view only)	5/0	5/0
Manufacturability	Pass/fail	Pass
Physical dimensions	5/0	5/0
Moisture sensitivity (level 2)	20/0	20/0

† Condition level 2 preconditioning sequence:

1. 85°C at 60% relative humidity for 168 hours with no bias
2. Board mount (DGG, PH, PM, PN, PZ, and RC packages only)
3. A 215°C IR solder-reflow simulation, a 5-min. room temperature delay, another IR solder-reflow simulation
4. Device cleanup with an isopropyl alcohol rinse, a deionized water rinse, and a one-hr. 25°C drying period

Table 11. 48-Pin TVSOP Package Reliability Results

	REQUIRED SS PER NUMBER OF FAILS	ABT16640DGV ACTUAL SS PER NUMBER OF FAILS
Operating life static test† (125°C, 1000 hours)	116/0	116/0
Biased humidity† (85°C/85% RH, 1000 hours)	116/0	116/0
Storage life test† (150°C, 1000 hours)	90/0	90/0
Temperature cycle test† (–65°C to 150°C, 1000 cycles)	116/0	116/0
Autoclave† (121°C, 15 psi, 240 hours)	76/0	76/0
Solderability	44/0	44/0
Solder heat	44/0	44/0
Lead fatigue	6/0	6/0
Lead pull to destruction	6/0	6/0
Lead finish adhesion	6/0	6/0
Flammability (UL)	10/0	10/0
Flammability (IEC)	10/0	10/0
Salt atmosphere	44/0	44/0
Resist solvent	24/0	24/0
X-ray (top view only)	10/0	10/0
Manufacturability	Pass/fail	Pass
Physical dimensions	10/0	10/0
Moisture sensitivity (level 2)	20/0	20/0

† Condition level 2 preconditioning sequence:
1. 85°C at 60% relative humidity for 168 hours with no bias
2. Board mount (DGG, PH, PM, PN, PZ, and RC packages only)
3. A 215°C IR solder-reflow simulation, a 5-min. room temperature delay, another IR solder-reflow simulation
4. Device cleanup with an isopropyl alcohol rinse, a deionized water rinse, and a one-hr. 25°C drying period

Table 12. 80-Pin TVSOP Package Reliability Results

	REQUIRED SS PER NUMBER OF FAILS	ALVC16901DBB ACTUAL SS PER NUMBER OF FAILS
Operating life static test† (125°C, 1000 hours)	120/0	120/0
Biased humidity‡ (85°C/85% RH, 1000 hours)	116/0	116/0
Storage life test† (150°C, 1000 hours)	45/0	45/0
Temperature cycle test† (–65°C to 150°C, 1000 cycles)	120/0	120/0
Autoclave† (121°C, 15 psi, 240 hours)	78/0	78/0
Lead fatigue	66/0	66/0
Lead pull to destruction	3/0	3/0
Lead finish adhesion	5/0	5/0
Salt atmosphere	24/0	24/0
X-ray (top view only)	6/0	6/0
Manufacturability	Pass/fail	Pass
Physical dimensions	6/0	6/0
Moisture sensitivity (level 2)	12/0	12/0

† Condition level 1 preconditioning sequence:
1. 85°C at 85% relative humidity for 168 hours with no bias
2. Board mount (DGG, PH, PM, PN, PZ, and RC packages only)
3. A 215°C IR solder-reflow simulation, a 5-min. room temperature delay, another IR solder-reflow simulation
4. Device cleanup with an isopropyl alcohol rinse, a deionized water rinse, and a one-hr. 25°C drying period

‡ Condition level 2 preconditioning sequence:
1. 85°C at 60% relative humidity for 168 hours with no bias
2. Board mount (DGG, PH, PM, PN, PZ, and RC packages only)
3. A 215°C IR solder-reflow simulation, a 5-min. room temperature delay, another IR solder-reflow simulation
4. Device cleanup with an isopropyl alcohol rinse, a deionized water rinse, and a one-hr. 25°C drying period

Delivery of the TVSOP to TI Customers

Moisture Sensitivity of the TVSOP

Moisture sensitivity describes the characteristic of some plastic surface-mount packages to absorb sufficient moisture from their environment to cause the package to crack when exposed to the extreme temperature of reflow soldering. During solder reflow (IR, VPR, or wave solder), flash vaporization of the absorbed moisture causes high stress, resulting in internal cracking or delamination between the chip and the leadframe chip pad. Packages are tested for moisture sensitivity in accordance with JESD A112. Those packages that fail to meet Level 1 are designated as moisture sensitive and are dry packed. Table 13 describes the recommended floor life of the package after it is removed from the sealed dry-pack bag prior to soldering. The floor life may be extended by sealing the dry-pack bag as soon as possible after removing the components to be used.

Table 13. TVSOP Floor Life

LEVEL	FLOOR LIFE	
	CONDITIONS	DURATION
1	≤ 30°C at 90% RH	Unlimited
2	≤ 30°C at 60% RH	1 year
3	≤ 30°C at 60% RH	168 hours
4	≤ 30°C at 60% RH	72 hours
5	≤ 30°C at 60% RH	24 hours
6	≤ 30°C at 60% RH	6 hours

Dry pack is a method that protects moisture-sensitive plastic surface-mount devices from moisture during shipment and storage. The parts are initially baked, then placed inside a moisture- and vapor-barrier bag with a desiccant. The desiccant absorbs moisture and keeps the humidity inside the bag at a safe level. The moisture- and vapor-barrier bag used in dry pack has a maximum transmission rate of 0.02g/100 square inches in 24 hours. The desiccant used can absorb up to 3 grams of water per unit at 20% relative humidity (RH). The actual shelf life will vary based on the storage conditions, the quality of moisture barrier the bag provides, the number of desiccants used, and the size of the package. A humidity-indicator card is also added to the bag which shows the internal humidity of the bag in 10% increments. This card can be used to verify that the humidity level inside the bag has not exceeded the safe level. If the humidity inside the dry pack bag exceeds the recommended RH limit shown on the dry-pack label, the parts must be baked dry before soldering.

Baking conditions and duration are described on the dry-pack labels along with an outline of necessary precautions and seal date for products. TI uses this dry-pack method regardless of whether the parts are shipped in tubes or tape and reel.

Moisture-Sensitivity Qualification Data

Table 14 shows the moisture-sensitivity levels of several TVSOP packages. Reliability tests have been submitted on 20- and 24-pin packages to determine whether they can be reclassified as non-moisture sensitive (Level 1 moisture sensivity).

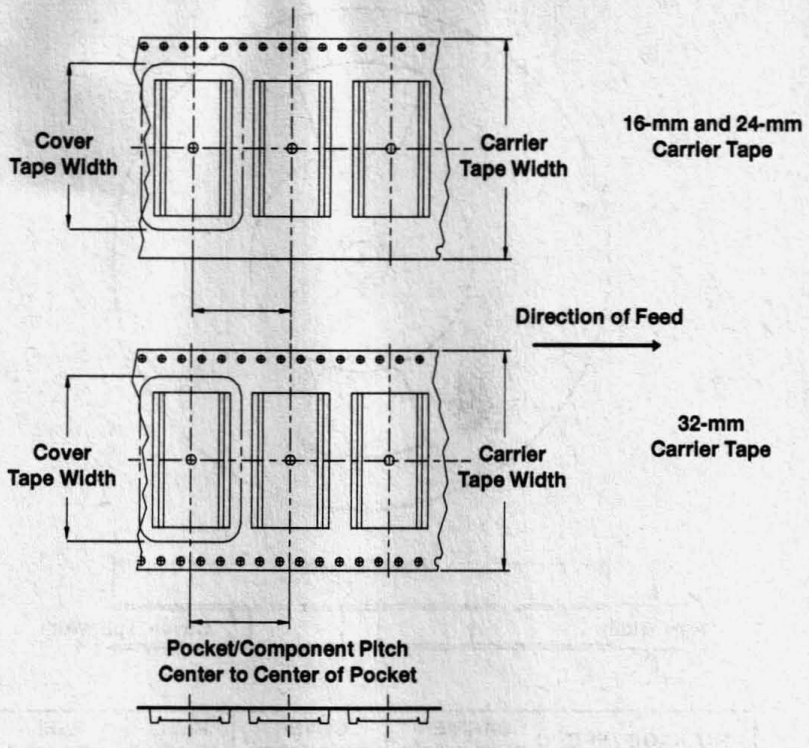
Table 14. TVSOP Moisture-Sensitivity Levels

PIN COUNT	MOISTURE LEVEL
14	Level 1
16	Level 1
20	Level 2
24	Level 2
48	Level 2
56	Level 2
80	Level 2
100	Level 2

Tape and Reel

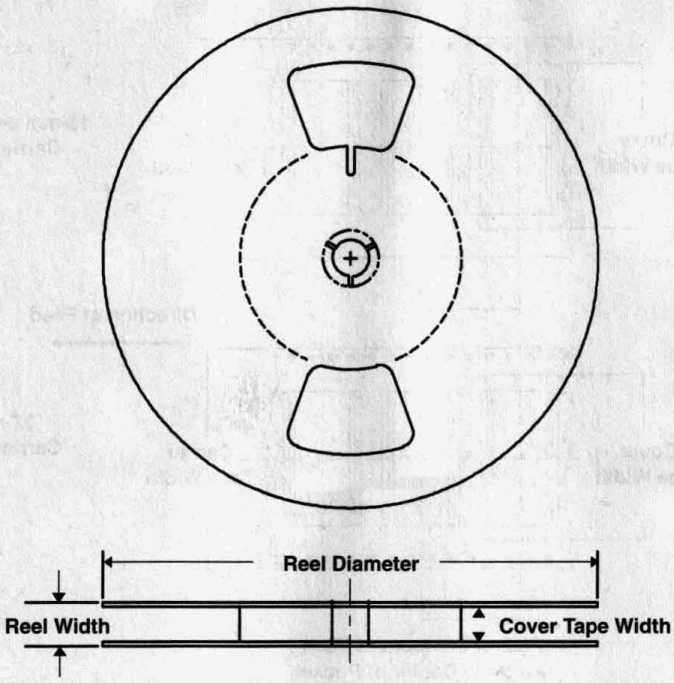
The purpose of tape-and-reel packaging is to position components so they can be placed on circuit boards using automated equipment. Components such as, but not limited to, diodes, capacitors, resistors, transistors, inductors, and ICs can be packed in this manner.

The packing materials used normally include a carrier tape, cover tape, and a reel. All material used meets industry guidelines for ESD protection. Dimensions are selected based on package size and design configurations. All dimensions are established to be within the recommendations of the Electronics Industry Association Standard EIA-481-1, EIA-481-2, and EIA-481-3. The dimensions that are of particular interest to the end user are tape width, pocket pitch, and quantity per reel. Figures 31 and 32 illustrate typical designs for carrier tape and reels for TVSOP packages.



PACKAGE	PINS	CARRIER TAPE WIDTH (mm)	COVER TAPE WIDTH (mm)	POCKET PITCH (mm)	QUANTITY PER REEL
DGV	14–48	16.00	13.3	8.00	2000
DGV	56	24.00	21.0	8.00	2000
DBB	80	24.00	21.0	12.00	2000
DBB	100	32.00	25.5	16.00	2000

Figure 31. Carrier and Cover-Tape Information for Reeled TVSOP Packages



PACKAGE TYPE (NUMBER OF PINS)	CARRIER TAPE WIDTH (mm)	COVER TAPE WIDTH (mm)	REEL WIDTH (mm)	REEL DIAMETER (mm)
DGV (14–48)	16.00	13.3	16.4	330
DGV (56), DBB (80)	24.00	21.0	24.4	330
DBB (100)	32.00	25.5	32.4	330

Figure 32. Reel Dimensions

Test Sockets

Table 15 lists available test sockets from Yamaichi and Enplas. The sockets are closed tooling.

Table 15. Available TVSOP Test Sockets

VENDOR	PIN COUNT	SOCKET WITH FLANGE	SOCKET WITHOUT FLANGE
Yamaichi	14	IC51-0142-2074-MF	IC51-0142-2074
Yamaichi	16	IC51-0162-2073-MF	IC51-0162-2073
Yamaichi	20	IC51-0202-2072-MF	IC51-0202-2072
Yamaichi	24	IC51-0242-2071-MF	IC51-0242-2071
Yamaichi	48	IC51-0482-2069-MF	IC51-0482-2069
Yamaichi	56	IC51-0562-2067-MF	IC51-0562-2067
Yamaichi	80	IC51-0802-2077-MF	IC51-0802-2077
Enplas	80		FP-80-0.4-01
Yamaichi	100	IC51-1002-2076-MF	IC51-1002-2076

Acknowledgment

The authors, Maria Y. Balian and Edgar Zuniga-Ortiz, ASL New Package Development, wish to acknowledge the following persons and corporations for their invaluable assistance in preparing this document:

Our co-workers in Advanced System Logic (ASL) and the Dallas Process Automation Center (DPAC) provided expert technical and editorial help and guidance. Without their support, this report would not have been possible.

Advanced System Logic, Texas Instruments, Sherman, Texas

David Holmgreen, ASL Launch Marketing
Douglas Romm, ASL Packaging (Thermal Modeling)
Cles Troxtell, ASL Test Finish

AVEX Electronics, Inc., a subsidiary of J.M. Huber Corporation, Huntsville, Alabama

Process Automation Center, Texas Instruments, Dallas, Texas

Darvin Edwards
Mike Lamson

Solectron, Texas (formerly TI Custom Manufacturing Services), Austin, Texas

David M. Mendez
Glen C. Shepherd
David M. Spitz
George C. Zbranek, Jr.

Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices

SCZA005
March 1997

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1997, Texas Instruments Incorporated

Contents

Title	*Page*
Thermal Considerations for Standard Linear and Logic (SLL) Packages and Devices	**8–99**
Package Thermal Performance	**8–100**
Power Calculation	**8–104**
CMOS	8–107
BiCMOS	8–108
Benefits of Minimizing Power Consumption	**8–110**
Reliability Implications	**8–111**
Thermal Definitions	8–111
Acknowledgment	**8–112**
References	**8–112**

TI is a trademark of Texas Instruments Incorporated.

Thermal Considerations for Standard Linear and Logic (SLL) Packages and Devices

Users of Texas Instruments (TI™) SLL products must consider device power dissipation, package power capability, and maximum ambient temperatures when designing with these products. The product users also need to be aware of the long-term reliability impact of maximum device-junction temperatures.

This application report is intended to help users understand and evaluate these factors. Three concepts — package thermal performance, device power dissipation, and reliability — are discussed in separate sections.

The first section, *Package Thermal Performance*, includes data about the recently developed JEDEC standard (EIA/JEDEC-Std-JESD51) for package thermal impedance measurement. It discusses most SLL package types and lists θ_{JA} (thermal impedance) values for those packages.

The second section, *Power Calculation*, discusses the power consumption by CMOS and BiCMOS/bipolar semiconductors. Standard formulas are given that allow the user to calculate the maximum power dissipated by a device in a typical application using data-book specifications, operating frequency, and voltage. The only characteristic not readily known is the output loading of the devices under consideration.

The third section, *Benefits of Minimizing Power Consumption*, discusses ways to reduce power consumption and the benefits thereof.

The final section, *Reliability Implications*, discusses the effects of chip temperature on reliability and electromigration. Information presented in this section allows the user to make an informed judgment as to the maximum chip temperature versus device wearout acceptable in the particular application.

The recommended analysis procedure is to assume a maximum chip temperature (see *Reliability Implications*) then, using θ_{JA} values for the chosen package (see *Package Thermal Performance*) and the known environmental requirements, calculate the maximum permissible power for that package. The formula presented in the *Power Calculation* section can then be used to ensure the operating conditions do not exceed the power capability of the chosen package type. Of course, the user can choose to calculate the maximum power from the application, then select a package that can meet the power dissipation requirement.

Package Thermal Performance

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_j - T_a}{P} \quad (1)$$

Where:

T_j = chip junction temperature
T_a = ambient temperature
P = device power dissipation

θ_{JA} values are also the most subject to interpretation. Factors that can greatly influence the measurement and calculation of θ_{JA} are:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

JEDEC established the JC 15.1 committee, comprising industry representatives, to develop industry-standard specifications for thermal testing. The specifications include development of electrical test procedures, careful descriptions of appropriate test environments, guidelines for the design of thermal test chips, guidelines for thermal modeling, and specifications for component mounting. The specifications for component mounting are divided into a series for different package types. The specifications include test-board descriptions for low effective thermal-conductivity test boards with a single metal layer and high effective thermal-conductivity test boards with embedded solid copper planes simulating system power and ground planes.

In August 1996, the Electronics Industries Association released EIA/JEDEC Std JESD51-3 titled *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. The standard describes guidelines with parameters for thermal-test-board design for low effective thermal conductivity (one signal layer in the trace fanout area) as differentiated from a multilayer printed-circuit board (PCB), which might include power and ground planes. The specified parameters include the area of the test board, the amount of copper traces on the test board, and the resulting trace fanout area, each important to the heat-sinking characteristics of the PCB. Prior to release of the standard, thermal-impedance data for similar packages varied widely within the industry due to the use of different test-board designs. As the industry adopts this standard methodology, thermal-impedance variations from test-board design should be minimized.

Key features of the standard test-board design are:

- Board thickness: 0.062 in.
- Board dimensions: 4.0 × 4.5 in. for packages > than 27 mm in length, 3.0 × 4.5 in. for packages ≤ 27 mm in length
- Trace thickness: 0.0028 in.
- Trace length: 25.0 mm (0.984 in.)

The SLL product group uses test boards designed to EIA/JEDEC Std JESD51-3 for thermal-impedance measurements. The parameters outlined in the standard also are used to set up thermal models. The thermal-model program used by SLL is ThermCAL, a finite-difference thermal-modeling tool.

Eleven SLL packages were tested using a JEDEC test-board design and compared to ThermCAL model results to validate the correlation between model results and data (see Table 1). This comparison shows that the models are accurate to within 10% of measured data. In many cases the model data varies from measured data by less than 5%.

Table 1. Package Comparison

PACKAGE TYPE (PINS, DESIGNATION)	DIE SIZE (mils)	θ_{JA} MEASURED (°C/W)	θ_{JA} MODELED (°C/W)	CHANGE (%)
56 DL	120 × 120	73.5	78.3	6.5
20 DW	62 × 62	96.6	90.9	–5.9
160 PCM	240 × 240	34.9	34.9	0
52 PAH†	120 × 120	87.2	92.2	5.7
52 PAH‡	120 × 120	72.7	75.2	3.4
100 PZ	360 × 360	45	42.8	–4.9
208 PDV	240 × 240	50.1	52.8	5.4
48 DGG	120 × 120	89.1	93.5	4.9
14 DGV	62 × 62	181.5	191.7	5.6
48 DGV	62 × 186	92.9	89.9	–3.2
100 PCA	240 × 240	33.3	34.9	4.8

† S-pad leadframe
‡ Conventional leadframe

After the accuracy of the model results was established, all other SLL packages could be modeled. θ_{JA} data based on EIA/JEDEC Std JESD51-3 is available for all SLL leaded surface-mount packages (see Table 2). The data is grouped by package type with values of θ_{JA} shown at different airflow levels. Leadframe pad size and die size are shown.

Junction-to-case thermal-impedance (θ_{JC}) data is shown with the junction-to-ambient data. Measured θ_{JC} data was generated for the packages tested using the JEDEC PCB. Previously published values of θ_{JC} are used for packages not yet tested using the PCB designed to EIA/JEDEC Std JESD51-3.

Table 2. SLL Package Thermal-Impedance Data

PIN COUNT	TI PACKAGE	JEDEC SPECIFICATION	PAD SIZE (mils)	CHIP SIZE (mils)	θ_{JA} (°C/W) AT AIRFLOW (LFM)				MEASURED/ MODELED	θ_{JC} (°C/W)
					0	150	250	500		
SOIC										
14	D	MS-012	70 × 70	32 × 37	126.6	104	96.4	87.4	Modeled	46
16	D	MS-012	90 × 90	44 × 65	112.6	91.2	83.9	74.8	Modeled	42
20	DW	MS-013	90 × 110	62 × 62	96.6	82.2	77.7	71.5	Measured	38.3
24	DW	MS-013	140 × 160	84 × 122	80.7	53.7	47.5	40.7	Modeled	25
28	DW	MS-013	120 × 140	90 × 128	78.2	54.3	48.4	41.9	Modeled	
SSOP										
14	DB	MO-150	71 × 71	43 × 52	158	128.6	118.9	106.5	Modeled	47
16	DB	MO-150	83 × 91	51 × 61	130.8	105.9	97.3	86.5	Modeled	47
20	DB	MO-150	87 × 106	61 × 65	114.6	92	84	74.7	Modeled	45
24	DB	MO-150	87 × 106	74 × 91	104.2	83.5	76.3	67.5	Modeled	42
28	DL	MO-118	150 × 180	97 × 142	97	77.2	70.9	63.1	Modeled	
48	DL	MO-118	120 × 180	73 × 128	93.5	69.9	63.8	57.1	Modeled	26
56	DL	MO-118	150 × 220	120 × 120	73.5	62.3	59	54.6	Measured	27.3
QSOP										
20	DBQ	MS-137	96 × 140	61 × 75	118.1	95.3	86.9	76.7	Modeled	46
24	DBQ	MS-137	96 × 140	61 × 75	113	92	84.1	74.6	Modeled	42
PLCC										
28	FN	MS-018	300 × 348	214 × 319	70.9	58.8	52.7	46	Modeled	26.7
44	FN	MS-018	270 × 270	235 × 235	46.2	38.6	35.4	31.6	Modeled	22
68	FN	MS-018	325 × 325	280 × 280	39.3	33	30.5	27.6	Modeled	14.5
84	FN	MS-018	275 × 275	188 × 185	39.7	33.9	31.8	29.4	Modeled	11.9
QFP										
52	RC	MS-022	210 × 210	120 × 120	78.9	48.4	43.6	38.1	Modeled	20
80	PH		265 × 265	232 × 240	76.1	67.9	61.4	53.6	Modeled	15.1
132	PQ	MO-069	315 × 315	272 × 272	46.3	34.5	31.6	28.3	Modeled	9.8
144	PCM	MS-022	433 × 433	338 × 338	38.8	27.3	25.1	22.4	Modeled	14.5
160	PCM	MS-022	511 × 511	433 × 433	34.9	29.9	28.3	24.7	Measured	11.4
208	PPM	MO-143	413 × 413	268 × 268	36.7	30.4	28.1	26.7	Modeled	
TQFP										
52	PAH	MO-136	S-Pad	120 × 120	87.2	76.1	71.5	67	Measured	28.3
52	PAH	MO-136	3.5 × 3.5 mm	120 × 120	72.7	62.6	59.2	53.8	Measured	24.0
64	PM	MO-136	6.75 × 6.75 mm	235 × 235	66.9	53.6	47.6	40.6	Modeled	10.4
64	PAG	MO-136	S-Pad	240 × 240	58.2	48.8	45.2	40.3	Measured	22.6
80	PN	MO-136	S-Pad	240 × 240	61.5	52.8	49.3	44.6	Measured	26.4
100	PZ	MO-136	S-Pad	360 × 360	45	38.3	35.3	27.9	Measured	7.6
100	PZ	MO-136	S-Pad	240 × 240	50.1	42.7	40.4	36.8	Measured	21.1
100	PCA	MO-136	6.5 × 6.5 mm	240 × 240	33.3	24.7	21.8	19.2	Measured	4.3
120	PCB	MO-136	6.5 × 6.5 mm	240 × 240	28.1	22.3	21	18	Modeled	3.3
144	PGE	MO-136	342 × 350	378 × 378	48.3	39.1	35.5	31	Modeled	9.9
208	PDV	MO-136	S-Pad	240 × 240	50.1	43.63	40.9	37.3	Measured	9.9

Table 2. SLL Package Thermal-Impedance Data (Continued)

PIN COUNT	TI PACKAGE	JEDEC SPECIFICATION	PAD SIZE (mils)	CHIP SIZE (mils)	θ_{JA} (°C/W) AT AIRFLOW (LFM)				MEASURED/ MODELED	θ_{JC} (°C/W)
					0	150	250	500		
SOP										
14	NS	EIAJ-TYPE-II	79 × 87	55 × 57	127.1	103.7	95.5	85.2	Modeled	95
16	NS	EIAJ-TYPE-II	87 × 142	76 × 86	111.3	89.3	81.4	71.5	Modeled	95
20	NS	EIAJ-TYPE-II	87 × 118	60 × 77	100.3	82.8	76.2	68	Modeled	90
TSSOP										
14	PW	MO-153	71 × 71	48 × 53	169.8	146.7	136	121.7	Modeled	35
16	PW	MO-153	104 × 104	56 × 76	148.9	127.9	117.6	103.9	Modeled	35
20	PW	MO-153	102 × 106	53 × 69	128	110.6	101.9	90.8	Modeled	34
24	PW	MO-153	94 × 140	74 × 91	119.9	98.8	90.6	80	Modeled	33
48	DGG	MO-153	4.6 × 3.2 mm	120 × 120	89.1	78.5	75.1	69.4	Measured	25.2
56	DGG	MO-153	3.94 × 5.08 mm	132 × 176	81.2	72.8	65.8	57.9	Modeled	13
64	DGG	MO-153	5.7 × 3.6 mm	120 × 120	72.9	63.3	61.8	57.1	Measured	21.3
TVSOP										
14	DGV	MO-194	75 × 75	62 × 62	181.5	165.8	159.5	150.4	Measured	66.7
16	DGV	MO-194	75 × 75	65 × 65	179.6	153.2	141.7	126.3	Modeled	
20	DGV	MO-194	104 × 104	94 × 94	146.1	122.3	111.6	97.4	Modeled	
24	DGV	MO-194	104 × 104	94 × 94	138.6	116.2	106.2	93.2	Modeled	
48	DGV	MO-194	100 × 240	62 × 186	92.9	80.9	77.1	71	Measured	27.2
56	DGV	MO-194	100 × 274	90 × 262	85.9	64.6	57.1	48.4	Modeled	
80	DBB	MO-194	100 × 224	93 × 203	105.6	78.4	71.8	63.7	Modeled	
PDIP (assumes zero trace length)										
8	P	MS-001			104					41
14/16	N	MS-001			78					32
20	N	MS-001			67					33
24	NT	MS-001			67					25
		· BGA								
256	GFN	MO-151			42				ANAM data	6.2
388	GFW	MO-151			18.9				Model data	

Power Calculation

Reduction of power consumption makes a device more robust and reliable. When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account. Both bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output (I_{CCL}, I_{CCH}, or I_{CCZ}), while a CMOS device has a single value for I_{CC}. These values can be found in the individual data sheets. TTL-compatible CMOS and BiCMOS inputs, when driven at TTL levels, also consume additional current because they may not be driven all the way to V_{CC} or GND; therefore, the input transistors are not switched completely off. This value, known as ΔI_{CC}, also is provided in the data sheet.

Due to the high operating frequencies, there is a strict limit on power consumption in computer systems. Therefore, allowable power consumption for each device on a board must be minimized. Power calculations are made to determine power-supply sizing, current requirements, cooling/heatsink requirements, and criteria for device selection. Power calculation also can determine the maximum reliable operating frequency.

There are two components that establish the amount of power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

Dynamic power consumption results from charging and discharging external load and internal parasitic capacitances. The parameter for CMOS device parasitic capacitance is C_{pd}, which is listed in the data sheet and is obtained using equations 2 and 3:

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_I} - C_{L(eff)} \quad (2)$$

$$C_{L(eff)} = C_L \times N_{SW} \times \frac{f_O}{f_I} \quad (3)$$

To explain the C_{pd} and the method of calculating dynamic power, see Table 3, which indicates the C_{pd} test conditions for AHC devices. The symbols used in Table 3 are:

V = V_{CC} (5 V)
G = ground (0 V)
1 = high logic level = V_{CC} (5 V)
0 = low logic level = ground (0 V)
X = don't care: 1 or 0, but not switching
C = 50% duty cycle input pulse (1 MHz) (see Figure 1)
D = 50% duty cycle input (1/2 frequency) out-of-phase input pulse (see Figure 1)
S = standard ac output load (50 pF to GND)

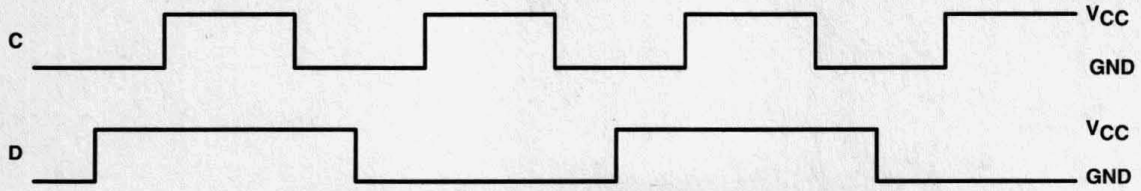


Figure 1. Input Waveform

Table 3 shows the switching of each pin for AHC devices. Once the C_{pd} is determined from the table, the P_D is easy to calculate using equations explained in the following sections.

Although a C_{pd} value is not provided for ABT and LVT, the I_{CC} versus frequency curves display essentially the same information (see Figures 2 and 3). The slope of the curve provides a value in the form of mA/(MHz × bit), which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device without the load current. Equations 4 through 14 can be used to calculate total power for CMOS or BiCMOS devices.

Table 3. C_{pd} Test Conditions With One- or Multiple-Bit Switching

TYPE	PIN NO.																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AHC00	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC02	S	C	0	S	X	X	G	X	X	S	X	X	S	V						
AHC04	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC08	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC10	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC11	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC14	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC32	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC74	1	D	C	1	S	S	G	S	S	X	X	X	1	V						
AHC86	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC138	C	0	0	0	0	1	S	G	S	S	S	S	S	S	S	V				
AHC139	0	C	0	S	S	S	S	G	S	S	S	S	X	X	X	V				
AHC240	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC244	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC245	1	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC373†	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC374‡	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC540	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC541	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC573†	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V
AHC574‡	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V

† All bits switching, but with no active clock signal
‡ All bits switching

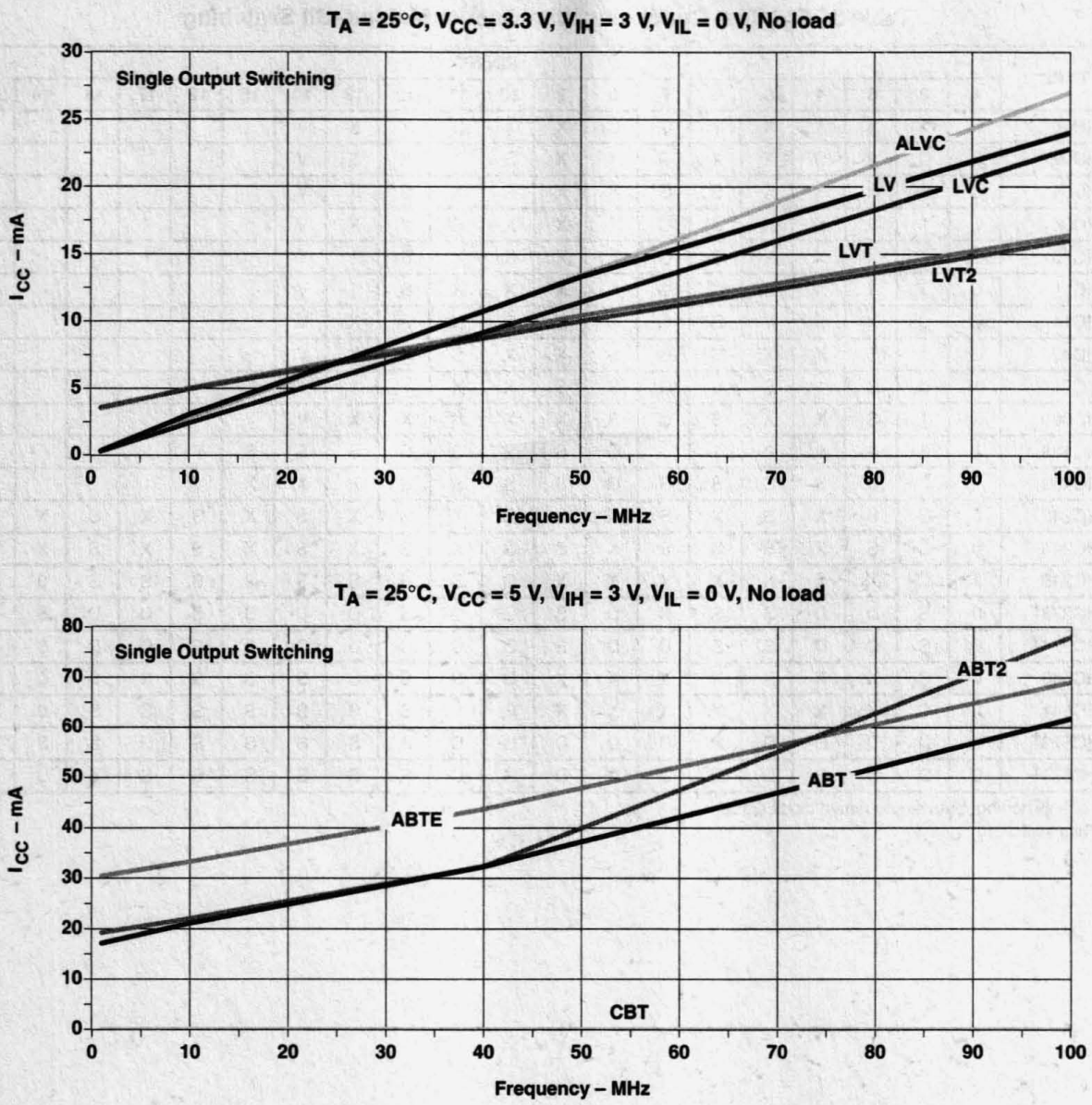


Figure 2. Power Consumption With a Single Output Switching

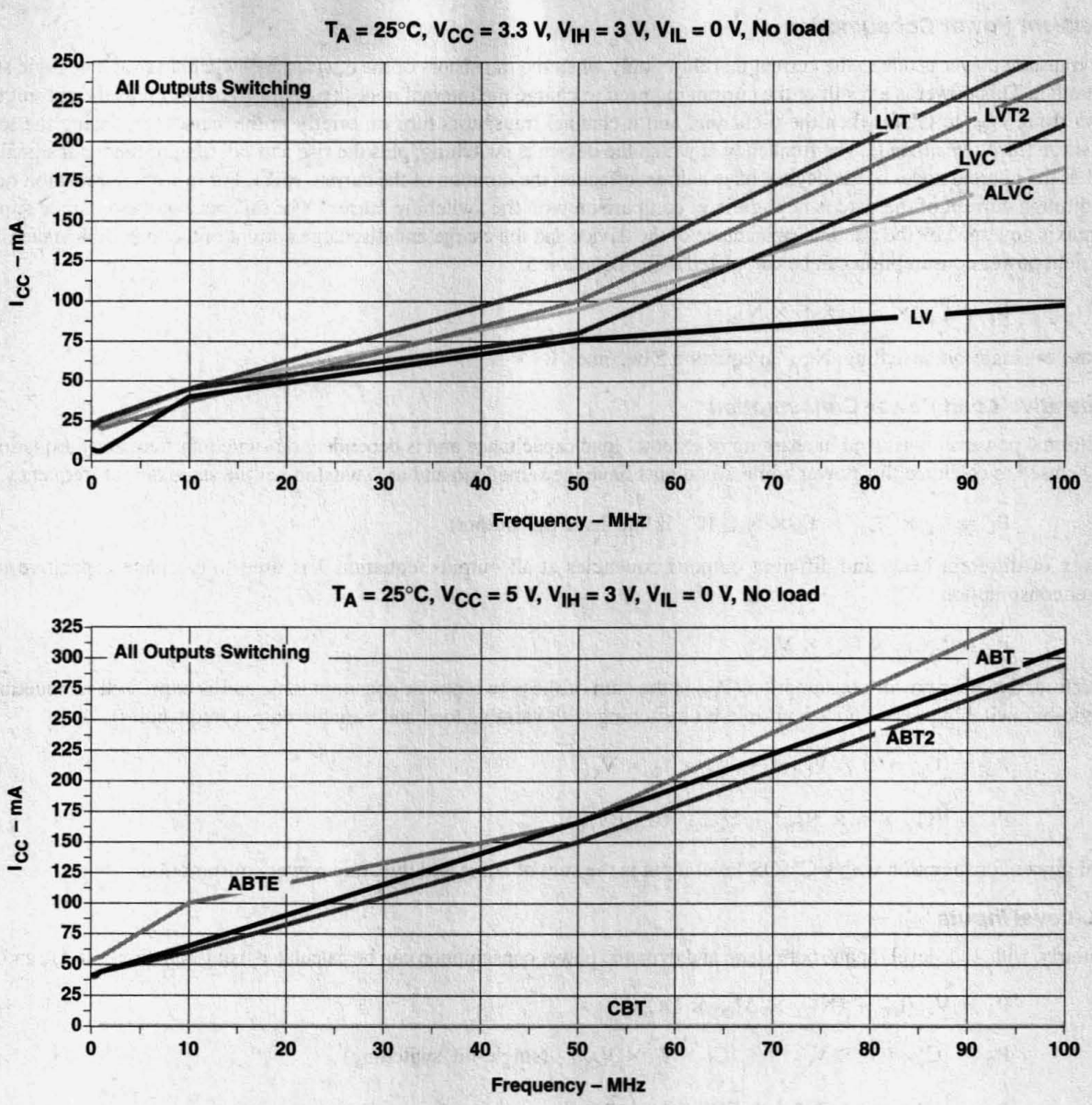


Figure 3. Power Consumption With All Outputs Switching

CMOS

CMOS-Level Inputs

Static power consumption can be calculated using equation 4.

$$P_S = V_{CC} \times I_{CC} \quad (4)$$

The dynamic power consumption of a CMOS device is calculated by adding the transient-power consumption and capacitive-load power consumption.

Transient Power Consumption

The transient power is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This power is a result of the current required to charge the internal nodes (*switching current*) plus the current that flows from V_{CC} to GND when the p-channel and n-channel transistors turn on briefly at the same time during the logic transition (*through current*). The frequency at which the device is switching, plus the rise and fall time of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible in comparison with the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the device and the charge and discharge current of the load capacitance.The transient power consumption can be calculated using equation 5.

$$P_T = C_{pd} \times V_{CC}^2 \times f_I \times N_{SW} \quad (5)$$

In case of single-bit switching, N_{SW} in equation 5 becomes 1.

Capacitive-Load Power Consumption

Additional power is consumed in charging of external load capacitance and is dependent on switching frequency. Equation 6 can be used to calculate this power while all outputs have the same load and are switching at the same output frequency.

$$P_L = C_L \times V_{CC}^2 \times f_O \times N_{SW} \text{ (C_L is the load per output)} \quad (6)$$

In case of different loads and different output frequencies at all outputs, equation 7 is used to calculate capacitive load power consumption.

$$P_L = \Sigma(C_{Ln} \times f_{On}) \times V_{CC}^2 \quad (7)$$

Therefore, dynamic power consumption (P_D) is the sum of these two power consumptions, and is expressed in equation 8 (single-bit-switching case) and 9 (multiple-bit switching with variable load and variable output frequencies):

$$P_D = \left(C_{pd} \times f_I \times V_{CC}^2\right) + \left(C_L \times f_O \times V_{CC}^2\right) \quad (8)$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma\left(C_{Ln} \times f_{On}\right)\right]V_{CC}^2 \quad (9)$$

Total power consumption with a CMOS-level input is the sum of static and dynamic power consumption.

TTL-Level Inputs

Similarly, with TTL-level inputs, both static and dynamic power consumption can be calculated using equations 10, 11, and 12.

$$P_S = V_{CC}[I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)] \quad (10)$$

$$P_D = \left(C_{pd} \times f_I \times V_{CC}^2\right) + \left(C_L \times f_O \times V_{CC}^2\right) \text{ (single-bit switching)} \quad (11)$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma(C_{Ln} \times f_{On})\right]V_{CC}^2 \quad (12)$$

(multiple-bit switching with variable load and frequency)

BiCMOS

Static Power

$$P_S = V_{CC}\left\{DC_{en}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] + (1 - DC_{en})I_{CCZ} + (N_{TTL} \times \Delta I_{CC} \times DC_d)\right\} \quad (13)$$

Where:

$\Delta I_{CC} = 0$ for bipolar devices

NOTE:
For a continuous waveform at 50% duty cycle, $DC_{en} = 1$.

Equation 13 becomes:

$$P_S = V_{CC}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] \quad (14)$$

NOTE:

If half of the time the waveform is high and half of the time the waveform is low and the waveform is switching continuously, $\Rightarrow (N_H = N_L = 1/2\ N_T)$, P_S becomes:

$$P_S = \left(\frac{V_{CC}}{2}\right)(I_{CCH} + I_{CCL}) \quad (15)$$

Dynamic Power

$$P_D = (DC_{em} \times N_{SW} \times V_{CC} \times f \times I_{CCD}) \text{ Condition is } 50\ pF \parallel 500\ \Omega \quad (16)$$

I_{CCD} is calculated with 50 pF || 500 Ω, and given number of outputs switching.

NOTE:

For a continuous waveform at 50% duty cycle, $DC_{en} = 1$.

Dynamic power with external capacitance:

$$P_D = DC_{en} \times N_{SW} \times V_{CC} \times f \times (V_{OH} - V_{OL}) \times (C_L - 50\ pF) + DC_{en} \times N_{SW} \times V_{CC} \times f \times I_{CCD} \quad (17)$$

I_{CCD} is calculated with 50 pF || 500 Ω, and given number of output switching.

Power is also consumed by the upper output driver due to the output resistor (500 Ω in most load circuits for outputs in the data sheet). This power is very small but must be included in the dynamic power consumption calculation. Equation 18 is used to calculate this power consumption.

$$P_{_Res} = (V_{CC} - V_{OH}) \times \frac{V_{OH}}{R} \quad (18)$$

NOTE:

Assume that the output waveform is always at logic high and is not frequency dependent.

Therefore, total dynamic power consumption is:

$$P_{D_TOT} = P_D + P_{_Res} \quad (19)$$

Finally, total power consumption can be calculated as:

$$P_{_Total} = P_{D_TOT} + P_S \quad (20)$$

Where:

V_{CC} = supply voltage (V)
I_{CC} = power-supply current (A) (from the data sheet)
I_{CCL} = power-supply current when outputs are in low state (A) (from the data sheet)
I_{CCH} = power-supply current when outputs are in high state (A) (from the data sheet)
I_{CCZ} = power-supply current when outputs are in high-impedance state (A) (from the data sheet)
ΔI_{CC} = power-supply current when one input is at a TTL level (A) (from the data sheet)
DC_{en} = % duty cycle enabled (50% = 0.5)

DC_d = % duty cycle of the data (50% = 0.5)
N_H = number of outputs in high state
N_L = number of outputs in low state
N_{sw} = total number of outputs switching
N_T = total number of outputs

N_{TTL} = number of inputs driven at TTL levels

fi = input frequency (Hz)
f_O = output frequency (Hz)
f = operating frequency (Hz)
V_{OH} = output voltage in high state (V)
V_{OL} = output voltage in low state (V)
C_L = external-load capacitance (F)
I_{CCD} = slope of the I_{CC} versus frequency curve (A/Hz × bit)

$C_{L(eff)}$ = effective-load capacitance (F)
f_O/f_I = ratio of output and input frequency (Hz)
P_T = transient power consumption
P_D = dynamic power consumption
P_S = static power consumption
$P_{_Res}$ = power consumption due to output resistance
P_{D_TOT} = total dynamic power consumption
$P_{_Total}$ = total power consumption

C_{PD} = dynamic power dissipation capacitance (F)
P_L = capacitive-load power consumption
Σ = sum of n different frequencies and loads at n different outputs
f_{On} = all different output frequencies at each output numbered 1 through n (Hz)
C_{Ln} = all different load capacitances at each output numbered 1 through n

For GTL and BTL/FB devices, the power consumption/calculation is similar to a BiCMOS device with the addition of the output power consumption through the pullup resistor, since GTL is open drain and BTL/FB is open collector.

The total power calculated using these equations should be less than the package power dissipation mentioned in the data sheets. Otherwise, the device might not function properly.

Benefits of Minimizing Power Consumption

Power consumption can be minimized in a number of ways. DC power consumption can be reduced to leakage by using only CMOS logic, as opposed to bipolar and BiCMOS logic. The leakage, in turn, is proportional to the area of diffusion, so the use of minimum-size devices is an advantage. Dynamic power consumption can be limited by reducing supply voltage, switched capacitance, and the frequency at which the logic is clocked. Supply voltage tends to be a system design consideration, and low-power systems use 1.5-V to 3.3-V supplies.

Power consumption is a function of the load capacitance, the frequency of operation, and the supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several other benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heatsinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower temperature stress gradients on the device, and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

Reliability Implications

The IC component power dissipation during operation elevates the device junction temperature. The thermal impedance (θ_{JA} or k-factor) of an IC package is defined as the increase in the junction temperature, above ambient temperature, due to the device power dissipation. Thermal impedance is measured in degrees Celsius per watt. Thermal characteristics of an IC package are commonly described using two indices, Q_{JA} (junction to ambient) and Q_{JC} (junction to case). Controlling the junction temperature within a desired range is critical for proper device functionality and long-term reliability.

Table 4, based on long-term sustained temperatures, shows the relationship between junction temperature and predicted failure rate.

Table 4. Junction Temperature Versus 100,000-Hour Predicted Failure Rate

JUNCTION TEMPERATURE (°C)	FAILURE RATE (%)
100	0.02
110	1
120	11
130	46
140	80
150	96

Higher component temperatures increase the possibility of component wearout due to such failure mechanisms as electromigration and ball-bond intermetallic failures.

Thermal Definitions

Heat — A form of energy associated with the motion of atoms or molecules in solids, and capable of being transmitted through solid and fluid media by conduction, through fluid media by convection, and through empty space by radiation

Conduction Heating — The most commonly recognized form of heat transfer. Metal materials are good conductors of heat and can be quantified by a proportionality constant (k), also known as thermal conductivity. The higher the thermal-conductivity number, the more quickly heat transfer, by means of conduction, occurs. Leadframes are the primary media for conduction heating in plastic ICs; however, mold compound materials play a major role in this type of heat transference.

Convection Heating — The heat transfer by fluid motion between regions of unequal density that result from nonuniform heating. This type of heat transfer is most commonly seen when air is forced across a heated surface, resulting in the cooling of the heat source. Heat is transferred to the air by means of convection heating. The rate of heat transfer depends on the surface area of the heat source and the velocity and physical properties of the air flow. When an IC package is generating heat through normal operation, the IC package can be cooled by applying a constant air flow across the surface of the package.

Radiation — Radiant heat transfer occurs between two objects separated within a vacuum.

Ambient Temperature — The temperature of the surrounding air, usually used as a reference point to calculate the junction or case temperature. This temperature is measured at some specific distance from the IC component.

Case Temperature — The temperature on the package surface measured at the center of the top of the package

Junction Temperature — The temperature of the die inside the package of the IC component

Acknowledgment

The authors of this report are David Holmgreen, Doug Romm, Abul Sarwar, and Ron Eller. The thermal-model program, ThermCAL, was developed by Darvin Edwards.

References

1 Electronic Industries Association, EIA/JEDEC Std JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, August 1996.

2 Darvin Edwards, "Thermal Analysis Using FEA (v1.1)," November 1991.

3 Darvin Edwards, "Development of JEDEC Standard Thermal Measurement Test Boards."

General Design Considerations 1
Backplane Design 2
Device-Specific Design Aspects 3
5-V Logic Design 4
3.3-V Logic Design 5
Clock-Distribution Circuits (CDC) 6
Boundary-Scan IEEE Std 1149.1 (JTAG) Logic 7
Packaging 8
Index 9

Index

θ_{JA}
see thermal impedance

3.3-V interface levels
comparison to 5-V interface levels 5–7

3.3-V market 5–50

3.3-V supply voltage 5–25, 5–49, 8–44

5-V to 3.3-V migration 4–18, 5–25, 5–49, 5–50

5-V to 3.3-V translation 5–3, 5–26
CBT solution 5–7
mechanics 5–8
need for 5–7
when 3.3-V supply line is not provided 4–97

5-V tolerant
3.3-V logic 4–34, 5–17, 5–28
pure 3.3-V V_{CC} level shifters 5–15

A

ABT
see advanced BiCMOS technology

AC termination 4–36
advantages, disadvantages 4–36

AC/ACT
see advanced CMOS technology

active termination 4–71

addressable shadow port (ASP) 7–91, 7–93, 7–94
star configuration, comparison with 7–94

advanced BiCMOS technology (ABT) 1–54, 1–70, 4–7, 4–98, 8–43, 8–45
advantages over other logic solutions 4–7
average output skew 3–8
bus-hold feature 4–12
capacitive load 4–11
comparison to other logic families 4–8
definition 4–9
dynamic power consumption 4–10
end-equipment-specific solutions 4–15
features, benefits 4–7, 4–9, 4–15, 4–16
ground noise 4–10
IEEE 896.1 FB+ backplane-interface standard compliance 4–17
IEEE Std 1149.1 (JTAG) 4–17, 7–6
input structure 3–21
with bus hold 3–28
input characteristics 3–48
input circuit structure 4–10
input transition rise or fall rate 3–22
LVT comparison 5–53
metastable characteristics 3–80
multiple-output switching curves 3–16, 4–11
operating temperature 4–10
output characteristics 3–58
output circuit structure 4–10
output skew 3–7
packaging 4–13, 4–14, 4–15
power consumption
with simultaneous switching 5–68
with single-output switching 5–69
products 4–15, 4–16
propagation delay 4–8, 4–11, 4–12, 4–15
rise time 1–8
signal integrity 4–10
simultaneous switching 1–9, 1–14, 8–25
simultaneous-switching curves 3–10, 3–14
single-switching curves 3–9, 3–11, 3–12, 3–13, 3–15
supply current 4–8
supply-current change of input at TTL level 3–23
target applications 4–15
V_{CC} line disturbance 1–7
voltage swing 4–10
waveforms 3–69

advanced CMOS technology (AC/ACT) 1–63, 3–21
input characteristics 3–47
metastable characteristics 3–80
output characteristics 3–57
performance 4–28
waveforms 3–68

advanced high-speed CMOS technology (AHC/AHCT)
5-V-input tolerant 4–34
ac performance 4–28
advantages over HC 4–26, 4–40
dc specifications 4–33
features 4–40
hex inverter 5–64
I_{CC} versus frequency 5–65
input characteristics 4–30

input circuitry 4–30
input current specification 4–32
input current versus input voltage 4–32
input TTL compatible, with (AHCT) 4–28
input waveform 5–66
interfacing TTL output to CMOS input (AHCT) 4–29
natural migration from HC 4–25
output circuitry 4–33
output drive 4–34
output voltage versus input voltage 4–31
packaging 4–41
partial power down (AHCT) 4–34
performance comparison, HC 4–28
recommended operating range, T_A 4–31
supply-current change specification, ΔI_{CC} 4–32

advanced low-power Schottky (ALS)
input characteristics 3–44
metastable characteristics 3–80
output characteristics 3–53
waveforms 3–64

advanced low-voltage CMOS technology (ALVC) 5–70
dynamic power 5–34
bus hold 3–28
input characteristics 3–50
input transition rise or fall rates 3–22
output characteristics 3–60
power consumption
with simultaneous switching 5–68
with single-output switching 5–69
propagation delay 5–30
versus load capacitance 5–32
versus number of outputs switching 5–31
versus operating free-air temperature 5–30
supply-current change of input at TTL level 3–23
waveforms 3–70

advanced Schottky (AS) 4–49
circuit models 4–52
input characteristics 3–45
input, output characteristics 2–48
load management 4–49
metastable characteristics 3–80
output characteristics 3–55
overshoot, undershoot 4–51
propagation delay 4–49
ringing 4–51
rise, fall times 4–50
spatial considerations 4–72
system model 4–54
waveform 3–65

AHC/AHCT
see advanced high-speed CMOS technology

aliasing 7–164

ALS
see advanced low-power Schottky

ALVC
see advanced low-voltage CMOS technology

ambient temperature 8–100, 8–111

analog power filter 6–21

antenna effect 6–42

AS
see advanced Schottky

ASP
see addressable shadow port

B

backdriving 1–74
simultaneous 1–77

backplane 5–51
capacitance 8–44
IEEE Std 1149.1 (JTAG) 7–87
impedance 8–44
wiring 2–72

backplane model
all boards connected 2–7
one driver, one receiver connected 2–7

backplane transceiver logic (BTL) 2–7, 2–73, 4–17
advantages over CMOS/TTL 2–8, 2–23
better noise immunity 2–11
design considerations 2–16
family input and output structure 2–9
maximum number loads 2–16, 2–17
open collector 8–81, 8–110
output capacitance 2–13
power consumption 2–10
propagation delay, t_{pd} 2–24
signal integrity 2–15
slew rate 2–13
suppliers 2–24
switching standards 2–23
UBT™ 2–27

balanced drive output
see reduced drive output

BCT
see BiCMOS technology

bed-of-nails test
see in-circuit test

Bergeron method 2–35, 3–95
Bergeron diagram 2–38
for short-circuited line 2–39
derivation 2–35
determine line reflections 2–35
nonlinear line terminations 2–47

BiCMOS
see bipolar CMOS

BiCMOS technology (BCT) 1–54, 8–43, 8–45
dynamic power 8–80, 8–109
IEEE Std 1149.1 (JTAG) 7–6, 7–144, 7–147
input characteristics 3–48
metastable characteristics 3–80
output characteristics 3–58
static power 8–80, 8–108
waveforms 3–68

bidirectional bus 3–24

bidirectional switching
CBT solution 5–7

bipolar
circuits 1–51, 1–54, 1–59
damping resistor, with 1–35

bipolar CMOS 1–33, 3–21
advantage over CMOS in live-insertion applications 2–65
damping resistor, with 1–35
input characteristics 3–21

BIST
see built-in self-test

BIT
see built-in test

board skew 6–53

boundary scan 7–3, 7–5, 7–17, 7–101
also IEEE Std 1149.1 (JTAG), built-in self-test (BIST)
4-wire test access port (TAP) 7–25
advantages 7–61
advantage over in-circuit test 7–25
architecture 7–117, 7–118
basics 7–51
board-level test 7–64
cell 7–51
comparison to in-circuit test 7–26
control architecture 7–63
definition 7–143
design partition 7–124
designer's perspective 7–49, 7–57
idea 7–63
instructions
BOUNDARY BIST 7–110
BOUNDARY READ 7–110
BOUNDARY SELF-TEST 7–110
BYPASS 7–146
CELLTST 7–146
CLAMP 7–110, 7–146
EXTEST 7–146
HIGHZ 7–146
INTEST 7–146
READBN 7–146
RUNT 7–146
SAMPLE 7–146
SCANCN 7–146
TOGGLE/SAMPLE 7–109
TOPHIP 7–146
octal parts 7–132
scan-path support devices 7–82
success stories 7–55
system-level test 7–82
training 7–48

BTL
see backplane transceiver logic

BTL-to-TTL translation 4–17

built-in self-test (BIST) 7–5, 7–65, 7–67, 7–101
also IEEE Std 1149.1 (JTAG), boundary scan

built-in test (BIT) 1–74, 7–6

bus conflict 1–73
avoidance 2–68
cause 2–68
curve for calculating short-circuit currents 2–68
determining short-circuit current 1–69
during power-on phase of system 1–73
output-stage conditions 1–70
prevention 1–73, 2–79

bus contention
causing 4–88
CBT solution 4–90
definition 4–88

bus control 3–24

bus disruption 4–88
effect on data flow 4–88
effect on signal integrity 4–88

bus isolation 4–87
solution 4–90

bus switches 4–87, 5–7
also crossbar technology (CBT)
5-V to 3.3-V translation 4–97
convert TTL logic to hot card-insertion capability 4–97
replacement for drivers, transceivers in bus applications 4–97

bus hold 3–26, 5–19, 5–38
advantages, benefits 4–12
definition 3–26
devices with 3–26
input characteristics
3.3-V 3–29
5-V 3–29
minimum specification 3–32
power consumption, impact on 3–31
replacement for pullup resistor 5–53
supply current versus input voltage 3–30

bus-hold cell
stand-alone 3–26
typical 3–26

bus-interface circuits
monitoring 2–69
technology and packaging evolution 4–19

bypass capacitor
capacitive storage 1–9
connecting to a line 2–70
with voltage bias 2–71
considerations 1–7
definition 1–7
lead inductance 1–8
placement 1–8, 1–14
size 1–14
ways to calculate 1–13

C

capacitance 1–68, 8–21, 8–43, 8–82
calculation 8–77, 8–104
power-dissipation calculation 4–29

capacitive-load power, P_L
calculation 5–62
consumption 8–79, 8–108

capacitive power dissipation
calculation 4–29

capacitor
see bypass capacitor

case temperature 8–111

CBT
see crossbar technology

CDC
see clock-distribution circuits

CDC5XX platform 6–3
decoupling 6–21
design considerations
configurations 6–11, 6–12, 6–13
driver output impedance 6–18
jitter 6–16
propagation delay 6–14
features 6–8, 6–9
functional block diagram 6–10
power supply 6–21
transmission line analysis 6–19
typical jitter performance 6–17
typical output impedance 6–19
typical V/I curves 6–20

change in power dissipation, ΔI_{CC}
misconceptions about 5–15

chip junction temperature 8–100

clamping diode 3–27
lower 3–27
upper 3–27

clock distribution 6–27

clock-distribution circuits (CDC) 6–23, 6–42
also CDC5XX platform
10% rule 6–29, 6–63
duty cycle 6–39
EMI evaluation results 6–46, 6–47
EMI prevention 6–33
high-speed design considerations 6–31
jitter 6–65
output skew, $t_{sk(o)}$ 6–63
phase-detector block 6–64
phase-lock loop 6–59
power dissipation 6–30
process skew 6–63
propagation delay 6–63
radiated emissions 6–40
transmission line 6–40

clock drivers
see clock-distribution circuits

clock edge 1–61

clock generation 6–27

clock network 6–27

CMOS
see complementary metal oxide semiconductor

complementary metallic oxide semiconductor (CMOS) 1–33, 3–21, 8–7
ΔI_{CC} typical current 5–16
calculating C_{pd} 5–64
capacitive-load power consumption 8–79, 8–108
circuits 1–55
comparison to BiCMOS 5–70, 8–110
comparison to bipolar 5–70
damping resistor, with 1–35
dynamic power consumption 8–79, 8–107
input characteristics 3–21
input structure 5–16
inverter circuit 1–20
power consumption 5–55, 5–60, 5–70
power-consumption calculations with TTL-level inputs 8–79, 8–108
power dissipation 4–28
power-dissipation capacitance, C_{pd} 5–55, 5–63
power economy 5–70
static power consumption 8–79, 8–107
supply current 1–20
input voltage with one input 3–22
input voltage with 36 inputs 3–24
transient power consumption 8–79, 8–108

conductance 1–20

conduction 8–71, 8–111

convection
see conduction

coupling factor 8–21

critical damping 2–76, 2–77

crossbar technology (CBT) 4–98
5-V to 3.3-V translation 5–7
bidirectional switching 5–7
definition 4–95
eliminates need for external diode 5–10
functions 4–99
output isolation 4–89
power consumption
with simultaneous switching 5–68
with single-output switching 5–69
power-up high-impedance state 4–99
preventing false switching 4–88
propagation delay 4–95
resistance 4–95
test conditions 4–89
to translate from 5-V TTL devices that are not 5-V tolerant 5–28

crosstalk 1–28
also electromagnetic compatibility, electromagnetic interference, interference, noise, radiation
reduction 1–25, 4–72

current paths 1–19

cycle-to-cycle jitter 6–8, 6–16
calculation 6–16

D

D-type flip-flop 3–155, 4–16, 6–64
bipolar master-slave 3–75
timing conditions 3–76

damping resistor 6–42
also output-damping resistor
effect of 1–34

data transceiver
basic logic 5–16

delay time 1–67

designing more reliable systems
bus control 3–24
bus hold 3–26
pulldown resistor 3–25
pullup resistor 3–25

device power dissipation 8–100

device processing
evolutions 8–43

digital phase-locked loop (DPLL)
see phase-lock loop

diode termination
also active termination
advantages, disadvantages 4–36

DIP
see dual in-line package

dissipation
reduction 2–51

distributed load
schematic diagram 4–64

double-sided surface mounting
eliminating the need for 2–29

driver output impedance 6–18

driver output type
balanced, light drive 1–43
damping resistor 1–43
or balanced drive 1–43
or light drive 1–43
decision tree 1–43
high drive 1–43

driving
3.3-V LVC to 5-V CMOS 5–27, 5–28
3.3-V LVC to 5-V TTL 5–27, 5–28
5-V CMOS to 3.3-V LVC 5–27, 5–28
5-V TTL to 3.3-V LVC 5–27, 5–28

dual in-line package (DIP) 8–17, 8–21, 8–25, 8–41

dynamic power, P_D 6–30, 8–80, 8–109
calculation 5–25, 5–34, 5–61, 5–63
comparison of logic families 5–34
consumption 4–10, 8–107
transient power, P_T 5–61

E

edge connector test
see functional test

effective load capacitance, $C_{L(eff)}$
calculation 5–66

electrical parameters
capacitance 8–82
inductance 8–82
resistance 8–82

electromagnetic compatibility (EMC) 1–22, 1–28
aspects of 1–19
determined by 1–19

electromagnetic energy
determined by 1–19
improving 1–20

electromagnetic interference (EMI)
causes 1–21
prevention 6–48
CDC 6–33
shielding techniques 6–37
suppression 1–21

electrostatic discharge (ESD)
definition 4–26
input-protection circuitry 4–26
output-protection circuitry 4–27
protection against 2–64, 4–26

EMC
see electromagnetic compatibility

EMI
see electromagnetic interference

enhanced transceiver logic (ETL) 2–73
bus-interface control 2–74

ESD
see electrostatic discharge

ETL
see enhanced transceiver logic

F

fall time
see rise/fall times

false switching 4–88
CBT solution 4–88

fanout 4–62, 6–14, 6–28
correction
series termination 4–70
parallel termination 4–70
definition 4–62
effects on propagation delay 4–65
influence on ringing 4–65
influence on rise and fall times 4–63
influence on transmission-line model 4–62
overshoot 4–66
propagation delay 4–65
rise, fall time 4–64

F logic
input characteristics 3–46
output characteristics 3–56
metastable characteristics 3–80
waveforms 3–66

FIFO
see first-in, first-out memories (FIFO)

fine-pitch packaging 4–13

first-in, first-out memories (FIFO) 8–3, 8–7

flip-flop 1–61, 3–75
also D-type flip-flop
oscillogram 3–78
going into metastable state, probability of 3–77
synchronize two signals, using to 3–77

floating inputs 3–23, 5–53
avoiding 3–24, 5–38

floating state
definition 3–24
results 3–24

frequency discriminator 3–145

functional test 7–62

Futurebus 2–23
layout 2–25
UBT™ 2–27

G

ganged outputs 6–49
  to eliminate output skew 6–53

gate configuration
  without matching 2–48

ground bounce 4–37
  measurement 4–39
  minimizing 4–38
  test circuit 4–39

ground noise 4–10

ground-plane effects
  advantages 4–72

GTL
  see Gunning transceiver logic

guard ring 4–28
  also latchup

Gunning transceiver logic (GTL) 2–7
  advantages over CMOS/TTL 2–8
  better noise immunity 2–11
  design considerations 2–15
  family output, output structure 2–8
  maximum number of loads 2–16, 2–17
  open drain 8–81, 8–110
  output capacitance 2–13
  power consumption 2–10
  signal integrity 2–15
  slew rate 2–13

H

HC/HCT
  see high-speed CMOS technology

heat 8–111

hex inverter 5–64

high drive 1–37

high-speed CMOS technology (HC/HCT)
  characteristics 4–25
    input 3–47
    output 3–57
  features 4–40
  input TTL compatible, with (HCT) 4–28
  metastable characteristics 3–80
  performance comparison, AHC 4–28
  waveforms 3–67

high-speed digital systems
  low-swing interface requirements, with 2–7

hot card insertion
  see live insertion

I

IC
  see integrated circuit

ideal matching 2–56

ideal voltage source
  turning on
    open circuit at end of line 2–37
    short circuit at end of line 2–39

IEEE Std 1149.1 (JTAG) 1–74, 7–5
  also boundary scan, built-in self-test (BIST)
  ACT 7–76
  addressable shadow port (ASP) 7–31, 7–91
  advantages 7–47, 7–65
  application interconnection test 7–38
  architecture 7–107, 7–118
  backplane applications 7–89
  BCT 7–51
  board level 7–31, 7–64, 7–66, 7–83
  chip level 7–68
  comparative test-cost model 7–46
  customer issues 7–47, 7–118, 7–122
  definition 7–117
  design tradeoffs 7–113, 7–119, 7–131
  driving forces 7–17, 7–45, 7–61
  generating patterns 7–6
  hierarchical access 7–31, 7–33
  impact on reliability 7–127
  instructions
    BOUNDARY BIST 7–110
    BOUNDARY READ 7–110
    BOUNDARY SELF-TEST 7–110
    BYPASS 7–108, 7–146
    CELLTST 7–146
    CLAMP 7–110, 7–146
    EXTEST 7–108, 7–146
    HIGHZ 7–146
    INTEST 7–146
    READBN 7–146
    RUNT 7–146
    SAMPLE 7–108, 7–146
    SCANCN 7–146
    TOGGLE/SAMPLE 7–109
    TOPHIP 7–146
  interrupt pin and application 7–107
  linear-feedback shift registers (LFSR) 7–7, 7–159
  logic cluster test 7–66
  mean time between failures (MTBF) 7–131
  mean time to repair (MTTR) 7–131
  memory array 7–5, 7–17, 7–18, 7–132
  package size 7–120
  parallel application self-test 7–38
  partitioning designs 7–73, 7–123
  power 7–122

printed wiring board design 7–123
product pinouts 7–147
propagation delay 7–122
parallel signal analyzer (PSA) 7–7, 7–163
reliability 7–122, 7–137
scan architecture
ring configuration 7–75
star configuration 7–75
scan path 7–53, 7–67, 7–79
scan-path selector 7–81, 7–86
scan-path support devices 7–82
SCOPE™ architecture 7–105
system level 7–69, 7–125, 7–151
test-access port (TAP) 7–31, 7–106, 7–145
test-bus and interrupt-pin connections 7–107
test-bus controller (TBC) 7–31, 7–126
timing diagram 7–7
training 7–48
virtual nails 7–65, 7–124
wiring interconnects, verifying 7–148

impedance 1–25, 1–33, 1–35, 1–52, 1–53, 1–54, 1–59, 2–39, 2–45, 2–54, 6–40
antenna effect 6–42
calculation 3–99, 8–44
determination 3–93
microstrip line, of a 3–101
minimizing 6–40
rule of thumb, mismatch 1–35
strip lines 3–99
supply lines 1–19

impedance matching 1–33, 3–93, 6–41, 6–48
effects 6–44
methods of 6–41
termination methods
ac 3–94
series resistor 3–94
single resistor to 2-V 3–94
single resistor to GND 3–94
spilt resistor 3–94

in-circuit test 7–23, 7–62
comparison to boundary scan 7–26

incident wave 1–33
also waveforms, signal reflection

inductance 1–22, 1–62, 8–21, 8–82
calculation 2–76
formula
parallel wires 1–8
minimizing 1–8

input skew, $t_{sk(i)}$ 3–7, 6–28

inputs
characteristics 3–41
curve 3–39
excessive currents 1–58
internal diodes 2–65
power consumption
with bus hold 3–31
without bus hold 3–31
unused 1–56, 1–57
withstanding voltages 2–65

integrated circuit (IC)
fabrication 5–29
internal construction 2–64

interference 1–28
also crosstalk, electromagnetic compatibility, electromagnetic interference, noise, radiation
suppression 1–27
signal lines 1–24

internal resistance 1–67

interrupt synchronization 3–82

J

JEDEC
see Joint Electronics Device Engineering Council

jitter 3–77, 3–79, 6–16, 6–21
calculations 6–16
definitions 6–8
measurement methodology test setup 6–16
phase detector, of 6–65
types
cycle-to-cycle 6–8
peak-to-peak 6–8
RMS 6–8

Joint Electronics Device Engineering Council (JEDEC) 8–55
standard JESD51 8–99
thermal test-board specifications 8–72

joint test action group (JTAG)
see IEEE Std 1149.1 (JTAG), boundary scan

JTAG
see joint test action group (JTAG)

junction temperature 8–111
versus long-term reliability comparison 8–72

L

latchup
  definition 4–27
  guard ring 4–28
  protection 4–27

lattice diagram 4–61

lead pitch 8–41, 8–61, 8–72
  component placement 8–62, 8–67

leakage current, I_{lkg}
  calculation 5–61

LFSR
  see linear-feedback shift register

light drive
  see reduced drive output

limit skew, $t_{sk(l)}$ 3–7, 6–7, 6–15, 6–29

line
  inductance 3–99
  loop 1–19
  switching 2–46
  turning off 2–45
  turning on 2–40
  without termination
    high-to-low transition 2–56
    low-to-high transition 2–55

line disturbance 1–7
  relation to
    capacitive load 1–12
    distance 1–9
    frequency 1–10, 1–11

line reflection 1–75, 2–45, 2–54, 3–27, 3–93
  avoidance of 2–44
  Bergeron method 2–35
  switching a line, when ($Z_O < R_t$) 2–46, 2–47

line termination 2–37, 5–40
  line reflections 2–41
  matching generator source impedance 2–44
  resistor network 2–57
  resistor to ground 2–56
  series resistor at generator output 2–57
  techniques
    diode 5–41
    resistor and capacitor 5–41
    series resistor 5–41
    single resistor 5–41
    split resistor 5–41
  terminating impedance at line end 2–44
  when ($R_O < Z_O$) 2–44
  when ($R_O < Z_O < R_t$) 2–43
  with a resistor 2–51

line transmission theory 1–25

linear-feedback shift register (LFSR) 7–68, 7–159
  maximal length 7–160
  potential problems 7–163
  pseudorandom pattern generation 7–160

live insertion
  crossbar switches, with 4–97, 4–98
  definition 2–63
  low-voltage BiCMOS technology (LVT), with 5–54
  operating conditions 2–66
  resulting logic states 2–66
  simple circuit modifications to obtain predictable circuit behavior 2–67

load resistance 3–93

lock detection circuit 3–155

logic timeline 4–19

long-term jitter
  see peak-to-peak jitter

low supply voltage
  behavior of digital circuits 1–51

low-power pulse generator 3–142

low-power Schottky (LS) 1–68, 3–131
  also LS123, LS297
  input characteristics 3–41
  metastable characteristics 3–80
  output characteristics 3–51
  waveforms 3–62

low-voltage BiCMOS technology (LVT) 5–17
  5-V to 3.3-V interface 4–18
  ABT comparison 5–53
  bus hold 5–18, 5–53
  characteristics 5–52
  dynamic power 5–34
  input structure 3–21
    with bus hold 3–28
  input characteristics 3–50
  input transition rise or fall rate 3–22
  live insertion 5–54
  optimized 3.3-V I/O 4–18
  output characteristics 3–60
  output structure 5–53
  partial power down 5–18, 5–54
  power consumption
    with simultaneous switching 5–68
    with single output switching 5–69
  propagation delay
    versus load capacitance 5–33
    versus number of outputs switching 5–31
    versus operating free-air temperature 5–30

supply current change of input at TTL level 3–23
supply voltage 4–18
versus FCT 5–17, 5–18
waveforms 3–70

low-voltage CMOS technology (LV/LVC) 5–28
AC performance 5–29
bus hold 3–28, 5–38
bus-hold specifications, $I_{I(hold)}$ 5–39
change in supply current (I_{CC}) specifications 5–38
characterization information 5–21
dynamic power 5–34
input characteristics 3–49, 5–35
input current loading 5–37
input current specifications 5–37
input current versus input voltage 5–36
input leakage current versus input voltage 5–37
input structure 3–21
output characteristics 3–59, 5–39
output circuitry 5–40
output drive 5–40
output voltage versus input voltage 5–36
partial power down 5–40
power considerations 5–33
power consumption
with simultaneous switching 5–68
with single-output switching 5–69
propagation delay
versus load capacitance 5–32
versus number of outputs switching 5–31
versus operating free-air temperature 5–29
rise/fall times 3–22
supply current versus input voltage 5–35
termination 5–38
TTL levels 3–23
waveforms 3–69

LS
see low-power Schottky

LS123 3–131
also low-power Schottky
applications
delayed-pulse generator with override 3–140
frequency discriminator 3–145
low-power pulse generator 3–142
missing-pulse detector 3–141
negative, positive edge-triggered one-shot 3–143
pulse-duration detector 3–144
device-to-device variation 3–137
features 3–131
logic diagram 3–131
rules for operation 3–132
special considerations 3–135

LS297
also low-power Schottky
applications 3–165
design considerations 3–163
features 3–151
floppy disk controller application 3–160
I/D circuit waveforms 3–153
lock-detection circuit and waveforms 3–155
low-power Schottky 3–147
phase-detector input versus output with zero phase error 5–152
PLL 3–151, 3–153
ripple-cancellation circuit 3–154

LV/LVC
see low-voltage CMOS technology

LVT
see low-voltage BiCMOS technology

M

matched line
signal response for 2–51

matching
nonideal 2–52
series resistor, by 2–54

mean static phase error 6–16

mean t me between failures (MTBF) 3–77, 3–79, 7–131
equation 3–80, 3–81

mean time to repair (MTTR) 7–131

memory arrays
IEEE Std 1149.1 (JTAG) 7–5, 7–17, 7–18, 7–132
importance of damping-resistor solution 1–34

memory test
improving speed 7–5

metastability 3–75, 3–82
also metastable

metastable
also metastability
characteristics 3–80
response 3–75
state
different output signals 3–77
timing 3–76

MicroGate
5-pin pinout 4–42
advantages 4–42
definition 4–42

microstrip line 4–57
characteristics 4–58
structure 4–57

missing-pulse detector 3–141

mixed mode 4–18, 5–7, 5–15, 5–51
also mixed voltage

mixed voltage 5–11
also mixed mode

MLC
see multilayer ceramic-chip capacitor

MOS transistor 2–77

MOSFET switch
leading to false switching 4–87
signal disruption 4–87

MTBF
see mean time between failures

MTTR
see mean time to repair

multilayer ceramic-chip capacitors (MLC) 1–8

N

node forcing
see backdriving

noise 3–22, 5–43, 6–21
also crosstalk, electromagnetic compatibility, electromagnetic interference, interference, radiation
minimizing 1–7
reduction 4–35, 5–43

O

open collector 8–81

open drain 8–81

open-circuit line
with ($R_O < Z_O < R_t$) 2–43

oscillation 2–77, 4–38

oscillator 1–26
circuit 1–19
layout of metallization 1–19
voltage controlled 6–10

oscillogram 3–39
clock, data signal on flip-flop 3–78

oscilloscope 3–102

output
balanced drive 1–37
curve 3–39
high drive 1–37
isolation 4–89
light drive 1–37
load effects 1–10
typical types 3–39, 3–40

output drive
also output-damping resistor
balanced, light 1–33
specifications
selected TI logic devices 1–36

output edge control (OEC™) 2–24

output skew, $t_{sk(o)}$ 3–7, 6–7, 6–28, 6–53, 6–63
definition 3–7
eliminating with ganged outputs 6–53

output-damping resistor 1–33, 4–69
3.3-V buffer 1–42
5-V buffer 1–42
also damping resistor
implementation 1–35
product-line offerings 1–35
TI device nomenclature 1–35
transceivers 1–44
vendor cross reference 1–42

overdamping 2–76, 2–77

overload
prevention 2–68

overshoot
see signal overshoot

overvoltage
see signal overshoot

P

packaging 8–37
area comparison 8–12, 8–56
PLCC 8–11
PQFP 8–11
SOIC 8–11
SSOP 8–11
TQFP 8–11
capacitance 8–21
comparison 8–42, 8–101
coupling factor 8–21
diagrams 8–42
dimensions
20-pin SOIC 8–18
20-pin SSOP 8–18
20-pin TSSOP 8–18
20-pin DIP 8–17
48-pin SSOP 8–19
48-pin TSSOP 8–19
100-pin TQFP 8–20
dry pack 8–10

electrical characteristics
20-pin TSSOP 8–23
20-pin SOIC 8–22
20-pin SSOP 8–22
20-pin DIP 8–21
48-pin TSSOP 8–24
48-pin SSOP 8–23
100-pin TQFP 8–24
evolutions 8–41
inductance 8–21
lead pitch 8–41
medium pin count 8–3
moisture sensitivity 8–9, 8–10
package dimensions
PLCC 8–11
PQFP 8–11
SOIC 8–11
SSOP 8–11
TQFP 8–11
packing methods 8–10
propagation delay 8–46
quantities 8–10
relation to delay time 8–28
falling edge 8–29
rising edge 8–29
reliability implications 8–111
simultaneous switching 8–25, 8–29
20-pin TSSOP 8–27
20-pin SOIC 8–26
20-pin SSOP 8–26
20-pin DIP 8–25
48-pin TSSOP 8–28
48-pin SSOP 8–27
100-pin TQFP 8–28
tape and reel 8–90
test sockets 8–12
thermal characteristics 8–95
20-pin TSSOP 8–33
20-pin SSOP 8–32
20-pin SOIC 8–31
20-pin DIP 8–30
48-pin TSSOP 8–35
48-pin SSOP 8–34
100-pin TQFP 8–36
thermal definitions 8–111
thermal impedance 4–15, 8–43, 8–102
timeline 8–41
trends 8–56
TVSOP 8–49

parallel outputs
see ganged outputs

parallel signal analyzer (PSA) 7–159, 7–163, 7–164

parallel termination 6–42
technique 4–68
waveform 4–68

parasitic transistor 1–59

partial power down 4–34, 5–18, 5–40
low-voltage BiCMOS technology (LVT), with 5–54

PDIP
see plastic dual in-line package

peak-to-peak jitter 6–8, 6–16

period jitter
see peak-to-peak jitter

phase error, Φ_e 3–156

phase-lock loop (PLL) 3–147, 3–151, 3–163, 3–164, 6–3, 6–59
benefits 6–63
block diagram 6–64
drawbacks 6–66
elements 3–151
latched-phase data, with 3–157
microprocessor control of bandwidth and center frequency, with 3–158
transfer characteristics (in lock) 3–153

plastic dual in-line package (PDIP) 4–13

plastic J-leaded chip carrier (PLCC) 4–13, 8–7
comparison to SOIC 4–13
packing methods and quantities 8–10
test sockets 8–12
thermal impedance, θ_{JA} 8–8

plastic quad flat package (PQFP) 4–13, 8–7
packing methods and quantities 8–10
test sockets 8–12
thermal impedance, θ_{JA} 8–8

PLCC
see plastic J-leaded chip carrier

PLL
see phase-lock loop (PLL)

power
calculation 5–34, 5–63, 8–77, 8–80, 8–81, 8–104
components of 5–59
economy 5–70

power consumption 3–21
minimizing 8–110
reduction 5–25
with all outputs switching 5–68
with single-output switching 5–69

power dissipation 1–70, 2–10, 4–29, 6–30
also change in power dissipation, ΔI_{CC}
capacitive, P_c 4–28
charging capacitance of bus line, P_C 1–72
high level, P_{conh} 1–70
output supplying low level, P_{conl} 1–69
quiescent, P_q 4–28
total, P_T 1–71
transient, P_t 4–28

power-dissipation capacitance, C_{pd}
calculation 5–33, 5–55, 5–64
CMOS 5–63
measurement procedures 5–64
test conditions
with one-bit switching 5–67
multiple-bit switching 5–67

power-up 3-state 2–65, 2–68
definition 2–65

powered-up subsystem
changing 1–56

PQFP
see plastic quad flat package

process geometries 8–44

process skew, $t_{sk(pr)}$ 3–7, 6–7, 6–28, 6–53, 6–63

propagation delay 6–14, 6–63
ABT 4–15
definition 4–49
fanout 4–65
large capacitive load 1–65
negative undershoot at outputs 1–64
several outputs switching simultaneously 1–62

PSA
see parallel signature analyzer

pulldown resistor 3–25, 6–41

pullup resistor 1–55, 1–73, 3–25
recommended, when 3–26
avoid, when to 3–26

pulse skew, $t_{sk(p)}$ 3–7, 6–28, 6–53

pulse width
relationship to amplitude

pulse duration
calculation 3–133
detector 3–144

Q

quad flat package (QFP) 8–41, 8–63

R

radiated emissions 6–40
comparisons 6–43
test setup 6–43

radiation 1–28, 8–71, 8–111
also crosstalk, electromagnetic compatibility, electromagnetic interference, interference, noise
reduction 1–23

READY input 3–84
synchronization 3–85

READY signal
timing conditions 3–84

real voltage source
switching a line 2–46
turning on
terminated line 2–40
unterminated line 2–42
turning off 2–45

reduced-drive output 1–37
versus output-damping resistor 1–36

reflection
see signal reflection

reliability 8–111
see designing more reliable systems

resistance 3–39, 8–82

ringing 6–48
definition 4–51
reduction 4–69, 4–71

ripple-cancellation circuit 3–154

rise/fall times 1–61, 2–16, 4–49
fanout 4–64

RMS jitter 6–8, 6–16
calculation 6–16

S

S
see Schottky logic

Schottky logic (S)
input characteristics 3–42
output characteristics 3–52
metastable characteristics 3–80
waveforms 3–63

SCOPE™ architecture
see IEEE Std 1149.1 (JTAG)

series damping resistor 4–69
also output-damping resistor

series termination 4–36, 4–69, 6–18
advantages, disadvantages 4–36
effect on propagation delay 4–70
technique 4–69
waveform 4–69, 4–70
when appropriate 4–70

shift register 1–62

shrink small-outline package (SSOP) 2–10, 3–23, 4–13, 4–14, 4–41, 8–7, 8–18, 8–19, 8–22, 8–23, 8–26, 8–27, 8–41, 8–57, 8–85
bus-interface usages 8–46
memory driver usages 8–44
packing methods and quantities 8–10
test sockets 8–12
thermal impedance, θ_{JA} 8–8

Shrink Widebus™ 4–13, 4–14

shunt termination
advantages, disadvantages 4–35

signal amplitude
relationship to V_H, V_L 1–60

signal distortion 1–35
avoiding 2–35

signal integrity 4–10, 4–37, 5–43

signal overshoot 1–36, 1–40, 1–58, 1–77, 2–76, 3–93, 4–38, 4–49, 6–44, 6–48
avoiding 3–27
definition 4–51
fanout 4–66
suppressing 1–33

signal reflection 1–33, 2–38, 4–59
reduction 4–35

signal undershoot 1–36, 1–40, 1–58, 1–77, 3–93, 4–36, 4–38, 4–49, 4–87, 6–44, 6–48
avoiding 3–27
definition 4–51
preventing 4–89
suppressing 1–33

signal waveform
see waveform

simultaneous switching 2–8, 2–11, 3–8, 3–22, 4–37, 4–41, 5–43, 5–64
noise waveform 4–39
power consumption 5–68
reduction of impact 5–43

skew
calculations 6–29
definition 3–7, 6–28
minimizing 6–49
reducing pin-to-pin 2–29
types
board 6–53
input skew, $t_{sk(i)}$ 3–7, 6–28
limit skew, $t_{sk(l)}$ 3–7, 6–7, 6–29
output skew, $t_{sk(o)}$ 3–7, 6–7, 6–28, 6–53
process skew, $t_{sk(pr)}$ 3–7, 6–7, 6–28, 6–53
pulse skew, $t_{sk(p)}$ 3–7, 6–28, 6–53

skew budget 6–29

slew-rate control 2–24

slow input edge rate 3–22

small-outline integrated circuit (SOIC) 4–13, 4–14, 4–41, 8–7, 8–18, 8–22, 8–26, 8–41
comparison to PLCC 4–13
packing methods and quantities 8–10
test sockets 8–12
thermal impedance, θ_{JA} 8–8

SOIC
see small-outline integrated circuit

spectrum analyzer 6–43

split-rail level shifters 5–15

split termination 2–51, 2–57

SSOP
see shrink small-outline package (SSOP)

static phase error 6–16

static power 5–59, 8–79, 8–80, 8–107, 8–108
calculation 5–34
consumption 5–60

strip line
structure 4–59
characteristics 4–59

supply voltage
avoidance of disturbances 2–75
calculating with lattice diagrams 4–61
decoupling 1–21
partially switched off
behavior of digital circuits 1–54
switched off 1–51
behavior of digital circuits 1–51
bipolar circuits 1–51
CMOS circuits 1–53
using an inductor 1–23

switch-on current
limiting 2–77

switching standards
3.3-V CMOS 5–51
3.3-V TTL 5–26, 5–51
5-V CMOS 5–7, 5–26
5-V TTL 5–7, 5–26, 5–51
comparison 5–26

synchronization circuit 3–83

T

TAP
see test-access port

tape and reel 8–90

TBC
see test-bus controller

temperature
also reliability
ambient 8–72, 8–100, 8–111
case 8–72, 8–111
increase 1–71
junction 8–72, 8–100, 8–111

termination 4–35, 4–66
bidirectional bus lines 2–54
maximum line length 4–67
parallel 4–68
series 4–69
when needed 4–66

termination techniques 4–35
AC 4–35
comparison 4–37, 5–42
diode 4–35
series 4–35
shunt 4–35
Thevenin 4–35

test-access port (TAP) 7–63, 7–77, 7–106, 7–117
also IEEE Std 1149.1 (JTAG)
boundary-scan diagram 7–52, 7–145

test-bus controller (TBC) 7–126, 7–147
also IEEE Std 1149.1 (JTAG), boundary scan

test circuit
description 3–77
examine metastable state, using to 3–78

test instructions
see instructions

test methodologies 7–22

test setup 3–93
conditions for good testing 3–110
bidirectional connections 3–104
inputs 3–102
outputs 3–102
supply voltage 3–104
essential conditions 3–93
example 3–104
measuring radiated emissions 6–43

test signal 3–79

testing
also IEEE Std 1149.1 (JTAG), boundary scan, built-in self-test (BIST)
physical-access difficulties 7–45
traditional methods 7–62

thermal characteristics 8–95
also reliability
conduction 8–71
convection 8–71
radiation 8–71

thermal impedance, θ_{JA} 8–7
calculation 8–100
definition 8–7
package area 4–15

thermal resistance 1–72, 1–76

Thevenin termination 4–36, 6–42
also parallel termination
advantages and disadvantages 4–36

thin quad flat package (TQFP) 2–27, 4–14, 8–7, 8–20, 8–24, 8–28
defect rates 8–66
packing methods and quantities 8–10
test sockets 8–12
thermal impedance, θ_{JA} 8–8

thin shrink small-outline package (TSSOP) 2–10, 3–23, 4–13, 4–14, 4–41, 8–18, 8–19, 8–23, 8–24, 8–27, 8–28, 8–57

thin very small-outline package (TVSOP) 4–41, 8–49, 8–57, 8–85
24-pin package 8–58
80-pin package 8–59
100-pin package 8–59
capacitance 8–84, 8–86
component placement 8–62
defect rates 8–66
derating curves 8–73
dimensions
by pin count 8–55
comparison to shrink small-outline package (SSOP) 8–55
comparison to thin shrink small-outline package (TSSOP) 8–55
comparison to thin quad flat package (TQFP) 8–55
electrical data 8–83, 8–86
inductance 8–83, 8–86
JEDEC registration 8–60
lead-to-pad solder joint 8–69
moisture sensitivity 8–89
pad-geometry requirements 8–61
power dissipation 8–73
printed-circuit-board manufacture 8–61
reel dimensions 8–92
reliability 8–86
resistance 8–86
stencil-geometry requirements 8–62
symbolization 8–60
tape and reel 8–91
temperature-cycle test 8–70
test implementation 8–70
test sockets 8–92
thermal impedance 8–73

threshold voltage 1–56, 2–70, 3–82

timing measurement 3–93

TQFP
see thin quad flat package

transceivers
output-damping resistor 1–44
vendor cross reference 1–44

transient power, P_T
calculation 5–62

transient power consumption 8–79, 8–108

transient power dissipation
calculation 4–29

transistor
multiple emitter 1–57

transistor-transistor logic (TTL)
backplane transceiver logic (BTL) translation 4–17
input, output characteristics 2–48
switching standards 2–23
typical noise margin 2–53

transition
low-to-high 2–49
high-to-low 2–50

transition times 1–59

transmission line 4–54, 6–40, 6–42
antenna effect 6–42
components 4–55
driver and receiver, with 6–40
Fourier analysis 4–79
loaded 4–60
lumped loading, with 4–63
matching, without 2–48
termination-resistor value less than Z_O, with 6–41
theory 4–54
types
microstrip lines 4–57
strip lines 4–58

TSSOP
see thin shrink small-outline package

TTL
see transistor-transistor logic

TVSOP
see thin very small-outline package

U

UBT™
see universal bus transceiver

undershoot
see signal undershoot

undervoltage
see signal undershoot

universal bus transceiver (UBT™)
configuration 4–16
portfolio 4–17

V

VCO
see voltage-controlled oscillator

voltage
see supply voltage

voltage divider 2–52
also split termination

voltage peaks
when making contacts to signal lines
with voltage bias 2–71
without voltage bias 2–70

voltage swing 4–10

voltage threshold 4–30

voltage waveforms
impedance matching, with 3–97
incorrect termination (Z_L = 40 Ω), with 3–96
incorrect termination (Z_L = 60 Ω), with 3–98
theoretical 3–95

voltage-controlled oscillator 6–64

W

wave propagation 2–36, 3–39

wave theory
predict signal waveform curves 1–40

waveforms 1–22, 1–33, 1–37, 1–65, 1–68, 3–39, 3–94, 3–95, 4–38, 5–43
balanced drive, with 1–38, 1–39
damping resistor
without 1–34
with 1–34
effect of line length 4–67
Fourier domains 4–56
high drive, with 1–38
impedance mismatch, with 1–35, 1–36
light drive, with 1–39
setup for obtaining 3–61
time domain 4–56
with receiver bus hold 3–30
without receiver bus hold 3–30

Widebus™ 1–14, 4–14

Widebus+™ 4–14, 8–17

Printed in U.S.A.
0597–CP

SDYA002